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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912xeq384j3cal

1.2.3.7 PA[7:0] / ADDR[15:8] / IVD[15:8] — Port A I/O Pins

PA[7:0] are general-purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external address bus. In MCU emulation modes of operation, these pins are used for external address bus and internal visibility read data.

1.2.3.8 PB[7:1] / ADDR[7:1] / IVD[7:1] — Port B I/O Pins

PB[7:1] are general-purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external address bus. In MCU emulation modes of operation, these pins are used for external address bus and internal visibility read data.

1.2.3.9 PB0 / ADDR0 / $\overline{\text{UDS}}$ / IVD[0] — Port B I/O Pin 0

PB0 is a general-purpose input or output pin. In MCU expanded modes of operation, this pin is used for the external address bus ADDR0 or as upper data strobe signal. In MCU emulation modes of operation, this pin is used for external address bus ADDR0 and internal visibility read data IVD0.

1.2.3.10 PC[7:0] / DATA [15:8] — Port C I/O Pins

PC[7:0] are general-purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external data bus.

The input voltage thresholds for PC[7:0] can be configured to reduced levels, to allow data from an external 3.3-V peripheral to be read by the MCU operating at 5.0 V. The input voltage thresholds for PC[7:0] are configured to reduced levels out of reset in expanded and emulation modes. The input voltage thresholds for PC[7:0] are configured to 5-V levels out of reset in normal modes.

1.2.3.11 PD[7:0] / DATA [7:0] — Port D I/O Pins

PD[7:0] are general-purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external data bus.

The input voltage thresholds for PD[7:0] can be configured to reduced levels, to allow data from an external 3.3-V peripheral to be read by the MCU operating at 5.0 V. The input voltage thresholds for PD[7:0] are configured to reduced levels out of reset in expanded and emulation modes. The input voltage thresholds for PC[7:0] are configured to 5-V levels out of reset in normal modes.

1.2.3.12 PE7 / ECLKX2 / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general-purpose input or output pin. ECLKX2 is a free running clock of twice the internal bus frequency, available by default in emulation modes and when enabled in other modes. The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal loop controlled Pierce oscillator is used or whether full swing Pierce oscillator/external clock circuitry is used (refer to Oscillator Configuration). An internal pullup is enabled during reset.

Table 1-14. Interrupt Vector Locations (Sheet 3 of 4)

Vector Address[1]	XGATE Channel ID[2]	Interrupt Source	CCR Mask	Local Enable	STOP Wake up	WAIT Wake up
Vector base + $8A	$45	SCI2	I bit	SCI2CR2 (TIE, TCIE, RIE, ILIE)	Yes	Yes
Vector base + $88	$44	SCI3	I bit	SCI3CR2 (TIE, TCIE, RIE, ILIE)	Yes	Yes
Vector base + $86	$43	SCI4	I bit	SCI4CR2 (TIE, TCIE, RIE, ILIE)	Yes	Yes
Vector base + $84	$42	SCI5	I bit	SCI5CR2 (TIE, TCIE, RIE, ILIE)	Yes	Yes
Vector base + $82	$41	IIC1 Bus	I bit	IBCR (IBIE)	No	Yes
Vector base + $80	$40	Low-voltage interrupt (LVI)	I bit	VREGCTRL (LVIE)	No	Yes
Vector base + $7E	$3F	Autonomous periodical interrupt (API)	I bit	VREGAPICTRL (APIE)	Yes	Yes
Vector base + $7C	—	High Temperature Interrupt	I bit	VREGHTCL (HTIE)	No	Yes
Vector base + $7A	$3D	Periodic interrupt timer channel 0	I bit	PITINTE (PINTE0)	No	Yes
Vector base + $78	$3C	Periodic interrupt timer channel 1	I bit	PITINTE (PINTE1)	No	Yes
Vector base + $76	$3B	Periodic interrupt timer channel 2	I bit	PITINTE (PINTE2)	No	Yes
Vector base + $74	$3A	Periodic interrupt timer channel 3	I bit	PITINTE (PINTE3)	No	Yes
Vector base + $72	$39	XGATE software trigger 0	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $70	$38	XGATE software trigger 1	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $6E	$37	XGATE software trigger 2	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $6C	$36	XGATE software trigger 3	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $6A	$35	XGATE software trigger 4	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $68	$34	XGATE software trigger 5	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $66	$33	XGATE software trigger 6	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $64	$32	XGATE software trigger 7	I bit	XGMCTL (XGIE)	No	Yes
Vector base + $62	Reserved					
Vector base + $60	Reserved					
Vector base + $5E	$2F	Periodic interrupt timer channel 4	I bit	PITINTE (PINTE4)	No	Yes
Vector base + $5C	$2E	Periodic interrupt timer channel 5	I bit	PITINTE (PINTE5)	No	Yes
Vector base + $5A	$2D	Periodic interrupt timer channel 6	I bit	PITINTE (PINTE6)	No	Yes
Vector base + $58	$2C	Periodic interrupt timer channel 7	I bit	PITINTE (PINTE7)	No	Yes
Vector base + $56	$2B	SCI7	I bit	SCI7CR2 (TIE, TCIE, RIE, ILIE)	Yes	Yes
Vector base + $54	$2A	TIM timer channel 0	I bit	TIE (C0I)	No	Yes
Vector base + $52	$29	TIM timer channel 1	I bit	TIE (C1I)	No	Yes
Vector base + $50	$28	TIM timer channel 2	I bit	TIE (C2I)	No	Yes

Chapter 2
Port Integration Module (S12XEPIMV1)

Table 2-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.17	02 Apr 2008		• Corrected reduced drive strength to 1/5 • Separated PE1,0 bit descriptions from other PE GPIO
V01.18	25 Nov 2008	2.3.19/120 2.4.3.4/181	• Corrected alternative functions on Port K (ACC[2:0]) • Corrected functions on PE[5] (MODB) and PE[2] (WE)
V01.19	18 Dec 2009		• Added function independency to reduced drive and wired-or bit descriptions • Minor corrections

2.1 Introduction

2.1.1 Overview

The S12XE Family Port Integration Module establishes the interface between the peripheral modules including the non-multiplexed External Bus Interface module (S12X_EBI) and the I/O pins for all ports. It controls the electrical pin properties as well as the signal prioritization and multiplexing on shared pins.

This document covers:

- Port A and B used as address output of the S12X_EBI
- Port C and D used as data I/O of the S12X_EBI
- Port E associated with the S12X_EBI control signals and the $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ interrupt inputs
- Port K associated with address output and control signals of the S12X_EBI
- Port T associated with 1 ECT module
- Port S associated with 2 SCI and 1 SPI modules
- Port M associated with 4 MSCAN and 1 SCI module
- Port P connected to the PWM and 2 SPI modules - inputs can be used as an external interrupt source
- Port H associated with 4 SCI modules - inputs can be used as an external interrupt source
- Port J associated with 1 MSCAN, 1 SCI, 2 IIC modules and chip select outputs - inputs can be used as an external interrupt source
- Port AD0 and AD1 associated with two 16-channel ATD modules
- Port R associated with 1 standard timer (TIM) module
- Port L associated with 4 SCI modules

2.3.42 Port M Polarity Select Register (PPSM)

Address 0x0255 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Reset	0	0	0	0	0	0	0	0

Figure 2-40. Port M Polarity Select Register (PPSM)

1. Read: Anytime.
   Write: Anytime.

Table 2-38. PPSM Register Field Descriptions

Field	Description
7-0 PPSM	**Port M pull device select**—Determine pull device polarity on input pins This register selects whether a pull-down or a pull-up device is connected to the pin. If CAN is active a pull-up device can be activated on the RXCAN[3:0] inputs, but not a pull-down. 1 A pull-down device is connected to the associated Port M pin, if enabled by the associated bit in register PERM and if the port is used as a general purpose but not as RXCAN. 0 A pull-up device is connected to the associated Port M pin, if enabled by the associated bit in register PERM and if the port is used as general purpose or RXCAN input.

2.3.43 Port M Wired-Or Mode Register (WOMM)

Address 0x0256 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Reset	0	0	0	0	0	0	0	0

Figure 2-41. Port M Wired-Or Mode Register (WOMM)

1. Read: Anytime.
   Write: Anytime.

Table 2-39. WOMM Register Field Descriptions

Field	Description
7-0 WOMM	**Port M wired-or mode**—Enable wired-or functionality This register configures the output pins as wired-or independent of the function used on the pins. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven.This allows a multipoint connection of several serial modules. These bits have no influence on pins used as inputs. 1 Output buffers operate as open-drain outputs. 0 Output buffers operate as push-pull outputs.

2.3.65 Port J Pull Device Enable Register (PERJ)

Address 0x026C Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PERJ7	PERJ6	PERJ5	PERJ4	PERJ3	PERJ2	PERJ1	PERJ0
Reset	1	1	1	1	1	1	1	1

Figure 2-63. Port J Pull Device Enable Register (PERJ)

1. Read: Anytime.
   Write: Anytime.

Table 2-61. PERJ Register Field Descriptions

Field	Description
7-0 PERJ	**Port J pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset all pull device are enabled. 1 Pull device enabled. 0 Pull device disabled.

2.3.66 Port J Polarity Select Register (PPSJ)

Address 0x026D Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PPSJ7	PPSJ6	PPSJ5	PPSJ4	PPSJ3	PPSJ2	PPSJ1	PPSJ0
Reset	0	0	0	0	0	0	0	0

Figure 2-64. Port J Polarity Select Register (PPSJ)

1. Read: Anytime.
   Write: Anytime.

Table 2-62. PPSJ Register Field Descriptions

Field	Description
7-0 PPSJ	**Port J pull device select**—Determine pull device polarity on input pins This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled. 1 A rising edge on the associated Port J pin sets the associated flag bit in the PIFJ register. A pull-down device is connected to the associated Port J pin, if enabled by the associated bit in register PERJ and if the port is used as input. 0 A falling edge on the associated Port J pin sets the associated flag bit in the PIFJ register.A pull-up device is connected to the associated Port J pin, if enabled by the associated bit in register PERJ and if the port is used as input.

- Single Stepping

  Writing a "1" to the XGSS bit will call the RISC core to execute a single instruction. All RISC core registers will be updated accordingly.

- Write accesses to the XGCHID register and the XGCHPL register

  XGATE threads can be initiated and terminated through a 16 write access to the XGCHID and the XGCHPL register or through a 8 bit write access to the XGCHID register. Detailed operation is shown in Table 10-22. Once a thread has been initiated it's code can be either single stepped or it can be executed by leaving debug mode.

Table 10-22. Initiating and Terminating Threads in Debug Mode

Register Content		Single Cycle Write Access to...		Action
XGCHID	XGCHPL	XGCHID	XGCHPL	
0	0	1..127	-(1)	Set new XGCHID Set XGCHPL to 0x01 Initiate new thread
0	0	1..127	0..7	Set new XGCHID Set new XGCHPL Initiate new thread
1..127	0..3	1..127	4..7	Interrupt current thread Set new XGCHID Set new XGCHPL Initiate new thread
1..127	0..7	0	0..7	Terminate current thread. Resume interrupted thread or become idle if no interrupted thread is pending
			-1	
All other combinations				No action

1. 8 bit write access to XGCHID

NOTE

Even though zero is not a valid interrupt priority level of the S12X_INT module, a thread of priority level 0 can be initiated in debug mode. The XGATE handles requests of priority level 0 in the same way as it handles requests of priority levels 1 to 3.

NOTE

All channels 1 to 127 can be initiated by writing to the XGCHID register, even if they are not assigned to any peripheral module.

NOTE

In Debug Mode the XGATE will ignore all requests from peripheral modules.

10.6.1.0.1 Entering Debug Mode

Debug mode can be entered in four ways:

1. Setting XGDBG to "1"

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
Reset	0	0	0	0	0	0	0	0

Figure 14-8. Timer Count Register Low (TCNT)

Read: Anytime

Write: Writable in special modes.

All bits reset to zero.

Table 14-6. TCNT Field Descriptions

Field	Description
15:0 TCNT[15:0]	**Timer Counter Bits** — The 16-bit main timer is an up counter. A read to this register will return the current value of the counter. Access to the counter register will take place in one clock cycle. **Note:** A separate read/write for high byte and low byte in test mode will give a different result than accessing them as a word. The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

14.3.2.6 Timer System Control Register 1 (TSCR1)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-9. Timer System Control Register 1 (TSCR1)

Read or write: Anytime except PRNT bit is write once

All bits reset to zero.

Table 14-7. TSCR1 Field Descriptions

Field	Description
7 TEN	**Timer Enable** 0 Disables the main timer, including the counter. Can be used for reducing power consumption. 1 Allows the timer to function normally. **Note:** If for any reason the timer is not active, there is no ÷64 clock for the pulse accumulator since the ÷64 is generated by the timer prescaler.
6 TSWAI	**Timer Module Stops While in Wait** 0 Allows the timer module to continue running during wait. 1 Disables the timer counter, pulse accumulators and modulus down counter when the MCU is in wait mode. Timer interrupts cannot be used to get the MCU out of wait.

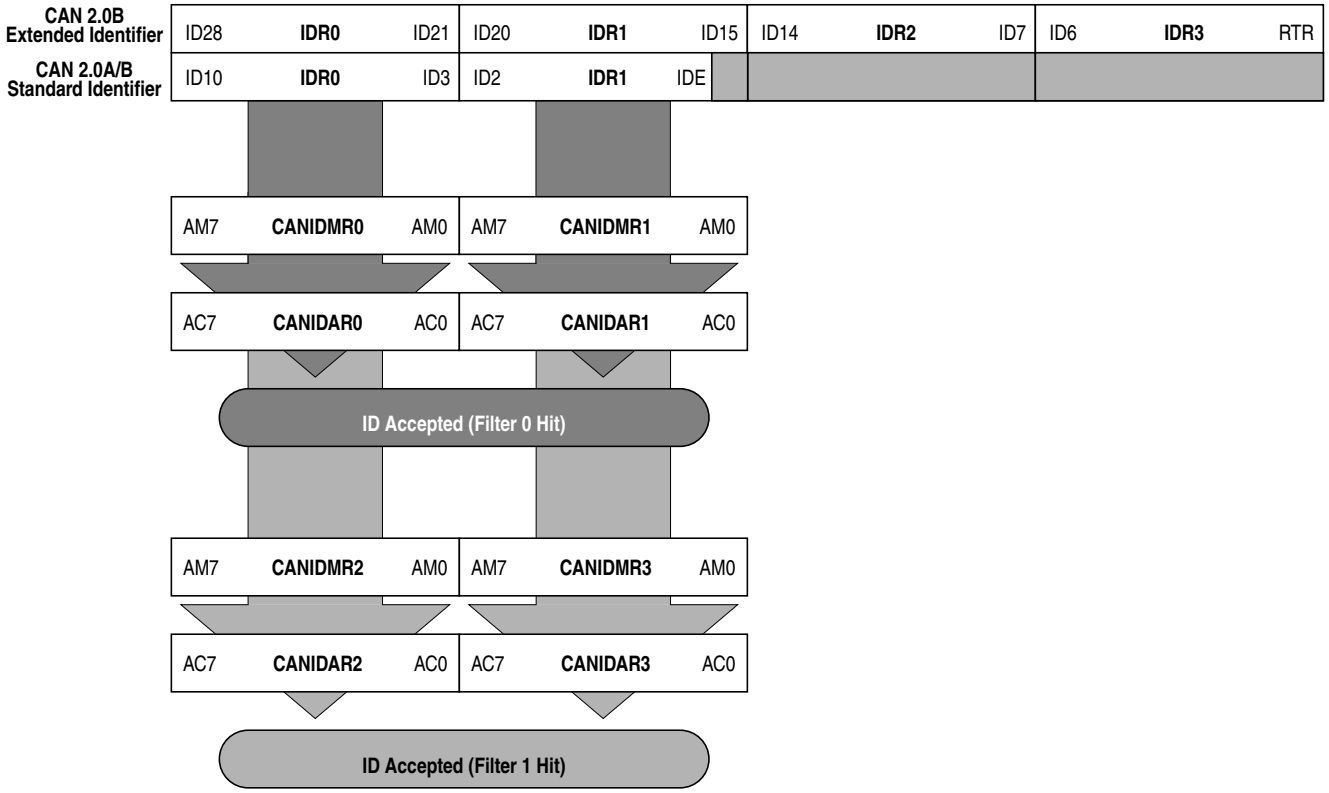


Figure 16-41. 16-bit Maskable Identifier Acceptance Filters

19.3.2.5 PWM Center Align Enable Register (PWMCAE)

The PWMCAE register contains eight control bits for the selection of center aligned outputs or left aligned outputs for each PWM channel. If the CAEx bit is set to a one, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. See Section 19.4.2.5, “Left Aligned Outputs” and Section 19.4.2.6, “Center Aligned Outputs” for a more detailed description of the PWM output modes.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
Reset	0	0	0	0	0	0	0	0

Figure 19-7. PWM Center Align Enable Register (PWMCAE)

Read: Anytime

Write: Anytime

NOTE

Write these bits only when the corresponding channel is disabled.

Table 19-8. PWMCAE Field Descriptions

Field	Description
7–0 CAE[7:0]	**Center Aligned Output Modes on Channels 7–0** 0 Channels 7–0 operate in left aligned output mode. 1 Channels 7–0 operate in center aligned output mode.

19.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R W	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-8. PWM Control Register (PWMCTL)

Read: Anytime

Write: Anytime

There are three control bits for concatenation, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. When channels 6 and 7are concatenated, channel 6 registers become the high order bytes of the double byte channel. When channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel

20.4 Functional Description

This section provides a complete functional description of the SCI block, detailing the operation of the design from the end user perspective in a number of subsections.

Figure 20-14 shows the structure of the SCI module. The SCI allows full duplex, asynchronous, serial communication between the CPU and remote devices, including other CPUs. The SCI transmitter and receiver operate independently, although they use the same baud rate generator. The CPU monitors the status of the SCI, writes the data to be transmitted, and processes received data.

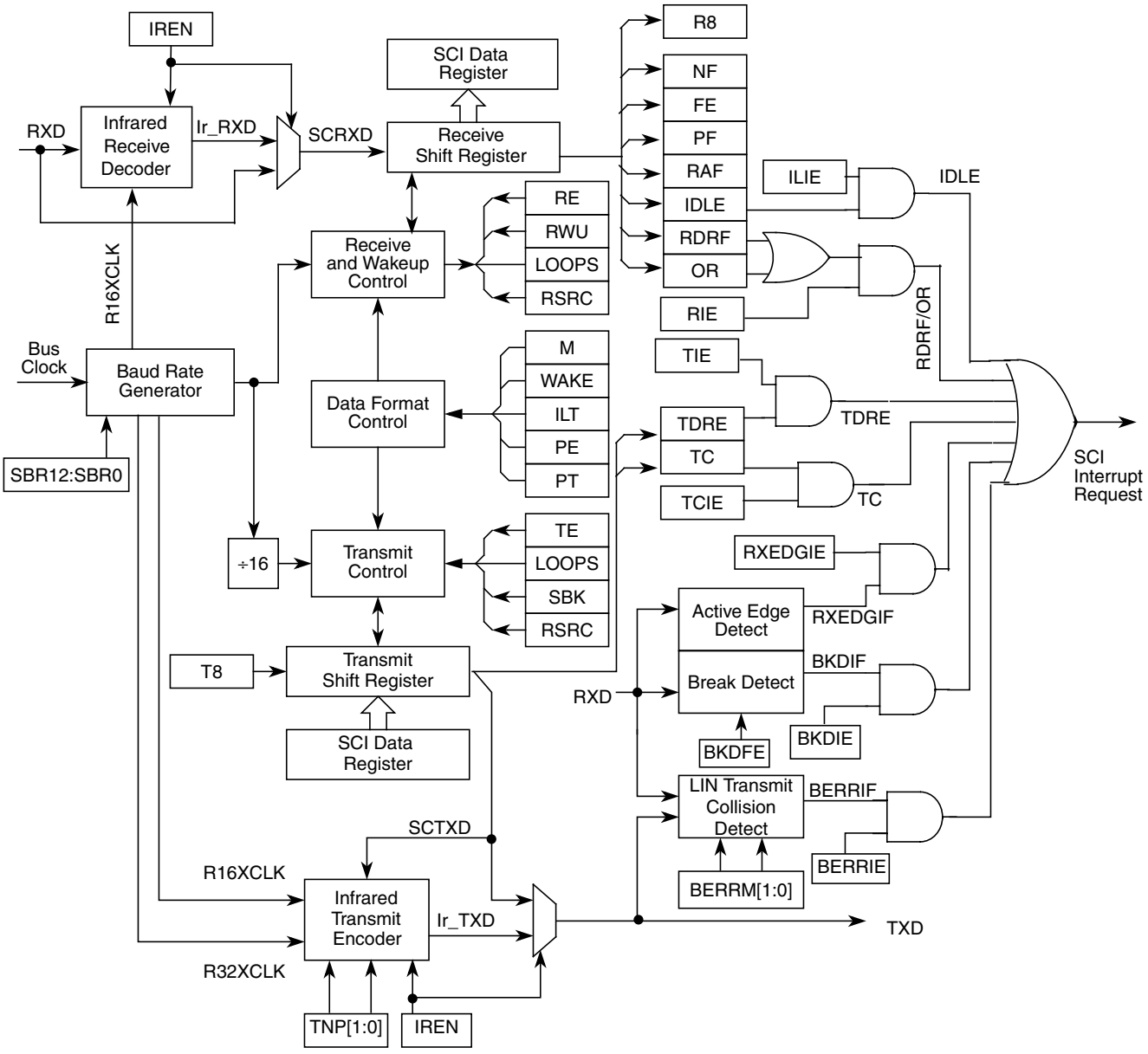


Figure 20-14. Detailed SCI Block Diagram

Table 24-62. Full Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 24-30)
		Set if an invalid DFPART or ERPART selection is supplied(1)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

1. As defined by the maximum ERPART for FTM256K2.

24.4.2.15 Erase Verify D-Flash Section Command

The Erase Verify D-Flash Section command will verify that a section of code in the D-Flash user partition is erased. The Erase Verify D-Flash Section command defines the starting point of the data to be verified and the number of words.

Table 24-63. Erase Verify D-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [22:16] to identify the D-Flash block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify D-Flash Section command, the Memory Controller will verify the selected section of D-Flash memory is erased. The CCIF flag will set after the Erase Verify D-Flash Section operation has completed.

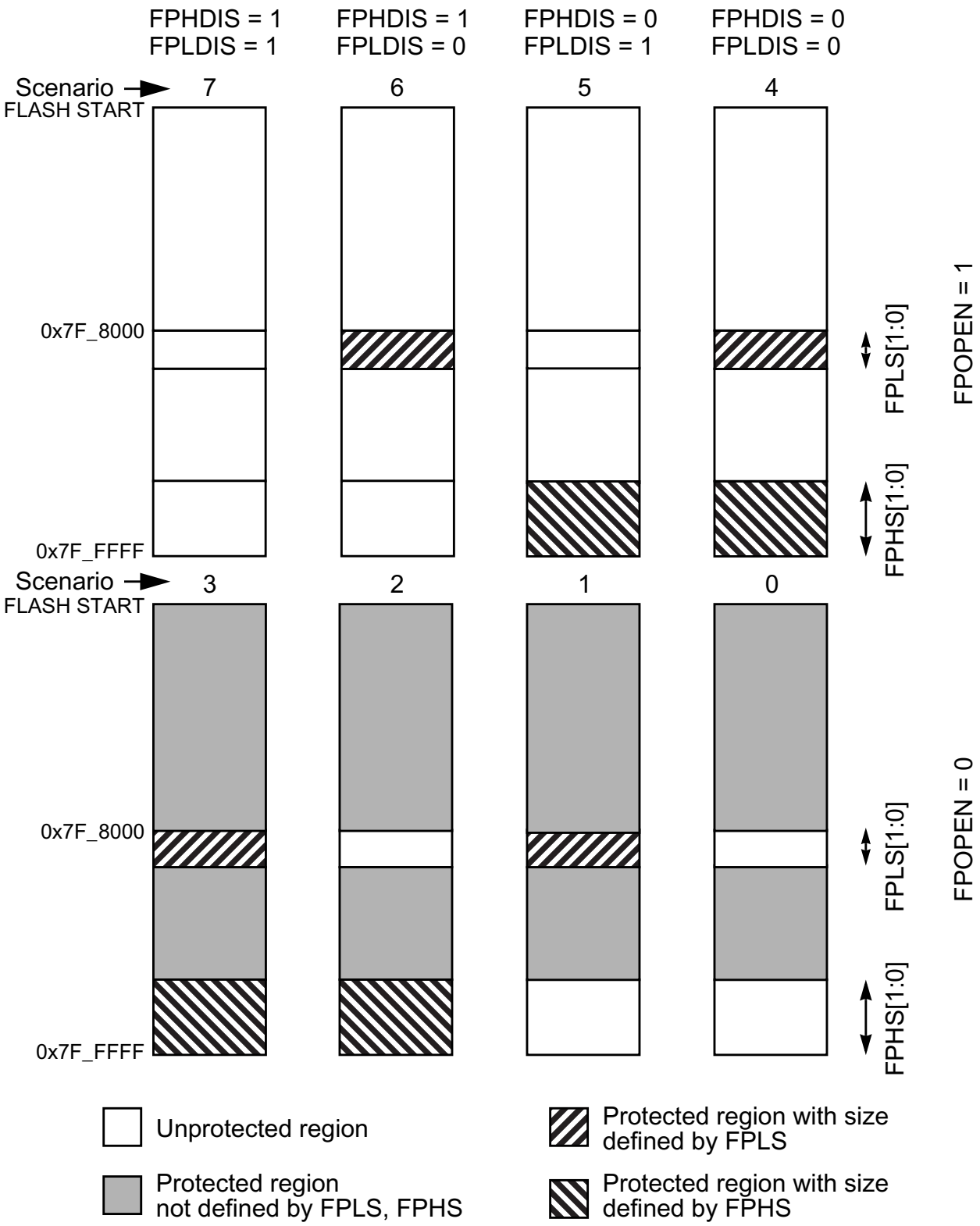


Figure 25-14. P-Flash Protection Scenarios

values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

Table 26-46. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 26-30)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed(1)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
FERSTAT	EPVIOLIF	None

1. If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

26.4.2.8 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and D-Flash memory space including the EEE nonvolatile information register.

Table 26-47. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

27.4.1.3 Valid Flash Module Commands

Table 27-30. Flash Commands by Mode

FCMD	Command	Unsecured				Secured			
		NS (1)	NX (2)	SS(3)	ST(4)	NS (5)	NX (6)	SS(7)	ST(8)
0x01	Erase Verify All Blocks	*	*	*	*	*	*	*	*
0x02	Erase Verify Block	*	*	*	*	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	*	*			
0x04	Read Once	*	*	*	*	*			
0x05	Load Data Field	*	*	*	*	*			
0x06	Program P-Flash	*	*	*	*	*			
0x07	Program Once	*	*	*	*	*			
0x08	Erase All Blocks			*	*			*	*
0x09	Erase P-Flash Block	*	*	*	*	*			
0x0A	Erase P-Flash Sector	*	*	*	*	*			
0x0B	Unsecure Flash			*	*			*	*
0x0C	Verify Backdoor Access Key	*				*			
0x0D	Set User Margin Level	*	*	*	*	*			
0x0E	Set Field Margin Level			*	*				
0x0F	Full Partition D-Flash			*	*				
0x10	Erase Verify D-Flash Section	*	*	*	*	*			
0x11	Program D-Flash	*	*	*	*	*			
0x12	Erase D-Flash Sector	*	*	*	*	*			
0x13	Enable EEPROM Emulation	*	*	*	*	*	*	*	*
0x14	Disable EEPROM Emulation	*	*	*	*	*	*	*	*
0x15	EEPROM Emulation Query	*	*	*	*	*	*	*	*
0x20	Partition D-Flash	*	*	*	*	*	*	*	*

1. Unsecured Normal Single Chip mode.
2. Unsecured Normal Expanded mode.
3. Unsecured Special Single Chip mode.
4. Unsecured Special Mode.
5. Secured Normal Single Chip mode.
6. Secured Normal Expanded mode.
7. Secured Special Single Chip mode.
8. Secured Special Mode.

Table 28-9. FDIV vs OSCCLK Frequency

OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]
MIN(1)	MAX(2)		MIN1	MAX2		MIN1	MAX2	
			33.60	34.65	0x20	67.20	68.25	0x40
1.60	2.10	0x01	34.65	35.70	0x21	68.25	69.30	0x41
2.40	3.15	0x02	35.70	36.75	0x22	69.30	70.35	0x42
3.20	4.20	0x03	36.75	37.80	0x23	70.35	71.40	0x43
4.20	5.25	0x04	37.80	38.85	0x24	71.40	72.45	0x44
5.25	6.30	0x05	38.85	39.90	0x25	72.45	73.50	0x45
6.30	7.35	0x06	39.90	40.95	0x26	73.50	74.55	0x46
7.35	8.40	0x07	40.95	42.00	0x27	74.55	75.60	0x47
8.40	9.45	0x08	42.00	43.05	0x28	75.60	76.65	0x48
9.45	10.50	0x09	43.05	44.10	0x29	76.65	77.70	0x49
10.50	11.55	0x0A	44.10	45.15	0x2A	77.70	78.75	0x4A
11.55	12.60	0x0B	45.15	46.20	0x2B	78.75	79.80	0x4B
12.60	13.65	0x0C	46.20	47.25	0x2C	79.80	80.85	0x4C
13.65	14.70	0x0D	47.25	48.30	0x2D	80.85	81.90	0x4D
14.70	15.75	0x0E	48.30	49.35	0x2E	81.90	82.95	0x4E
15.75	16.80	0x0F	49.35	50.40	0x2F	82.95	84.00	0x4F
16.80	17.85	0x10	50.40	51.45	0x30	84.00	85.05	0x50
17.85	18.90	0x11	51.45	52.50	0x31	85.05	86.10	0x51
18.90	19.95	0x12	52.50	53.55	0x32	86.10	87.15	0x52
19.95	21.00	0x13	53.55	54.60	0x33	87.15	88.20	0x53
21.00	22.05	0x14	54.60	55.65	0x34	88.20	89.25	0x54
22.05	23.10	0x15	55.65	56.70	0x35	89.25	90.30	0x55
23.10	24.15	0x16	56.70	57.75	0x36	90.30	91.35	0x56
24.15	25.20	0x17	57.75	58.80	0x37	91.35	92.40	0x57
25.20	26.25	0x18	58.80	59.85	0x38	92.40	93.45	0x58
26.25	27.30	0x19	59.85	60.90	0x39	93.45	94.50	0x59
27.30	28.35	0x1A	60.90	61.95	0x3A	94.50	95.55	0x5A
28.35	29.40	0x1B	61.95	63.00	0x3B	95.55	96.60	0x5B
29.40	30.45	0x1C	63.00	64.05	0x3C	96.60	97.65	0x5C
30.45	31.50	0x1D	64.05	65.10	0x3D	97.65	98.70	0x5D
31.50	32.55	0x1E	65.10	66.15	0x3E	98.70	99.75	0x5E
32.55	33.60	0x1F	66.15	67.20	0x3F	99.75	100.80	0x5F

1. FDIV shown generates an FCLK frequency of >0.8 MHz

2. FDIV shown generates an FCLK frequency of 1.05 MHz

28.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Offset Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	KEYEN[1:0]		RNV[5:2]				SEC[1:0]	
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 28-6. Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x7F_FF0F located in P-Flash memory (see Table 28-3) as indicated by reset condition F in Figure 28-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 28-10. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 28-11.
5–2 RNV[5:2}	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 28-12. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 28-11. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED(1)
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

Table 28-66. Erase Verify D-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 28-30)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the global address [22:0] points to an area of the D-Flash EEE partition
		Set if the requested section breaches the end of the D-Flash block or goes into the D-Flash EEE partition
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

28.4.2.17 Program D-Flash Command

The Program D-Flash operation programs one to four previously erased words in the D-Flash user partition. The Program D-Flash operation will confirm that the targeted location(s) were successfully programmed upon completion.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 28-67. Program D-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [22:16] to identify the D-Flash block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program D-Flash command, the user-supplied words will be transferred to the Memory Controller and be programmed. The CCOBIX index value at Program D-Flash command launch determines how many words will be programmed in the D-Flash block. No protection checks are made in the Program D-Flash operation on the D-Flash block, only access error checks. The CCIF flag is set when the operation has completed.

A.5 Output Loads

A.5.1 Resistive Loads

The voltage regulator is intended to supply the internal logic and oscillator. It allows no external DC loads.

A.5.2 Capacitive Loads

The capacitive loads are specified in Table A-22. Ceramic capacitors with X7R dielectricum are required.

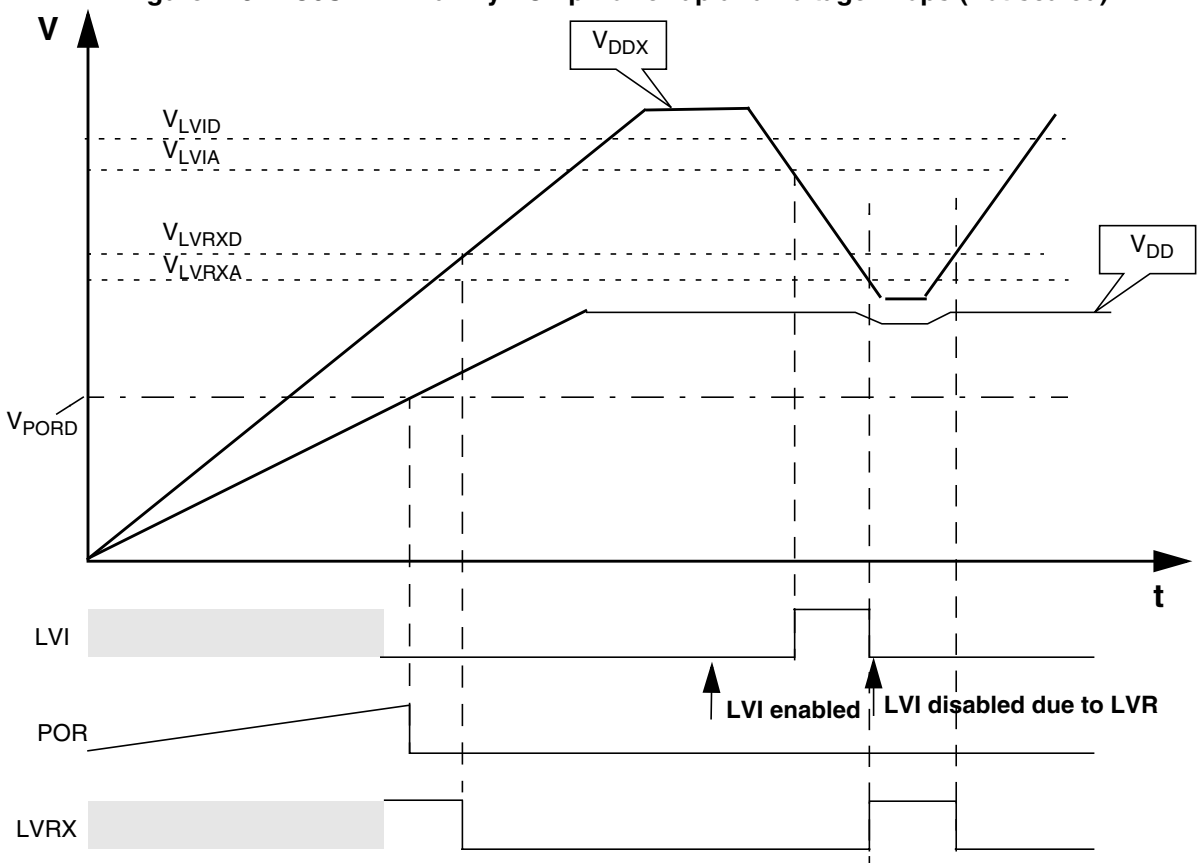
Table A-22. - Required Capacitive Loads

Num	Characteristic	Symbol	Min	Recommended	Max	Unit
1	VDD/VDDF external capacitive load	C_{DDext}	176	220	264	nF
3	VDDPLL external capacitive load	$C_{DDPLLext}$	80	220	264	nF

A.5.3 Chip Power-up and Voltage Drops

LVI (low voltage interrupt), POR (power-on reset) and LVRs (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is shown in Figure A-3 .

Figure A-3. MC9S12XE-Family - Chip Power-up and Voltage Drops (not scaled)



0x0040–0x007F Enhanced Capture Timer 16-Bit 8-Channels (ECT) Map (Sheet 1 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0040	TIOS	R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		W								
0x0041	CFORC	R	0	0	0	0	0	0	0	0
		W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
0x0042	OC7M	R	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		W								
0x0043	OC7D	R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		W								
0x0044	TCNT (high)	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
		W								
0x0045	TCNT (low)	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
		W								
0x0046	TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
		W								
0x0047	TTOV	R	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		W								
0x0048	TCTL1	R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		W								
0x0049	TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		W								
0x004A	TCTL3	R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		W								
0x004B	TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		W								
0x004C	TIE	R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		W								
0x004D	TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
		W								
0x004E	TFLG1	R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		W								
0x004F	TFLG2	R	TOF	0	0	0	0	0	0	0
		W								
0x0050	TC0 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0051	TC0 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0052	TC1 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0053	TC1 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0054	TC2 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0055	TC2 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0040–0x007F Enhanced Capture Timer 16-Bit 8-Channels (ECT) Map (Sheet 3 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x006D	TIMTST	R	0	0	0	0	0	0	0	0
		W	Reserved For Factory Test							
0x006E	PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
		W								
0x006F	PTMCPSR	R	PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0
		W								
0x0070	PBCTL	R	0	PBEN	0	0	0	0	PBOVI	0
		W								
0x0071	PBFLG	R	0	0	0	0	0	0	PBOVF	0
		W								
0x0072	PA3H	R	PA3H7	PA3H6	PA3H5	PA3H4	PA3H3	PA3H2	PA3H1	PA3H0
		W								
0x0073	PA2H	R	PA2H7	PA2H6	PA2H5	PA2H4	PA2H3	PA2H2	PA2H1	PA2H0
		W								
0x0074	PA1H	R	PA1H7	PA1H6	PA1H5	PA1H4	PA1H3	PA1H2	PA1H1	PA1H 0
		W								
0x0075	PA0H	R	PA0H7	PA0H6	PA0H5	PA0H4	PA0H3	PA0H2	PA0H1	PA0H0
		W								
0x0076	MCCNT (hi)	R	MCCNT15	MCCNT14	MCCNT13	MCCNT12	MCCNT11	MCCNT10	MCCNT9	MCCNT8
		W								
0x0077	MCCNT (lo)	R	MCCNT7	MCCNT6	MCCNT5	MCCNT4	MCCNT3	MCCNT2	MCCNT1	MCCNT0
		W								
0x0078	TC0H (hi)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
		W								
0x0079	TC0H (lo)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
		W								
0x007A	TC1H (hi)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
		W								
0x007B	TC1H (lo)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
		W								
0x007C	TC2H (hi)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
		W								
0x007D	TC2H (lo)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
		W								
0x007E	TC3H (hi)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
		W								
0x007F	TC3H (lo)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
		W								