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Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	119
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xeq512bvag

Table 1-14. Interrupt Vector Locations (Sheet 4 of 4)

Vector Address ⁽¹⁾	XGATE Channel ID ⁽²⁾	Interrupt Source	CCR Mask	Local Enable	STOP Wake up	WAIT Wake up
Vector base+ \$4E	\$27	TIM timer channel 3	I bit	TIE (C3I)	No	Yes
Vector base + \$4C	\$26	TIM timer channel 4	I bit	TIE (C4I)	No	Yes
Vector base+ \$4A	\$25	TIM timer channel 5	I bit	TIE (C5I)	No	Yes
Vector base+ \$48	\$24	TIM timer channel 6	I bit	TIE (C6I)	No	Yes
Vector base+ \$46	\$23	TIM timer channel 7	I bit	TIE (C7I)	No	Yes
Vector base+ \$44	\$22	TIM timer overflow	I bit	TSRC2 (TOF)	No	Yes
Vector base + \$42	\$21	TIM Pulse accumulator A overflow	I bit	PACTL (PAOVI)	No	Yes
Vector base+ \$40	\$20	TIM Pulse accumulator input edge	I bit	PACTL (PAI)	No	Yes
Vector base + \$3E	\$1F	ATD0 Compare Interrupt	I bit	ATD0CTL2 (ACMPIE)	Yes	Yes
Vector base + \$3C	\$1E	ATD1 Compare Interrupt	I bit	ATD1CTL2 (ACMPIE)	Yes	Yes
Vector base+ \$18 to Vector base + \$3A	Reserved					
Vector base + \$16	—	XGATE software error interrupt	None	None	No	Yes
Vector base + \$14	—	MPU Access Error	None	None	No	No
Vector base + \$12	—	System Call Interrupt (SYS)	—	None	—	—
Vector base + \$10	—	Spurious interrupt	—	None	—	—

1. 16 bits vector address based

2. For detailed description of XGATE channel ID refer to XGATE Block Guide

1.6.3 Effects of Reset

When a reset occurs, MCU registers and control bits are initialized. Refer to the respective block descriptions for register reset states.

On each reset, the Flash module executes a reset sequence to load Flash configuration registers and initialize the buffer RAM EEE partition, if required.

1.6.3.1 Flash Configuration Reset Sequence (Core Hold Phase)

On each reset, the Flash module will hold CPU activity while loading Flash module registers and configuration from the Flash memory. The duration of this phase is given as t_{RST} in the device electrical parameter specification. If double faults are detected in the reset phase, Flash module protection and security may be active on leaving reset. This is explained in more detail in the Flash module section.

1.6.3.2 EEE Reset Sequence Phase (Core Active Phase)

During this phase of the reset sequence (following on from the core hold phase) the CPU can execute instructions while the FTM initialization completes and, if configured for EEE operation, the EEE RAM

Table 2-103. Register availability per port⁽¹⁾

Port	Data	Input	Data Direction	Reduced Drive	Pull Enable	Polarity Select	Wired-Or Mode	Interrupt Enable	Interrupt Flag	Routing
A	yes	-	yes	yes	yes	-	-	-	-	-
B	yes	-	yes			-	-	-	-	-
C	yes	-	yes			-	-	-	-	-
D	yes	-	yes			-	-	-	-	-
E	yes	-	yes			-	-	-	-	-
K	yes	-	yes			-	-	-	-	-
T	yes	yes	yes	yes	yes	yes	-	-	-	-
S	yes	yes	yes	yes	yes	yes	yes	-	-	yes
M	yes	yes	yes	yes	yes	yes	yes	-	-	yes
P	yes	yes	yes	yes	yes	yes	-	yes	yes	-
H	yes	yes	yes	yes	yes	yes	-	yes	yes	-
J	yes	yes	yes	yes	yes	yes	-	yes	yes	-
AD0	yes	-	yes	yes	yes	-	-	-	-	-
AD1	yes	-	yes	yes	yes	-	-	-	-	-
R	yes	yes	yes	yes	yes	yes	-	-	-	-
L	yes	yes	yes	yes	yes	yes	yes	-	-	yes
F	yes	yes	yes	yes	yes	yes	-	-	-	yes

1. Each cell represents one register with individual configuration bits

2.4.2.1 Data register (PORTx, PTx)

This register holds the value driven out to the pin if the pin is used as a general purpose I/O.

Writing to this register has only an effect on the pin if the pin is used as general purpose output. When reading this address, the buffered state of the pin is returned if the associated data direction register bit is set to “0”.

If the data direction register bits are set to logic level “1”, the contents of the data register is returned. This is independent of any other configuration ([Figure 2-107](#)).

2.4.2.2 Input register (PTIx)

This is a read-only register and always returns the buffered state of the pin ([Figure 2-107](#)).

2.4.2.3 Data direction register (DDRx)

This register defines whether the pin is used as an input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored ([Figure 2-107](#)).

11.3.2 Register Descriptions

This section describes in address order all the S12XECRG registers and their individual bits.

11.3.2.1 S12XECRG Synthesizer Register (SYNR)

The SYNR register controls the multiplication factor of the IPLL and selects the VCO frequency range.

Module Base + 0x0000

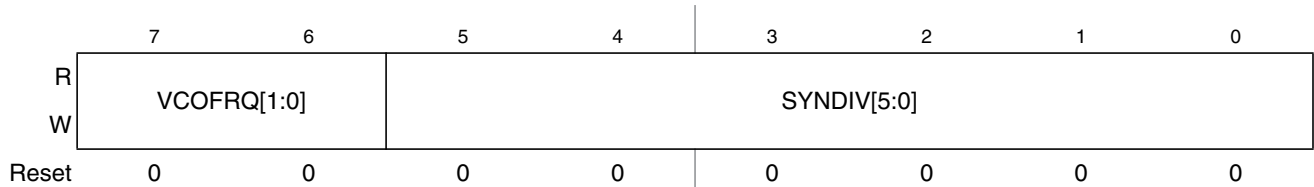


Figure 11-3. S12XECRG Synthesizer Register (SYNR)

Read: Anytime

Write: Anytime except if PLLSEL = 1

NOTE

Write to this register initializes the lock detector bit.

$$f_{VCO} = 2 \times f_{OSC} \times \frac{(SYNDIV + 1)}{(REFDIV + 1)}$$

$$f_{PLL} = \frac{f_{VCO}}{2 \times POSTDIV}$$

$$f_{BUS} = \frac{f_{PLL}}{2}$$

NOTE

f_{VCO} must be within the specified VCO frequency lock range. F_{BUS} (Bus Clock) must not exceed the specified maximum. If POSTDIV = \$00 then f_{PLL} is same as f_{VCO} (divide by one).

The VCOFRQ[1:0] bit are used to configure the VCO gain for optimal stability and lock time. For correct IPLL operation the VCOFRQ[1:0] bits have to be selected according to the actual target VCOCLK frequency as shown in Table 11-2. Setting the VCOFRQ[1:0] bits wrong can result in a non functional IPLL (no locking and/or insufficient stability).

Table 11-2. VCO Clock Frequency Selection

VCOCLK Frequency Ranges	VCOFRQ[1:0]
32MHz <= f_{VCO} <= 48MHz	00
48MHz < f_{VCO} <= 80MHz	01
Reserved	10
80MHz < f_{VCO} <= 120MHz	11

Table 14-11. The OC7 and OCx event priority

OC7M7=0				OC7M7=1			
OC7Mx=1		OC7Mx=0		OC7Mx=1		OC7Mx=0	
TC7=TCx	TC7>TCx	TC7=TCx	TC7>TCx	TC7=TCx	TC7>TCx	TC7=TCx	TC7>TCx
IOCx=OC7Dx IOC7=OM7/O L7	IOCx=OC7Dx +OMx/OLx IOC7=OM7/O L7	IOCx=OMx/OLx IOC7=OM7/OL7		IOCx=OC7Dx IOC7=OC7D7	IOCx=OC7Dx +OMx/OLx IOC7=OC7D7	IOCx=OMx/OLx IOC7=OC7D7	

Note: in Table 14-11, the IOS7 and IOSx should be set to 1

IOSx is the register TIOS bit x,

OC7Mx is the register OC7M bit x,

TCx is timer Input Capture/Output Compare register,

IOCx is channel x,

OMx/OLx is the register TCTL1/TCTL2,

OC7Dx is the register OC7D bit x.

IOCx = OC7Dx+ OMx/OLx, means that both OC7 event and OCx event will change channel x value.

14.3.2.9 Timer Control Register 3/Timer Control Register 4 (TCTL3/TCTL4)

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
W								
Reset	0	0	0	0	0	0	0	0

Figure 14-13. Timer Control Register 3 (TCTL3)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
W								
Reset	0	0	0	0	0	0	0	0

Figure 14-14. Timer Control Register 4 (TCTL4)

Read or write: Anytime

All bits reset to zero.

16.4.5.5 MSCAN Sleep Mode

The CPU can request the MSCAN to enter this low power mode by asserting the SLPRQ bit in the CANCTL0 register. The time when the MSCAN enters sleep mode depends on a fixed synchronization delay and its current activity:

- If there are one or more message buffers scheduled for transmission (TXEx = 0), the MSCAN will continue to transmit until all transmit message buffers are empty (TXEx = 1, transmitted successfully or aborted) and then goes into sleep mode.
- If the MSCAN is receiving, it continues to receive and goes into sleep mode as soon as the CAN bus next becomes idle.
- If the MSCAN is neither transmitting nor receiving, it immediately goes into sleep mode.

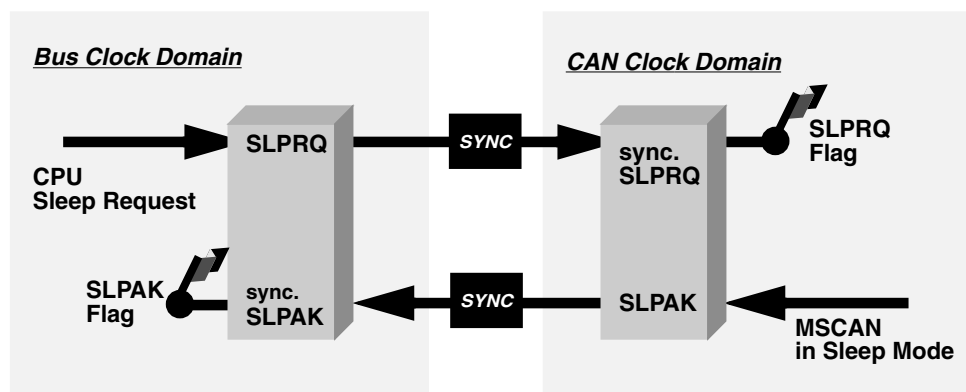


Figure 16-46. Sleep Request / Acknowledge Cycle

NOTE

The application software must avoid setting up a transmission (by clearing one or more TXEx flag(s)) and immediately request sleep mode (by setting SLPRQ). Whether the MSCAN starts transmitting or goes into sleep mode directly depends on the exact sequence of operations.

If sleep mode is active, the SLPRQ and SLPK bits are set (Figure 16-46). The application software must use SLPK as a handshake indication for the request (SLPRQ) to go into sleep mode.

When in sleep mode (SLPRQ = 1 and SLPK = 1), the MSCAN stops its internal clocks. However, clocks that allow register accesses from the CPU side continue to run.

If the MSCAN is in bus-off state, it stops counting the 128 occurrences of 11 consecutive recessive bits due to the stopped clocks. TXCAN remains in a recessive state. If RXF = 1, the message can be read and RXF can be cleared. Shifting a new message into the foreground buffer of the receiver FIFO (RxFG) does not take place while in sleep mode.

It is possible to access the transmit buffers and to clear the associated TXE flags. No message abort takes place while in sleep mode.

Table 18-2. PITCFLMT Field Descriptions

Field	Description
7 PITE	PIT Module Enable Bit — This bit enables the PIT module. If PITE is cleared, the PIT module is disabled and flag bits in the PITTF register are cleared. When PITE is set, individually enabled timers (PCE set) start down-counting with the corresponding load register values. 0 PIT disabled (lower power consumption). 1 PIT is enabled.
6 PITSWAI	PIT Stop in Wait Mode Bit — This bit is used for power conservation while in wait mode. 0 PIT operates normally in wait mode 1 PIT clock generation stops and freezes the PIT module when in wait mode
5 PITFRZ	PIT Counter Freeze while in Freeze Mode Bit — When during debugging a breakpoint (freeze mode) is encountered it is useful in many cases to freeze the PIT counters to avoid e.g. interrupt generation. The PITFRZ bit controls the PIT operation while in freeze mode. 0 PIT operates normally in freeze mode 1 PIT counters are stalled when in freeze mode
1:0 PFLMT[1:0]	PIT Force Load Bits for Micro Timer 1:0 — These bits have only an effect if the corresponding micro timer is active and if the PIT module is enabled (PITE set). Writing a one into a PFLMT bit loads the corresponding 8-bit micro timer load register into the 8-bit micro timer down-counter. Writing a zero has no effect. Reading these bits will always return zero. Note: A micro timer force load affects all timer channels that use the corresponding micro time base.

18.3.0.2 PIT Force Load Timer Register (PITFLT)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W					PFLT3	PFLT2	PFLT1	PFLT0
Reset	0	0	0	0	0	0	0	0

Figure 18-4. PIT Force Load Timer Register (PITFLT)

Read: Anytime

Write: Anytime

Table 18-3. PITFLT Field Descriptions

Field	Description
3:0 PFLT[3:0]	PIT Force Load Bits for Timer 3-0 — These bits have only an effect if the corresponding timer channel (PCE set) is enabled and if the PIT module is enabled (PITE set). Writing a one into a PFLT bit loads the corresponding 16-bit timer load register into the 16-bit timer down-counter. Writing a zero has no effect. Reading these bits will always return zero.

The SCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (SCIDRH/L) to the transmitter shift register. The transmit driver routine may respond to this flag by writing another byte to the Transmitter buffer (SCIDRH/SCIDRL), while the shift register is still shifting out the first byte.

To initiate an SCI transmission:

1. Configure the SCI:
 - a) Select a baud rate. Write this value to the SCI baud registers (SCIBDH/L) to begin the baud rate generator. Remember that the baud rate generator is disabled when the baud rate is zero. Writing to the SCIBDH has no effect without also writing to SCIBDL.
 - b) Write to SCICR1 to configure word length, parity, and other configuration bits (LOOPS,RSRC,M,WAKE,ILT,PE,PT).
 - c) Enable the transmitter, interrupts, receive, and wake up as required, by writing to the SCICR2 register bits (TIE,TCIE,RIE,ILIE,TE,RE,RWU,SBK). A preamble or idle character will now be shifted out of the transmitter shift register.
2. Transmit Procedure for each byte:
 - a) Poll the TDRE flag by reading the SCISR1 or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to one.
 - b) If the TDRE flag is set, write the data to be transmitted to SCIDRH/L, where the ninth bit is written to the T8 bit in SCIDRH if the SCI is in 9-bit data format. A new transmission will not result until the TDRE flag has been cleared.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to be transmitted from SCIDRH/L, which happens, generally speaking, a little over half-way through the stop bit of the previous frame. Specifically, this transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Writing the TE bit from 0 to a 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the SCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

Hardware supports odd or even parity. When parity is enabled, the most significant bit (MSB) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in SCI status register 1 (SCISR1) becomes set when the SCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the SCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCICR2) is also set, the TDRE flag generates a transmitter interrupt request.

20.4.6.6.1 Idle Input line Wakeup (WAKE = 0)

In this wakeup method, an idle condition on the RXD pin clears the RWU bit and wakes up the SCI. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle character appears on the RXD pin.

Idle line wakeup requires that messages be separated by at least one idle character and that no message contains idle characters.

The idle character that wakes a receiver does not set the receiver idle bit, IDLE, or the receive data register full flag, RDRF.

The idle line type bit, ILT, determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit. ILT is in SCI control register 1 (SCICR1).

20.4.6.6.2 Address Mark Wakeup (WAKE = 1)

In this wakeup method, a logic 1 in the most significant bit (MSB) position of a frame clears the RWU bit and wakes up the SCI. The logic 1 in the MSB position marks a frame as an address frame that contains addressing information. All receivers evaluate the addressing information, and the receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD pin.

The logic 1 MSB of an address frame clears the receiver's RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wakeup allows messages to contain idle characters but requires that the MSB be reserved for use in address frames.

NOTE

With the WAKE bit clear, setting the RWU bit after the RXD pin has been idle can cause the receiver to wake up immediately.

20.4.7 Single-Wire Operation

Normally, the SCI uses two pins for transmitting and receiving. In single-wire operation, the RXD pin is disconnected from the SCI. The SCI uses the TXD pin for both receiving and transmitting.

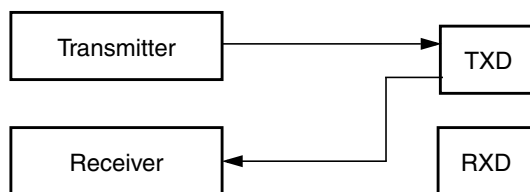


Figure 20-30. Single-Wire Operation (LOOPS = 1, RSRC = 1)

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

22.1.1 Features

The TIM16B8CV2 includes these distinctive features:

- Eight input capture/output compare channels.
- Clock prescaling.
- 16-bit counter.
- 16-bit pulse accumulator.

22.1.2 Modes of Operation

Stop:	Timer is off because clocks are stopped.
Freeze:	Timer counter keep on running, unless TSFRZ in TSCR1 (0x0006) is set to 1.
Wait:	Counters keep on running, unless TSWAI in TSCR1 (0x0006) is set to 1.
Normal:	Timer counter keep on running, unless TEN in TSCR1 (0x0006) is cleared to 0.

Table 24-18. FERSTAT Field Descriptions

Field	Description
7 ERSERIF	EEE Erase Error Interrupt Flag — The setting of the ERSERIF flag occurs due to an error in a Flash erase command that resulted in the erase operation not being successful during EEE operations. The ERSERIF flag is cleared by writing a 1 to ERSERIF. Writing a 0 to the ERSERIF flag has no effect on ERSERIF. While ERSERIF is set, it is possible to write to the buffer RAM EEE partition but the data written will not be transferred to the D-Flash EEE partition. 0 Erase command successfully completed on the D-Flash EEE partition 1 Erase command failed on the D-Flash EEE partition
6 PGMERIF	EEE Program Error Interrupt Flag — The setting of the PGMERIF flag occurs due to an error in a Flash program command that resulted in the program operation not being successful during EEE operations. The PGMERIF flag is cleared by writing a 1 to PGMERIF. Writing a 0 to the PGMERIF flag has no effect on PGMERIF. While PGMERIF is set, it is possible to write to the buffer RAM EEE partition but the data written will not be transferred to the D-Flash EEE partition. 0 Program command successfully completed on the D-Flash EEE partition 1 Program command failed on the D-Flash EEE partition
4 EPVIOLIF	EEE Protection Violation Interrupt Flag —The setting of the EPVIOLIF flag indicates an attempt was made to write to a protected area of the buffer RAM EEE partition. The EPVIOLIF flag is cleared by writing a 1 to EPVIOLIF. Writing a 0 to the EPVIOLIF flag has no effect on EPVIOLIF. While EPVIOLIF is set, it is possible to write to the buffer RAM EEE partition as long as the address written to is not in a protected area. 0 No EEE protection violation 1 EEE protection violation detected
3 ERSVIF1	EEE Error Interrupt 1 Flag —The setting of the ERSVIF1 flag indicates that the memory controller was unable to change the state of a D-Flash EEE sector. The ERSVIF1 flag is cleared by writing a 1 to ERSVIF1. Writing a 0 to the ERSVIF1 flag has no effect on ERSVIF1. While ERSVIF1 is set, it is possible to write to the buffer RAM EEE partition but the data written will not be transferred to the D-Flash EEE partition. 0 No EEE sector state change error detected 1 EEE sector state change error detected
2 ERSVIF0	EEE Error Interrupt 0 Flag —The setting of the ERSVIF0 flag indicates that the memory controller was unable to format a D-Flash EEE sector for EEE use. The ERSVIF0 flag is cleared by writing a 1 to ERSVIF0. Writing a 0 to the ERSVIF0 flag has no effect on ERSVIF0. While ERSVIF0 is set, it is possible to write to the buffer RAM EEE partition but the data written will not be transferred to the D-Flash EEE partition. 0 No EEE sector format error detected 1 EEE sector format error detected
1 DFDIF	Double Bit Fault Detect Interrupt Flag — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation. The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF. 0 No double bit fault detected 1 Double bit fault detected or an invalid Flash array read operation attempted
0 SFDIF	Single Bit Fault Detect Interrupt Flag — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation. The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or an invalid Flash array read operation attempted

24.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.



Table 25-3. Flash Configuration Field⁽¹⁾

Global Address	Size (Bytes)	Description
0x7F_FF0F ²	1	Flash Security byte Refer to Section 25.3.2.2 , “Flash Security Register (FSEC)”

- 1. Older versions may have swapped protection byte addresses
- 2. 0x7FF08 - 0x7F_FF0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0x7F_FF08 - 0x7F_FF0B reserved field should be programmed to 0xFF.

Table 25-28. FECCR Index=000 Bit Descriptions

Field	Description
15:8 PAR[7:0]	ECC Parity Bits — Contains the 8 parity bits from the 72 bit wide P-Flash data word or the 6 parity bits, allocated to PAR[5:0], from the 22 bit wide D-Flash word with PAR[7:6]=00.
7 XBUS01	Bus Source Identifier — The XBUS01 bit determines whether the ECC error was caused by a read access from the CPU or XGATE. 0 ECC Error happened on the CPU access 1 ECC Error happened on the XGATE access
6–0 GADDR[22:16]	Global Address — The GADDR[22:16] field contains the upper seven bits of the global address having caused the error.

The P-Flash word addressed by ECCRIX = 001 contains the lower 16 bits of the global address. The following four words addressed by ECCRIX = 010 to 101 contain the 64-bit wide data phrase. The four data words and the parity byte are the uncorrected data read from the P-Flash block.

The D-Flash word addressed by ECCRIX = 001 contains the lower 16 bits of the global address. The uncorrected 16-bit data word is addressed by ECCRIX = 010.

25.3.2.14 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

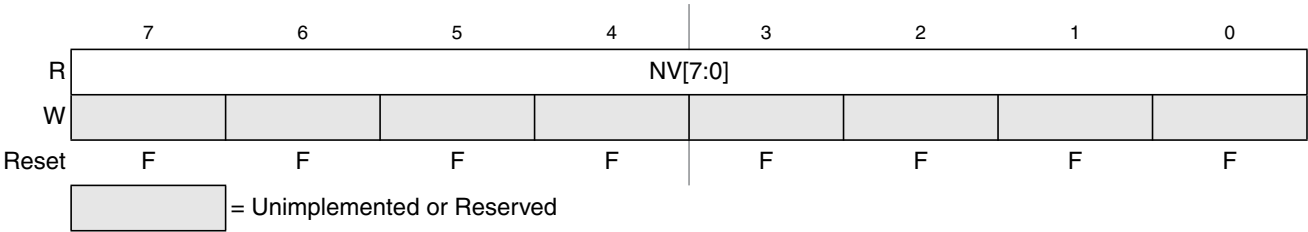


Figure 25-22. Flash Option Register (FOPT)

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x7F_FF0E located in P-Flash memory (see Table 25-3) as indicated by reset condition F in Figure 25-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 25-29. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	Nonvolatile Bits — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

25.3.2.15 Flash Reserved0 Register (FRSV0)

This Flash register is reserved for factory testing.

Table 26-70. Erase D-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 26-30)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the global address [22:0] points to the D-Flash EEE partition
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
FERSTAT	EPVIOLIF	None

26.4.2.19 Enable EEPROM Emulation Command

The Enable EEPROM Emulation command causes the Memory Controller to enable EEE activity. EEE activity is disabled after any reset.

Table 26-71. Enable EEPROM Emulation Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x13	Not required

Upon clearing CCIF to launch the Enable EEPROM Emulation command, the CCIF flag will set after the Memory Controller enables EEE operations using the contents of the EEE tag RAM and tag counter. The Full Partition D-Flash or the Partition D-Flash command must be run prior to launching the Enable EEPROM Emulation command.

Table 26-72. Enable EEPROM Emulation Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if Full Partition D-Flash or Partition D-Flash command not previously run
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None
FERSTAT	EPVIOLIF	None

Table 27-9. FDIV vs OSCCLK Frequency

OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]
MIN ⁽¹⁾	MAX ⁽²⁾		MIN ¹	MAX ²		MIN ¹	MAX ²	
			33.60	34.65	0x20	67.20	68.25	0x40
1.60	2.10	0x01	34.65	35.70	0x21	68.25	69.30	0x41
2.40	3.15	0x02	35.70	36.75	0x22	69.30	70.35	0x42
3.20	4.20	0x03	36.75	37.80	0x23	70.35	71.40	0x43
4.20	5.25	0x04	37.80	38.85	0x24	71.40	72.45	0x44
5.25	6.30	0x05	38.85	39.90	0x25	72.45	73.50	0x45
6.30	7.35	0x06	39.90	40.95	0x26	73.50	74.55	0x46
7.35	8.40	0x07	40.95	42.00	0x27	74.55	75.60	0x47
8.40	9.45	0x08	42.00	43.05	0x28	75.60	76.65	0x48
9.45	10.50	0x09	43.05	44.10	0x29	76.65	77.70	0x49
10.50	11.55	0x0A	44.10	45.15	0x2A	77.70	78.75	0x4A
11.55	12.60	0x0B	45.15	46.20	0x2B	78.75	79.80	0x4B
12.60	13.65	0x0C	46.20	47.25	0x2C	79.80	80.85	0x4C
13.65	14.70	0x0D	47.25	48.30	0x2D	80.85	81.90	0x4D
14.70	15.75	0x0E	48.30	49.35	0x2E	81.90	82.95	0x4E
15.75	16.80	0x0F	49.35	50.40	0x2F	82.95	84.00	0x4F
16.80	17.85	0x10	50.40	51.45	0x30	84.00	85.05	0x50
17.85	18.90	0x11	51.45	52.50	0x31	85.05	86.10	0x51
18.90	19.95	0x12	52.50	53.55	0x32	86.10	87.15	0x52
19.95	21.00	0x13	53.55	54.60	0x33	87.15	88.20	0x53
21.00	22.05	0x14	54.60	55.65	0x34	88.20	89.25	0x54
22.05	23.10	0x15	55.65	56.70	0x35	89.25	90.30	0x55
23.10	24.15	0x16	56.70	57.75	0x36	90.30	91.35	0x56
24.15	25.20	0x17	57.75	58.80	0x37	91.35	92.40	0x57
25.20	26.25	0x18	58.80	59.85	0x38	92.40	93.45	0x58
26.25	27.30	0x19	59.85	60.90	0x39	93.45	94.50	0x59
27.30	28.35	0x1A	60.90	61.95	0x3A	94.50	95.55	0x5A
28.35	29.40	0x1B	61.95	63.00	0x3B	95.55	96.60	0x5B
29.40	30.45	0x1C	63.00	64.05	0x3C	96.60	97.65	0x5C
30.45	31.50	0x1D	64.05	65.10	0x3D	97.65	98.70	0x5D
31.50	32.55	0x1E	65.10	66.15	0x3E	98.70	99.75	0x5E
32.55	33.60	0x1F	66.15	67.20	0x3F	99.75	100.80	0x5F

1. FDIV shown generates an FCLK frequency of >0.8 MHz

Table 27-38. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FERSTAT	EPVIOLIF	None

27.4.2.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash block 0. The Read Once field is programmed using the Program Once command described in [Section 27.4.2.7](#). The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 27-39. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required
001	Read Once phrase index (0x0000 - 0x0007)	
010	Read Once word 0 value	
011	Read Once word 1 value	
100	Read Once word 2 value	
101	Read Once word 3 value	

Upon clearing CCIF to launch the Read Once command, a Read Once phrase is fetched and stored in the FCCOB indexed register. The CCIF flag will set after the Read Once operation has completed. Valid phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

Table 27-40. Read Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 27-30)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

27.4.2.5 Load Data Field Command

The Load Data Field command is executed to provide FCCOB parameters for multiple P-Flash blocks for a future simultaneous program operation in the P-Flash memory space.

Offset Module Base + 0x000A

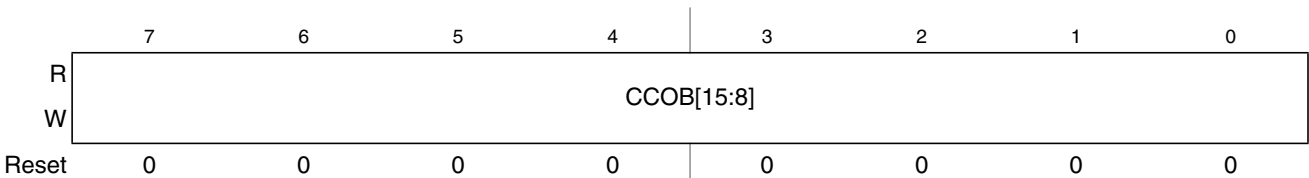


Figure 28-16. Flash Common Command Object High Register (FCCOBHI)

Offset Module Base + 0x000B

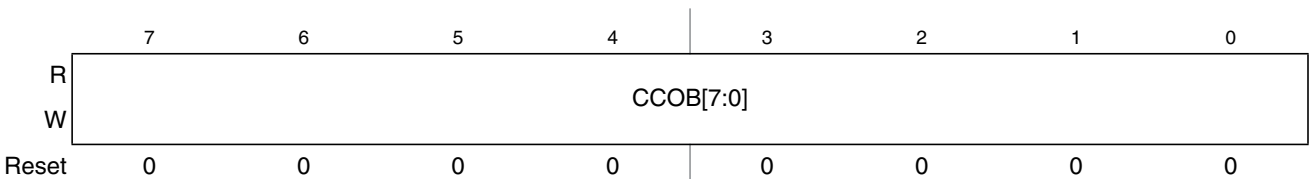


Figure 28-17. Flash Common Command Object Low Register (FCCOBLO)

28.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 28-26. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 28-26 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 28.4.2.

Table 28-26. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	0, Global address [22:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]

Table A-8. 5V I/O Characteristics

Conditions are $4.5\text{ V} < V_{DD35} < 5.5\text{ V}$ temperature from -40°C to $+150^{\circ}\text{C}$, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL, TEST and supply pins.							
16	D	Port H, J, P interrupt input pulse passed ($\overline{\text{STOP}}$)	t_{PULSE}	4	—	—	tcyc
17	D	$\overline{\text{IRQ}}$ pulse width, edge-sensitive mode ($\overline{\text{STOP}}$)	PW_{IRQ}	1	—	—	tcyc
18	D	$\overline{\text{XIRQ}}$ pulse width with X-bit set ($\overline{\text{STOP}}$)	PW_{XIRQ}	4	—	—	tosc

1. Maximum leakage current occurs at maximum operating temperature.
2. Refer to [Section A.1.4, “Current Injection”](#) for more details
3. Parameter only applies in stop or pseudo stop mode.

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{\max}(N)}{N \cdot t_{\text{nom}}}\right|, \left|1 - \frac{t_{\min}(N)}{N \cdot t_{\text{nom}}}\right|\right)$$

The following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

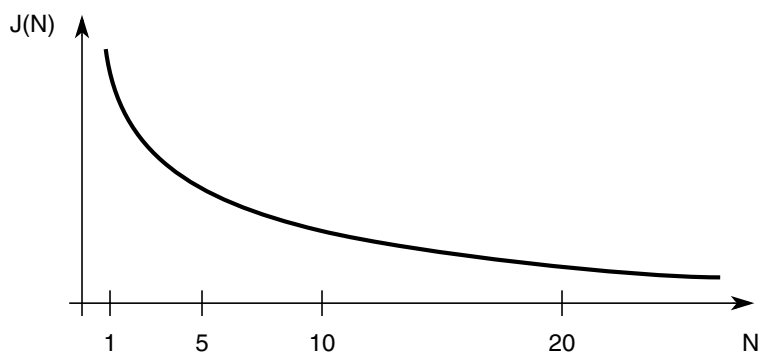


Figure A-6. Maximum bus clock jitter approximation

A.7.3.4 Emulation Expanded Mode (With Optional Access Stretching)

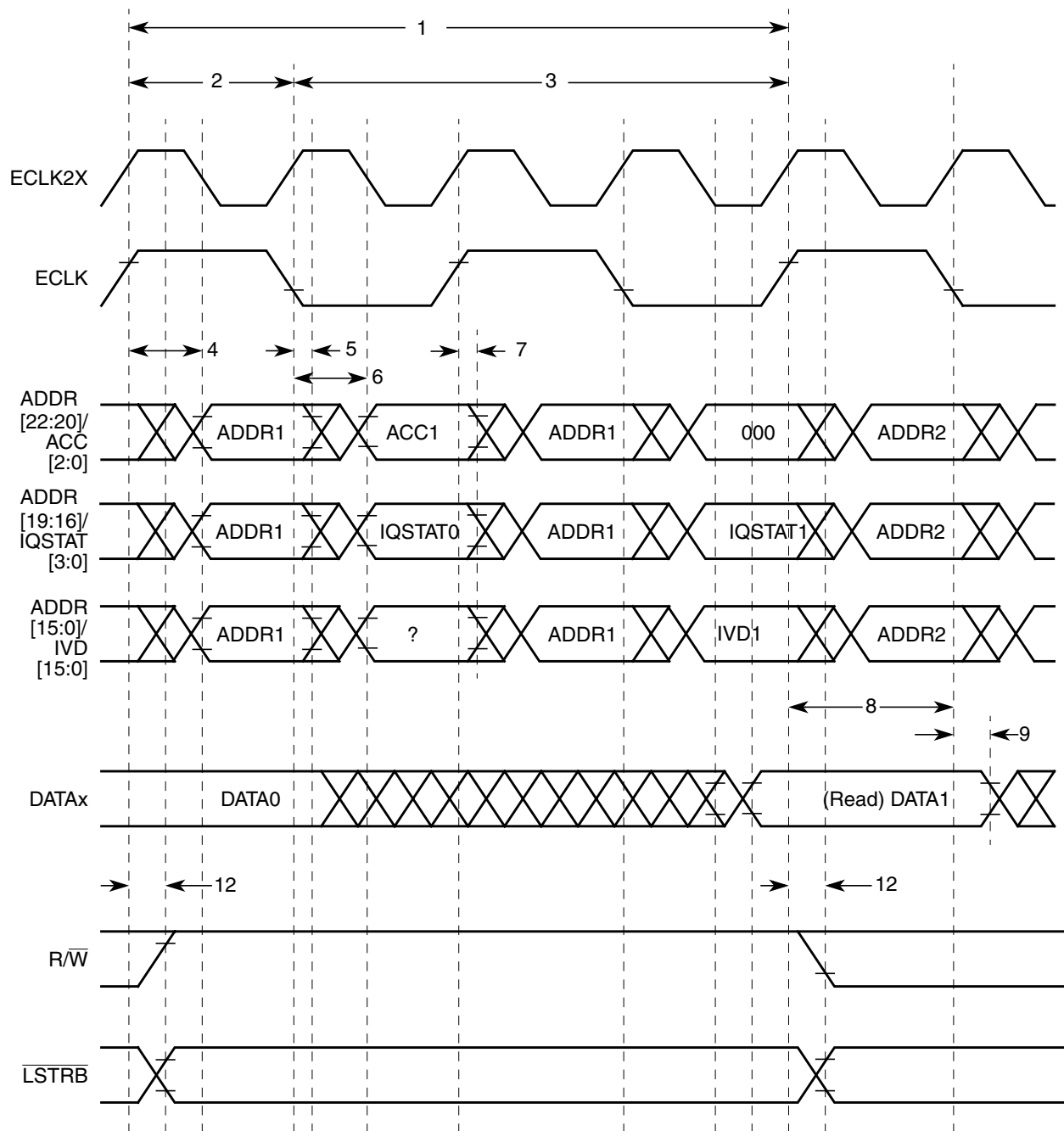


Figure A-16. Example 2b: Emulation Expanded Mode — Read with 1 Stretch Cycle

0x0080–0x00AF Analog-to-Digital Converter 12-bit 16-Channels (ATD1) Map (Sheet 2 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0096	ATD1DR3H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0097	ATD1DR3L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0098	ATD1DR4H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0099	ATD1DR4L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x009A	ATD1DR5H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009B	ATD1DR5L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x009C	ATD1DR6H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009D	ATD1DR6L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x009E	ATD1DR7H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009F	ATD1DR7L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A0	ATD1DR8H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A1	ATD1DR8L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A2	ATD1DR9H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A3	ATD1DR9L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A4	ATD1DR10H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A5	ATD1DR10L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A6	ATD1DR11H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A7	ATD1DR11L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00A8	ATD1DR12H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A9	ATD1DR12L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x00AA	ATD1DR13H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AB	ATD1DR13L	R	Bit7	Bit6	0	0	0	0	0	0
		W								