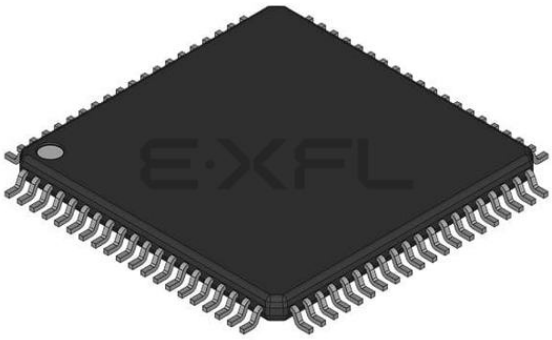

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912xet256bmaar

interrupt is level sensitive and active low. As XIRQ is level sensitive, while this pin is low the MCU will not enter STOP mode.

1.2.3.20 PF7 / TXD3 — Port F I/O Pin 7

PF7 is a general-purpose input or output pin. It can be configured as the transmit pin TXD of serial communication interface 3 (SCI3).

1.2.3.21 PF6 / RXD3 — Port F I/O Pin 6

PF6 is a general-purpose input or output pin. It can be configured as the transmit pin RXD of serial communication interface 3 (SCI3).

1.2.3.22 PF5 / SCL0 — Port F I/O Pin 5

PF5 is a general-purpose input or output pin. It can be configured as the serial clock pin SCL of the IIC0 module.

1.2.3.23 PF4 / SDA0 — Port F I/O Pin 4

PF4 is a general-purpose input or output pin. It can be configured as the serial data pin SDA of the IIC0 module.

1.2.3.24 PF[3:0] / $\overline{\text{CS}}$[3:0] — Port F I/O Pins 3 to 0

PF[3:0] are a general-purpose input or output pins. They can be configured as chip select outputs [3:0].

1.2.3.25 PH7 / KWH7 / $\overline{\text{SS2}}$ / TXD5 — Port H I/O Pin 7

PH7 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as slave select pin $\overline{\text{SS}}$ of the serial peripheral interface 2 (SPI2). It can be configured as the transmit pin TXD of serial communication interface 5 (SCI5).

1.2.3.26 PH6 / KWH6 / SCK2 / RXD5 — Port H I/O Pin 6

PH6 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as serial clock pin SCK of the serial peripheral interface 2 (SPI2). It can be configured as the receive pin (RXD) of serial communication interface 5 (SCI5).

1.2.3.27 PH5 / KWH5 / MOSI2 / TXD4 — Port H I/O Pin 5

PH5 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the serial peripheral interface 2 (SPI2). It can be configured as the transmit pin TXD of serial communication interface 4 (SCI4).

1.2.4.4 VDDF — NVM Power Pin

Power is supplied to the MCU NVM through VDDF . The voltage supply of nominally 2.8V is derived from the internal voltage regulator. No static external loading of these pins is permitted.

1.2.4.5 VDDA2, VDDA1, VSSA2, VSSA1 — Power Supply Pins for ATD and Voltage Regulator

These are the power supply and ground input pins for the analog-to-digital converters and the voltage regulator. Internally the V_{DDA} pins are connected together. Internally the V_{SSA} pins are connected together.

1.2.4.6 VRH, VRL — ATD Reference Voltage Input Pins

V_{RH} and V_{RL} are the reference voltage input pins for the analog-to-digital converter.

1.2.4.7 VDDPLL, VSSPL — Power Supply Pins for PLL

These pins provide operating voltage and ground for the oscillator and the phased-locked loop. The voltage supply of nominally 1.8V is derived from the internal voltage regulator. This allows the supply voltage to the oscillator and PLL to be bypassed independently. This voltage is generated by the internal voltage regulator. No static external loading of these pins is permitted.

Table 1-11. Power and Ground Connection Summary

Mnemonic	Nominal Voltage	Description
VDDR	5.0 V	External power supply to internal voltage regulator
VDDX[7:1]	5.0 V	External power and ground, supply to pin drivers
VSSX[7:1]	0 V	
VDDA2, VDDA1	5.0 V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA2, VSSA1	0 V	
VRL	0 V	Reference voltages for the analog-to-digital converter.
VRH	5.0 V	
VDD	1.8 V	Internal power and ground generated by internal regulator for the internal core.
VSS1, VSS2, VSS3	0V	
VDDF	2.8 V	Internal power and ground generated by internal regulator for the internal NVM.

2.3.1 Memory Map

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
	W								
0x0001 PORTB	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
	W								
0x0002 DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
	W								
0x0003 DDRB	R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
	W								
0x0004 PORTC	R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	W								
0x0005 PORTD	R	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	W								
0x0006 DDRC	R	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
	W								
0x0007 DDRD	R	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
	W								
0x0008 PORTE	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	W								
0x0009 DDRE	R	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	0	0
	W								
0x000A 0x000B Non-PIM Address Range	R	Non-PIM Address Range							
	W								
0x000C PUCR	R	PUPKE	BKPUE	0	PUPEE	PUPDE	PUPCE	PUPBE	PUPAE
	W								
0x000D RDRIV	R	RDPK	0	0	RDPE	RDPD	RDPC	RDPB	RDPA
	W								

= Unimplemented or Reserved

Table 2-87. PTR Routing Register Field Descriptions (continued)

Field	Description
5 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC5 is available on PP5 0 TIMIOC5 is available on PR5
4 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC4 is available on PP4 0 TIMIOC4 is available on PR4
3 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC3 is available on PP3 0 TIMIOC3 is available on PR3
2 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC2 is available on PP2 0 TIMIOC2 is available on PR2
1 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC1 is available on PP1 0 TIMIOC1 is available on PR1
0 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC0 is available on PP0 0 TIMIOC0 is available on PR0

2.3.93 Port L Data Register (PTL)

Address 0x0370 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PTL7	PTLT6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
Altern. Function	(TXD7)	(RXD7)	(TXD6)	(RXD6)	(TXD5)	(RXD5)	(TXD4)	(RXD4)
Reset	0	0	0	0	0	0	0	0

Figure 2-91. Port L Data Register (PTL)

1. Read: Anytime.
   Write: Anytime.

Chapter 4
Memory Protection Unit (S12XMPUV1)

Table 4-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.04	14 Sep 2005	4.3.1.1/4-231 4.4.1/4-237	- Added note to only use the CPU to clear the AE flag. - Added disclaimer to avoid changing descriptors while they are in use because of other bus-masters doing accesses.
V01.05	14 Mar 2006	4.3.1.1/4-231 4.4/4-237	- Clarified that interrupt generation is independent of AEF bit state. - Corrected preliminary statement about execution of violating accesses.
V01.06	09 Oct 2006		- Made Revision History entries public.

4.1 Introduction

The MPU module provides basic functionality required to protect memory mapped resources from undesired accesses. Multiple address range comparators compare memory accesses against eight memory protection descriptors located in the MPU module to determine if each access is valid or not. The comparison is sensitive to which bus master generates the access and the type of the access.

The MPU module can be used to isolate memory ranges accessible by different bus masters. It can be also be used by an operating system or software kernel to isolate the regions of memory “legally” available to specific software tasks, with the kernel re-configuring the task specific memory protection descriptors in supervisor state during task-switching.

4.1.1 Preface

The following terms and abbreviations are used in the document.

Table 4-2. Terminology

Term	Meaning
MCU	Micro-Controller Unit
MPU	Memory Protection Unit
CPU	S12X Central Processing Unit (see S12XCPU Reference Manual)
XGATE	XGATE Co-processor (see XGATE chapter)
supervisor state	refers to the supervisor state of the S12XCPU (see S12XCPU Reference Manual)
user state	refers to the user state of the S12XCPU (see S12XCPU Reference Manual)

4.1.2 Overview

The MPU module monitors the bus activity of each bus master. The data describing each access is fed into multiple address range comparators. The output of the comparators is used to determine if a particular

ORH — Logical OR Immediate 8 bit Constant (High Byte) — ORH

Operation

RD.H | IMM8 ⇒ RD.H

Performs a bit wise logical OR between the high byte of register RD and an immediate 8 bit constant and stores the result in the destination register RD.H. The low byte of RD is not affected.

CCR Effects

N	Z	V	C
Δ	Δ	0	—

N: Set if bit 15 of the result is set; cleared otherwise.
Z: Set if the 8 bit result is $00; cleared otherwise.
V: 0; cleared.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code							Cycles
ORH RD, #IMM8	IMM8	1	0	1	0	1	RD	IMM8	P

STW Store Word to Memory STW

Operation

RS ⇒ M[RB, #OFFS5]
RS ⇒ M[RB, RI]
RS ⇒ M[RB, RI]; RI+2 ⇒ RI;
RI–2 ⇒ RI; RS ⇒ M[RB, RI][1]

Stores the content of register RS to memory.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code										Cycles
STW RS, (RB, #OFFS5)	IDO5	0	1	0	1	1	RS	RB	OFFS5			PW
STW RS, (RB, RI)	IDR	0	1	1	1	1	RS	RB	RI	0	0	PW
STW RS, (RB, RI+)	IDR+	0	1	1	1	1	RS	RB	RI	0	1	PW
STW RS, (RB, -RI)	-IDR	0	1	1	1	1	RS	RB	RI	1	0	PW

1. If the same general purpose register is used as index (RI) and source register (RS), the unmodified content of the source register is written to the memory: RS ⇒ M[RB, RS–2]; RS–2 ⇒ RS

Field	Description
6–3 S8C, S4C, S2C, S1C	**Conversion Sequence Length** — These bits control the number of conversions per sequence. Table 13-11 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.
2 FIFO	**Result Register FIFO Mode** — If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register (ATDDR0), the second result in the second result register (ATDDR1), and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or ending of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC3-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data. If this bit is one, automatic compare of result registers is always disabled, that is ADC12B16C will behave as if ACMPIE and all CPME[*n*] were zero. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1–0 FRZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 13-12. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Table 13-9. ATDCTL3 Field Descriptions (continued)

Table 13-10. Examples of ideal decimal ATD Results

Input Signal V_{RL} = 0 Volts V_{RH} = 5.12 Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	12-Bit Codes (transfer curve has 1.25mV offset) (resolution=1.25mV)
5.120 Volts	255	1023	4095
...	...	...	...
0.022	1	4	17
0.020	1	4	16
0.018	1	4	14
0.016	1	3	12
0.014	1	3	11
0.012	1	2	9
0.010	1	2	8
0.008	0	2	6
0.006	0	1	4
0.004	0	1	3
0.003	0	0	2
0.002	0	0	1
0.000	0	0	0

Table 15-7. IIC Divider and Hold Values (Sheet 6 of 6)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
AC	2304	388	1144	1156
AD	2560	388	1272	1284
AE	3072	516	1528	1540
AF	3840	516	1912	1924
B0	2560	260	1272	1284
B1	3072	260	1528	1540
B2	3584	516	1784	1796
B3	4096	516	2040	2052
B4	4608	772	2296	2308
B5	5120	772	2552	2564
B6	6144	1028	3064	3076
B7	7680	1028	3832	3844
B8	5120	516	2552	2564
B9	6144	516	3064	3076
BA	7168	1028	3576	3588
BB	8192	1028	4088	4100
BC	9216	1540	4600	4612
BD	10240	1540	5112	5124
BE	12288	2052	6136	6148
BF	15360	2052	7672	7684

15.3.1.3 IIC Control Register (IBCR)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	IBEN	IBIE	MS/SL	Tx/Rx	TXAK	0	0	IBSWAI
W						RSTA		
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-6. IIC Bus Control Register (IBCR)

Read and write anytime

17.4.1 Timer

As shown in Figure 17-1 and Figure 17-27, the 24-bit timers are built in a two-stage architecture with eight 16-bit modulus down-counters and two 8-bit modulus down-counters. The 16-bit timers are clocked with two selectable micro time bases which are generated with 8-bit modulus down-counters. Each 16-bit timer is connected to micro time base 0 or 1 via the PMUX[7:0] bit setting in the PIT Multiplex (PITMUX) register.

A timer channel is enabled if the module enable bit PITE in the PIT control and force load micro timer (PITCFLMT) register is set and if the corresponding PCE bit in the PIT channel enable (PITCE) register is set. Two 8-bit modulus down-counters are used to generate two micro time bases. As soon as a micro time base is selected for an enabled timer channel, the corresponding micro timer modulus down-counter will load its start value as specified in the PITMTLD0 or PITMTLD1 register and will start down-counting. Whenever the micro timer down-counter has counted to zero the PITMTLD register is reloaded and the connected 16-bit modulus down-counters count one cycle.

Whenever a 16-bit timer counter and the connected 8-bit micro timer counter have counted to zero, the PITLD register is reloaded and the corresponding time-out flag PTF in the PIT time-out flag (PITTF) register is set, as shown in Figure 17-28. The time-out period is a function of the timer load (PITLD) and micro timer load (PITMTLD) registers and the bus clock f_{BUS}:

time-out period = (PITMTLD + 1) * (PITLD + 1) / f_{BUS}.

For example, for a 40 MHz bus clock, the maximum time-out period equals:

256 * 65536 * 25 ns = 419.43 ms.

The current 16-bit modulus down-counter value can be read via the PITCNT register. The micro timer down-counter values cannot be read.

The 8-bit micro timers can individually be restarted by writing a one to the corresponding force load micro timer PFLMT bits in the PIT control and force load micro timer (PITCFLMT) register. The 16-bit timers can individually be restarted by writing a one to the corresponding force load timer PFLT bits in the PIT forceload timer (PITFLT) register. If desired, any group of timers and micro timers can be restarted at the same time by using one 16-bit write to the adjacent PITCFLMT and PITFLT registers with the relevant bits set, as shown in Figure 17-28.

Figure 20-26 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

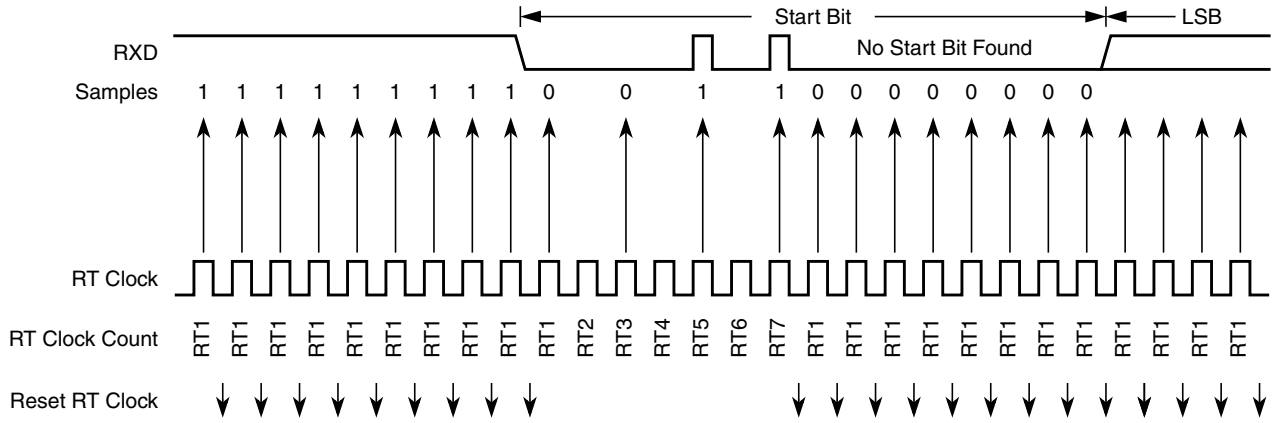


Figure 20-26. Start Bit Search Example 5

In Figure 20-27, a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

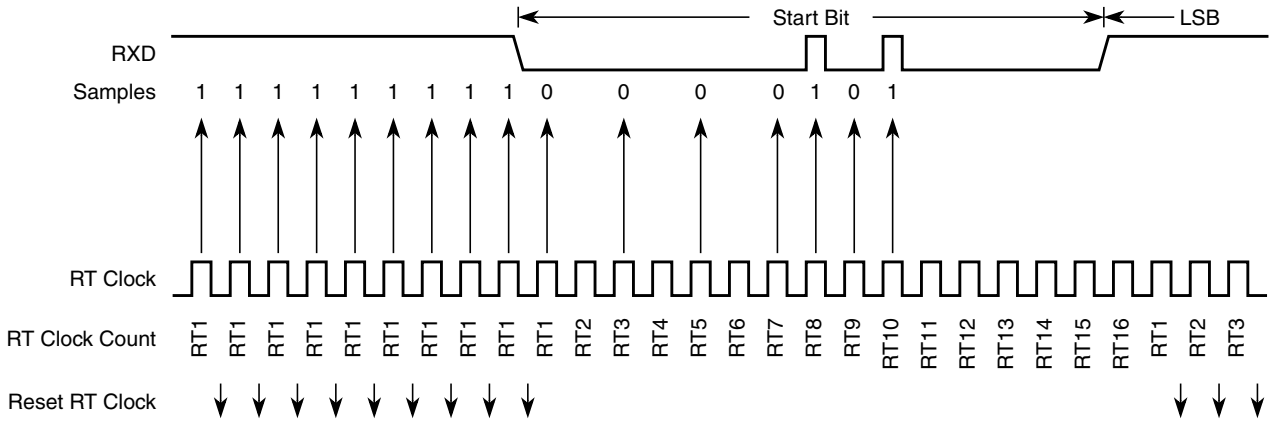


Figure 20-27. Start Bit Search Example 6

20.4.6.4 Framing Errors

If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming frame, it sets the framing error flag, FE, in SCI status register 1 (SCISR1). A break character also sets the FE flag because a break character has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

- Program ERPART to the EEE nonvolatile information register at global address 0x12_0004 (see Table 24-7)
- Program a duplicate ERPART to the EEE nonvolatile information register at global address 0x12_0006 (see Table 24-7)

The D-Flash user partition will start at global address 0x10_0000. The buffer RAM EEE partition will end at global address 0x13_FFFF. After the Partition D-Flash operation has completed, the CCIF flag will set.

Running the Partition D-Flash command a second time will result in the ACCERR bit within the FSTAT register being set. The data value written corresponds to the number of 256 byte sectors allocated for either direct D-Flash access (DFPART) or buffer RAM EEE access (ERPART).

Table 24-76. Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 24-30)
		Set if partitions have already been defined
		Set if an invalid DFPART or ERPART selection is supplied(1)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

1. As defined by the maximum ERPART for FTM256K2.

2. FDIV shown generates an FCLK frequency of 1.05 MHz

26.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Offset Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	KEYEN[1:0]		RNV[5:2]				SEC[1:0]	
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 26-6. Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x7F_FF0F located in P-Flash memory (see Table 26-3) as indicated by reset condition F in Figure 26-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 26-10. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 26-11.
5–2 RNV[5:2}	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 26-12. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 26-11. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED(1)
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

Chapter 28
768 KByte Flash Module (S12XFTM768K4V2)

Table 28-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.09	29 Nov 2007		- Cleanup
V02.10	19 Dec 2007	28.4.2/28-1113 28.4.2/28-1113 28.3.1/28-1082	- Updated Command Error Handling tables based on parent-child relationship with FTM1024K5 - Corrected Error Handling table for Full Partition D-Flash, Partition D-Flash, and EEPROM Emulation Query commands - Corrected P-Flash Memory Addressing table
V02.11	25 Sep 2009	28.1/28-1077 28.3.2.1/28-1089 28.4.2.4/28-1116 28.4.2.7/28-1119 28.4.2.12/28-1123 28.4.2.12/28-1123 28.4.2.12/28-1123 28.4.2.20/28-1132 28.3.2/28-1087 28.3.2.1/28-1089 28.4.1.2/28-1108 28.6/28-1138	- Clarify single bit fault correction for P-Flash phrase - Expand FDIV vs OSCCLK Frequency table - Add statement concerning code runaway when executing Read Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Program Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Verify Backdoor Access Key command from Flash block containing associated fields - Relate Key 0 to associated Backdoor Comparison Key address - Change “power down reset” to “reset” - Add ACCERR condition for Disable EEPROM Emulation command The following changes were made to clarify module behavior related to Flash register access during reset sequence and while Flash commands are active: - Add caution concerning register writes while command is active - Writes to FCLKDIV are allowed during reset sequence while CCIF is clear - Add caution concerning register writes while command is active - Writes to FCCOBIX, FCCOBHI, FCCOBLO registers are ignored during reset sequence

28.1 Introduction

The FTM768K4 module implements the following:

- 768 Kbytes of P-Flash (Program Flash) memory, consisting of 4 physical Flash blocks, intended primarily for nonvolatile code storage

Table 28-36. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if an invalid global address [22:16] is supplied(1)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read(2)
	MGSTAT0	Set if any non-correctable errors have been encountered during the read2
FERSTAT	EPVIOLIF	None

1. As defined by the memory map for FTM1024K5.
2. As found in the memory map for FTM1024K5.

28.4.2.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases. The section to be verified cannot cross a 256 Kbyte boundary in the P-Flash memory space.

Table 28-37. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [22:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed.

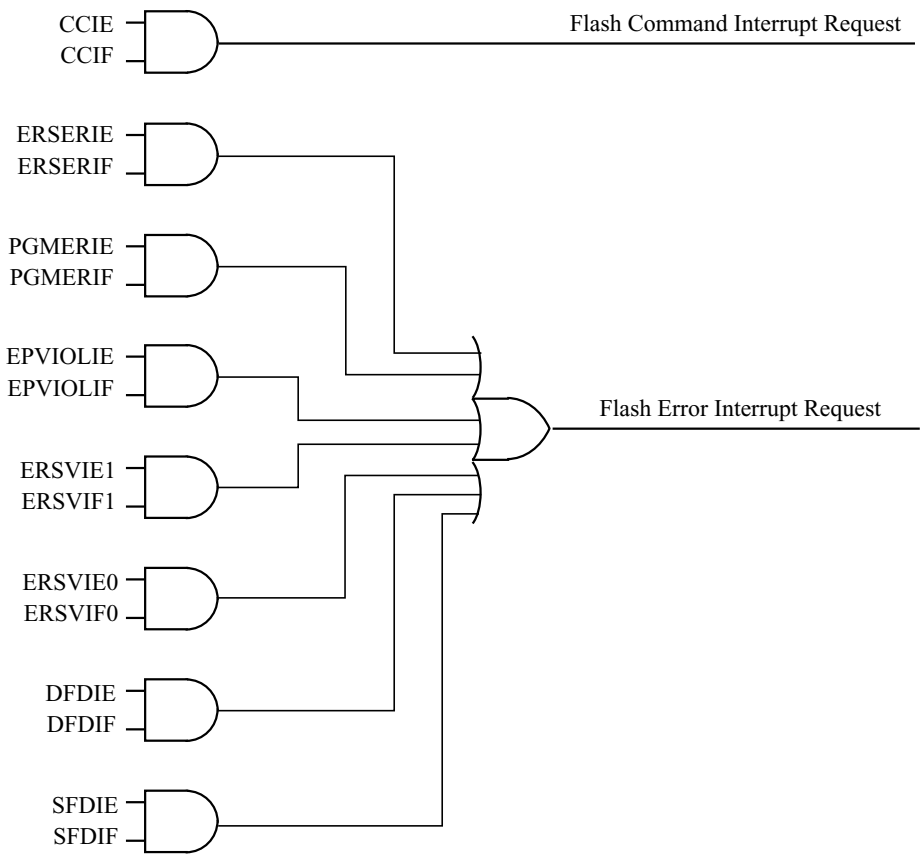


Figure 29-27. Flash Module Interrupts Implementation

29.4.4 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 29.4.3, “Interrupts”).

29.4.5 Stop Mode

If a Flash command is active (CCIF = 0) or an EE-Emulation operation is pending when the MCU requests stop mode, the current Flash operation will be completed before the CPU is allowed to enter stop mode.

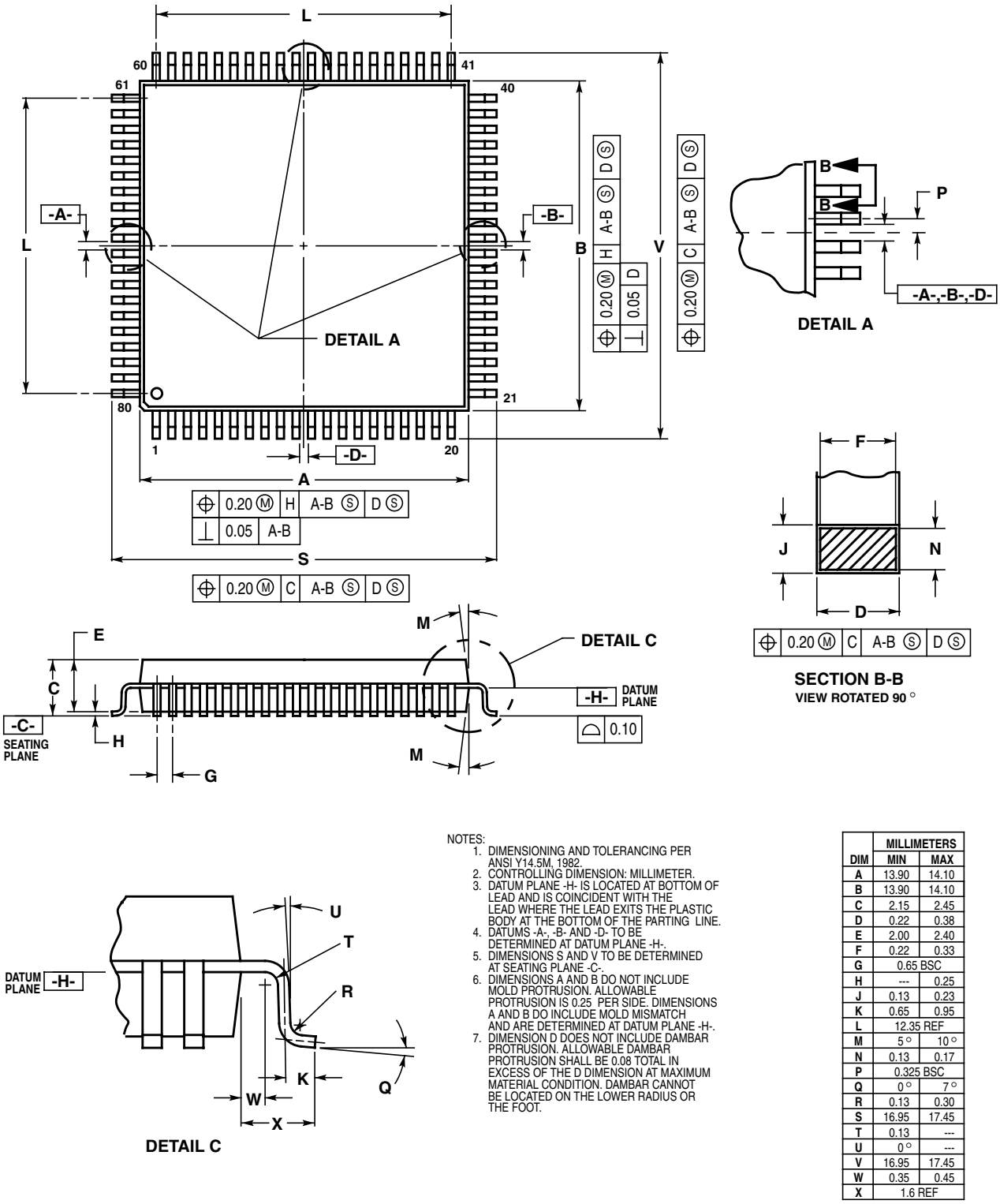
29.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 29-12). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x7F_FF0F.

Table A-8. 5V I/O Characteristics

Conditions are 4.5 V < V_{DD35} < 5.5 V temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input high voltage	V_{IH}	0.65*V_{DD35}	—	—	V
	T	Input high voltage	V_{IH}	—	—	V_{DD35} + 0.3	V
2	P	Input low voltage	V_{IL}	—	—	0.35*V_{DD35}	V
	T	Input low voltage	V_{IL}	V_{SS35} – 0.3	—	—	V
3	T	Input hysteresis	V_{HYS}	—	250	—	mV
4a	P	Input leakage current (pins in high impedance input mode)[1] V_{in} = V_{DD35} or V_{SS35} **M** Temperature range -40°C to 150°C **V** Temperature range -40°C to 130°C **C** Temperature range -40°C to 110°C	I_{in}	 –1 –0.75 –0.5	 — — —	 1 0.75 0.5	µA
4b	C	Input leakage current (pins in high impedance input mode) V_{in} = V_{DD35} or V_{SS35} -40°C 27°C 70°C 85°C 100°C 105°C 110°C 120°C 125°C 130°C 150°C	I_{in}	—	— — ±1 ±1 ±8 ±14 ±26 ±32 40 ±60 ±74 ±92 ±240	—	nA
5	C	Output high voltage (pins in output mode) Partial drive I_{OH} = –2 mA	V_{OH}	V_{DD35} – 0.8	—	—	V
6	P	Output high voltage (pins in output mode) Full drive I_{OH} = –10 mA	V_{OH}	V_{DD35} – 0.8	—	—	V
7	C	Output low voltage (pins in output mode) Partial drive I_{OL} = +2 mA	V_{OL}	—	—	0.8	V
8	P	Output low voltage (pins in output mode) Full drive I_{OL} = +10 mA	V_{OL}	—	—	0.8	V
9	P	Internal pull up resistance V_{IH} min > input voltage > V_{IL} max	R_{PUL}	25	—	50	KΩ
10	P	Internal pull down resistance V_{IH} min > input voltage > V_{IL} max	R_{PDH}	25	—	50	KΩ
11	D	Input capacitance	C_{in}	—	6	—	pF
12	T	Injection current[2] Single pin limit Total device Limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA
13	P	Port H, J, P interrupt input pulse filtered(STOP)[3]	t_{PULSE}	—	—	3	µs
14	P	Port H, J, P interrupt input pulse passed(STOP)[3]	t_{PULSE}	10	—	—	µs
15	D	Port H, J, P interrupt input pulse filtered ($\overline{STOP}$)	t_{PULSE}	—	—	3	tcyc

B.4 80-Pin QFP Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure B-4. 80-Pin QFP Mechanical Dimensions (Case No. 841B)

0x01C0–0x01FF MSCAN (CAN2) Map (Sheet 3 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01DF	CAN2IDMR7	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01E0– 0x01EF	CAN2RXFG	R	FOREGROUND RECEIVE BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								
0x01F0– 0x01FF	CAN2TXFG	R	FOREGROUND TRANSMIT BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								

0x03C0–0x03CF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03C0 -0x03CF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x03D0–0x03FF Timer Module (TIM) Map (Sheet 1 of 2)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03D0	TIOS	R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		W								
0x03D1	CFORC	R	0	0	0	0	0	0	0	0
		W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
0x03D2	OC7M	R	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		W								
0x03D3	OC7D	R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		W								
0x03D4	TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
		W								
0x03D5	TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
		W								
0x03D6	TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
		W								
0x03D7	TTOV	R	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		W								
0x03D8	TCTL1	R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		W								
0x03D9	TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		W								
0x03DA	TCTL3	R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		W								
0x03DB	TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		W								
0x03DC	TIE	R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		W								
0x03DD	TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
		W								
0x03DE	TFLG1	R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		W								
0x03DF	TFLG2	R	TOF	0	0	0	0	0	0	0
		W								
0x03E0	TC0H	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x03E1	TC0L	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x03E2	TC1H	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x03E3	TC1L	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								