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Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xet256j2cal



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1.1.3 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12XE-Family devices

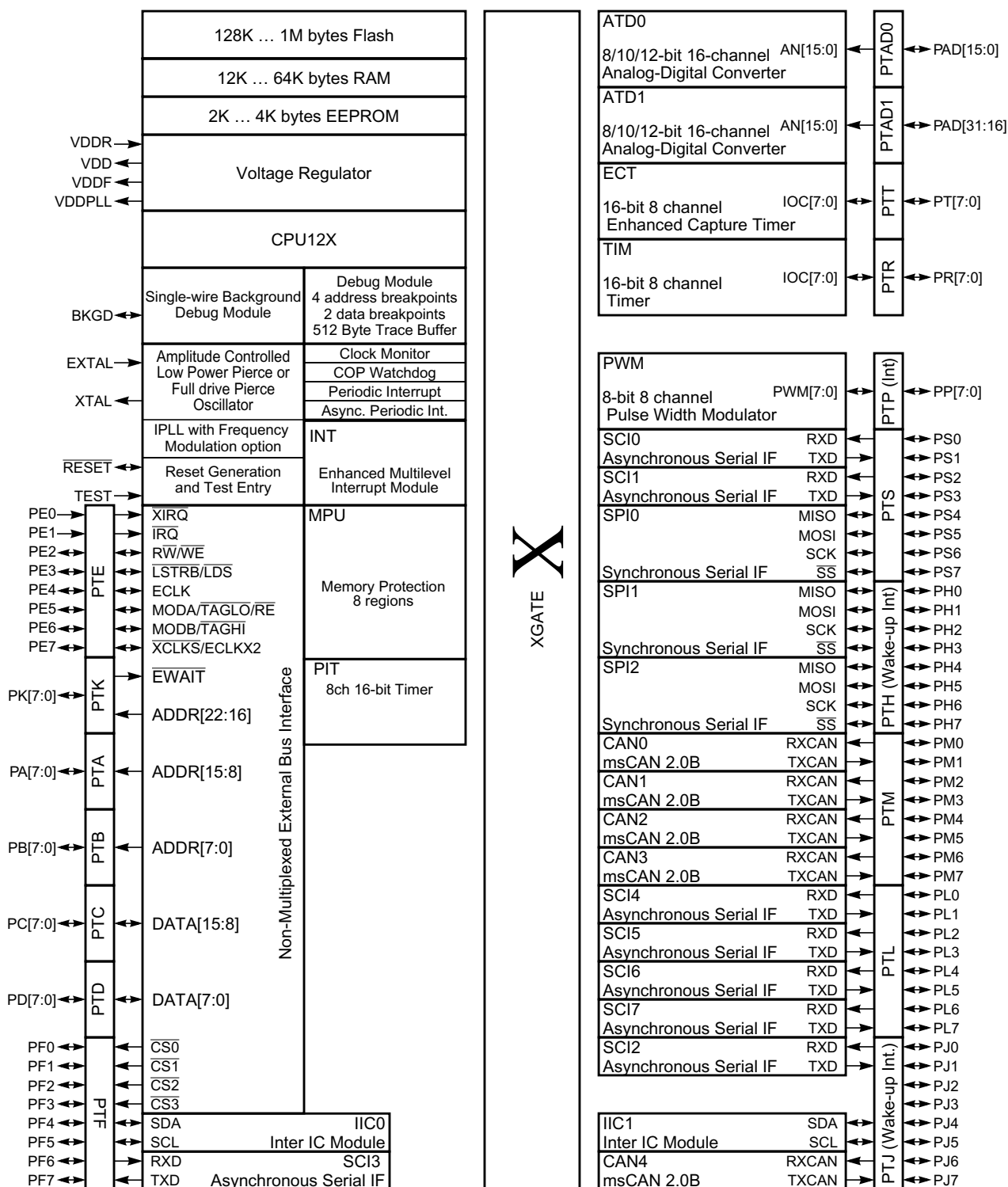


Figure 1-1. MC9S12XE-Family Block Diagram

The fixed 16K page from 0x4000–0x7FFF (when ROMHM = 0) is the page number 0xFD.

The reset value of 0xFE ensures that there is linear Flash space available between addresses 0x4000 and 0xFFFF out of reset.

The fixed 16K page from 0xC000-0xFFFF is the page number 0xFF.

3.3.2.7 RAM Page Index Register (RPAGE)

Address: 0x0016

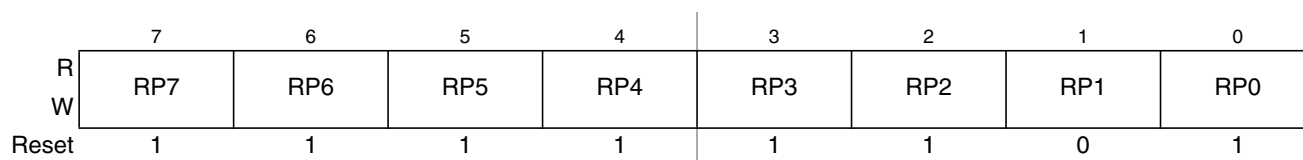


Figure 3-13. RAM Page Index Register (RPAGE)

Read: Anytime

Write: Anytime

These eight index bits are used to page 4 KByte blocks into the RAM page window located in the local (CPU or BDM) memory map from address 0x1000 to address 0x1FFF (see [Figure 3-14](#)). This supports accessing up to 1022 KByte of RAM (in the Global map) within the 64 KByte Local map. The RAM page index register is effectively used to construct paged RAM addresses in the Local map format.

CAUTION

XGATE write access to this register during an CPU access which makes use of this register could lead to unexpected results.

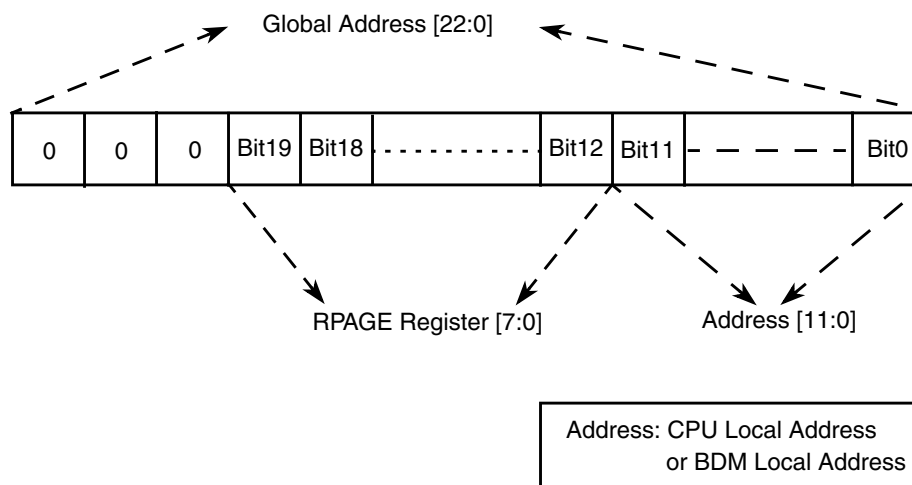


Figure 3-14. RPAGE Address Mapping

NOTE

Because RAM page 0 has the same global address as the register space, it is possible to write to registers through the RAM space when RPAGE = 0x00.

SUBH

Subtract Immediate 8 bit Constant
(High Byte)

SUBH

Operation

$RD - IMM8: \$00 \Rightarrow RD$

Subtracts a signed immediate 8 bit constant from the content of high byte of register RD and using binary subtraction and stores the result in the high byte of destination register RD. This instruction can be used after an SUBL for a 16 bit immediate subtraction.

Example:

```
SUBL    R2, #LOWBYTE
SUBH    R2, #HIGHBYTE      ; R2 = R2 - 16 bit immediate
```

CCR Effects

N	Z	V	C
Δ	Δ	Δ	Δ

- N: Set if bit 15 of the result is set; cleared otherwise.
- Z: Set if the result is \$0000; cleared otherwise.
- V: Set if a two’s complement overflow resulted from the operation; cleared otherwise.
 $RD[15]_{old} \& IMM8[7] \& \overline{RD[15]_{new}} \mid \overline{RD[15]_{old}} \& IMM8[7] \& RD[15]_{new}$
- C: Set if there is a carry from the bit 15 of the result; cleared otherwise.
 $\overline{RD[15]_{old}} \& IMM8[7] \mid \overline{RD[15]_{old}} \& RD[15]_{new} \mid IMM8[7] \& RD[15]_{new}$

Code and CPU Cycles

Source Form	Address Mode	Machine Code						Cycles
SUBH RD, #IMM8	IMM8	1	1	0	0	1	RD IMM8	P

Table 13-11. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 13-12. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

13.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004

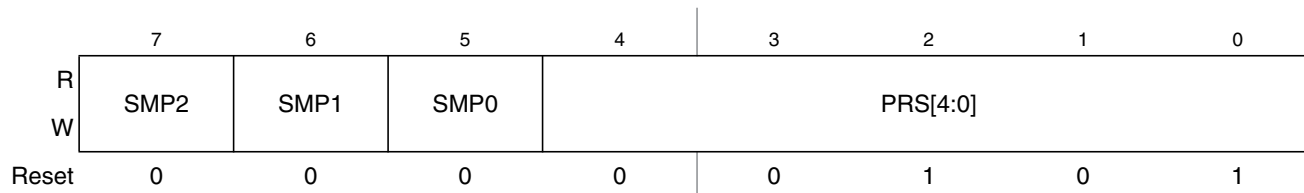


Figure 13-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output code.

13.4.2 Digital Sub-Block

This subsection explains some of the digital features in more detail. See [Section 13.3.2, “Register Descriptions”](#) for all details.

13.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The external trigger signal (out of reset ATD channel 15, configurable in ATDCTL1) is programmable to be edge or level sensitive with polarity control. [Table 13-23](#) gives a brief description of the different combinations of control bits and their effect on the external trigger function.

Table 13-23. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	X	Rising edge triggered. Performs one conversion sequence per trigger.
1	0	1	X	Trigger active low. Performs continuous conversions while trigger is active.
1	1	1	X	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received.

Once ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

Module Base + 0x00X2

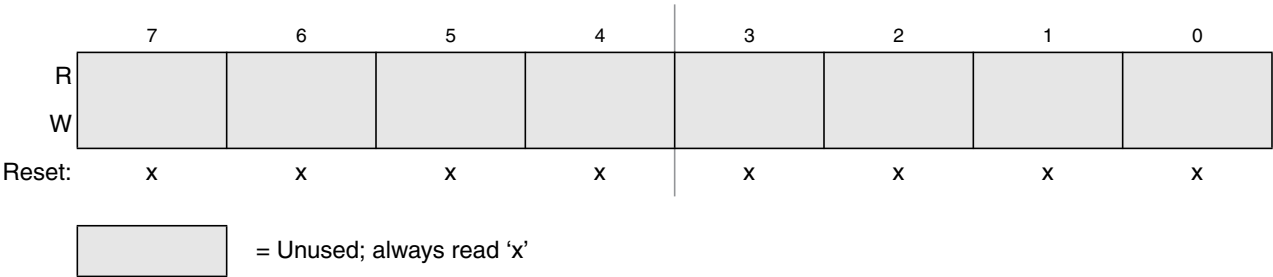


Figure 16-32. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

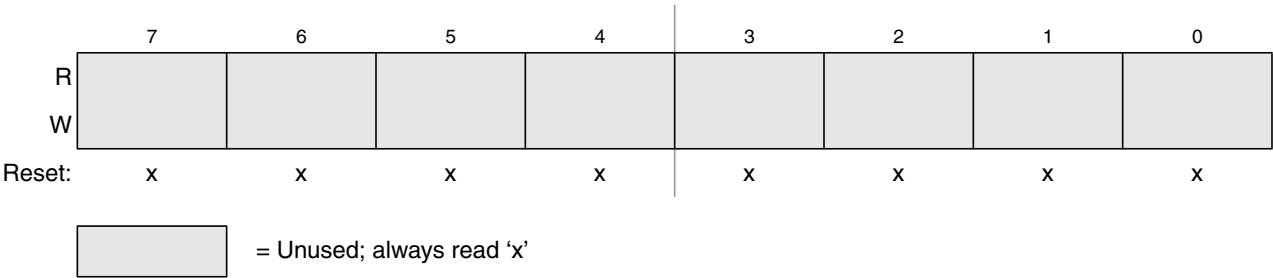


Figure 16-33. Identifier Register 3 — Standard Mapping

16.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

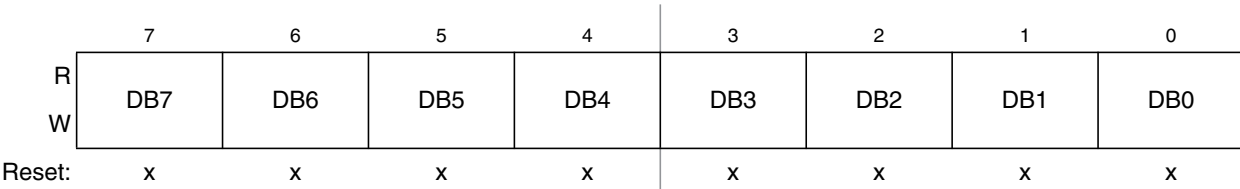


Figure 16-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 16-33. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	Data bits 7-0

20.3.2.5 SCI Alternative Control Register 2 (SCIACR2)

Module Base + 0x0002

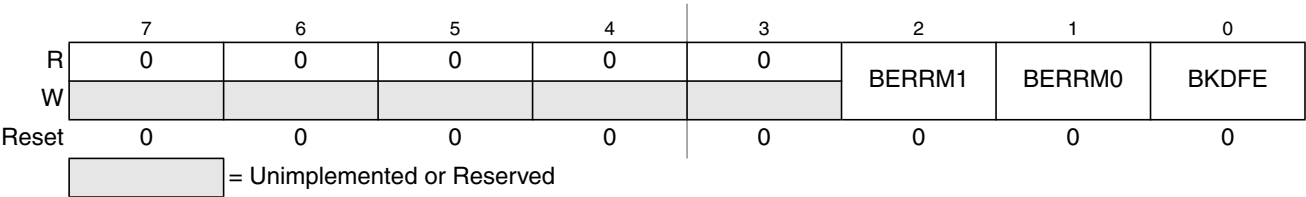


Figure 20-8. SCI Alternative Control Register 2 (SCIACR2)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 20-8. SCIACR2 Field Descriptions

Field	Description
2:1 BERRM[1:0]	Bit Error Mode — Those two bits determines the functionality of the bit error detect feature. See Table 20-9 .
0 BKDFE	Break Detect Feature Enable — BKDFE enables the break detect circuitry. 0 Break detect circuit disabled 1 Break detect circuit enabled

Table 20-9. Bit Error Mode Coding

BERRM1	BERRM0	Function
0	0	Bit error detect circuit is disabled
0	1	Receive input sampling occurs during the 9th time tick of a transmitted bit (refer to Figure 20-19)
1	0	Receive input sampling occurs during the 13th time tick of a transmitted bit (refer to Figure 20-19)
1	1	Reserved

Chapter 21

Serial Peripheral Interface (S12SPIV5)

Table 21-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V05.00	24 Mar 2005	21.3.2/21-765	- Added 16-bit transfer width feature.

21.1 Introduction

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or the SPI operation can be interrupt driven.

21.1.1 Glossary of Terms

SPI	Serial Peripheral Interface
SS	Slave Select
SCK	Serial Clock
MOSI	Master Output, Slave Input
MISO	Master Input, Slave Output
MOMI	Master Output, Master Input
SISO	Slave Input, Slave Output

21.1.2 Features

The SPI includes these distinctive features:

- Master mode and slave mode
- Selectable 8 or 16-bit transfer width
- Bidirectional mode
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- Control of SPI operation during wait mode

21.1.3 Modes of Operation

The SPI functions in three modes: run, wait, and stop.

Table 21-2. SPICR1 Field Descriptions (continued)

Field	Description
1 SSOE	Slave Select Output Enable — The \overline{SS} output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 21-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	LSB-First Enable — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in the highest bit position. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 21-3. \overline{SS} Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	\overline{SS} not used by SPI	\overline{SS} input
0	1	\overline{SS} not used by SPI	\overline{SS} input
1	0	\overline{SS} input with MODF feature	\overline{SS} input
1	1	\overline{SS} is slave select output	\overline{SS} input

21.3.2.2 SPI Control Register 2 (SPICR2)

Module Base +0x0001

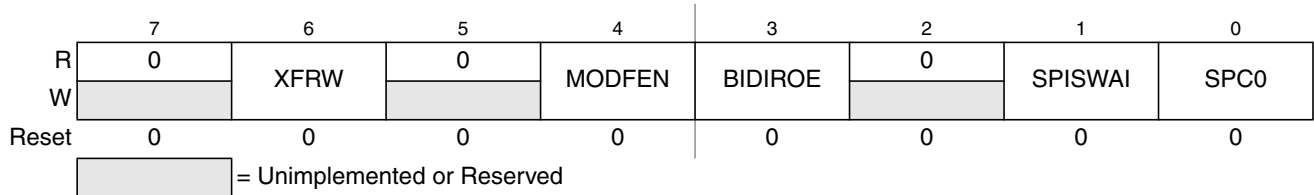


Figure 21-4. SPI Control Register 2 (SPICR2)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 22-19. Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

NOTE

If the timer is not active (TEN = 0 in TSCR), there is no divide-by-64 because the ÷64 clock is generated by the timer prescaler.

Table 22-20. Timer Clock Selection

CLK1	CLK0	Timer Clock
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PCLK as input to timer counter clock
1	0	Use PCLK/256 as timer counter clock frequency
1	1	Use PCLK/65536 as timer counter clock frequency

For the description of PCLK please refer [Figure 22-30](#).

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

22.3.2.16 Pulse Accumulator Flag Register (PAFLG)

Module Base + 0x0021

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
Reset	0	0	0	0	0	0	0	0
	Unimplemented or Reserved							

Figure 22-25. Pulse Accumulator Flag Register (PAFLG)

Read: Anytime

Write: Anytime

When the TFFCA bit in the TSCR register is set, any access to the PACNT register will clear all the flags in the PAFLG register. Timer module or Pulse Accumulator must stay enabled (TEN=1 or PAEN=1) while clearing these bits.

Chapter 23

Voltage Regulator (S12VREGL3V3V1)

Table 23-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.02	09 Sep 2005	23.3.2.3/23-822	- Updates for API external access and LVR flags.
V01.03	23 Sep 2005	23.3.2.1/23-820	- VAE reset value is 1.
V01.04	08 Jun 2007	23.4.6/23-827	- Added temperature sensor to customer information

23.1 Introduction

Module VREG_3V3 is a tri output voltage regulator that provides two separate 1.84V (typical) supplies differing in the amount of current that can be sourced and a 2.82V (typical) supply. The regulator input voltage range is from 3.3V up to 5V (typical).

23.1.1 Features

Module VREG_3V3 includes these distinctive features:

- Three parallel, linear voltage regulators with bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR)
- Low-voltage reset (LVR)
- High Temperature Detect (HTD) with High Temperature Interrupt (HTI)
- Autonomous periodical interrupt (API)

23.1.2 Modes of Operation

There are three modes VREG_3V3 can operate in:

1. Full performance mode (FPM) (MCU is not in stop mode)
The regulator is active, providing the nominal supply voltages with full current sourcing capability. Features LVD (low-voltage detect), LVR (low-voltage reset), and POR (power-on reset) and HTD (High Temperature Detect) are available. The API is available.
2. Reduced power mode (RPM) (MCU is in stop mode)
The purpose is to reduce power consumption of the device. The output voltage may degrade to a lower value than in full performance mode, additionally the current sourcing capability is substantially reduced. Only the POR is available in this mode, LVD, LVR and HTD are disabled. The API is available.

Chapter 24

128 KByte Flash Module (S12XFTM128K2V1)

Table 24-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.10	30 Nov 2007	24.1.3/24-834	- Correction to Table 24-6
V01.11	19 Dec 2007	24.4.2/24-867 24.4.2/24-867 24.4.2/24-867 24.4.2/24-867 24.3.1/24-836 24.1.3/24-834 24.3.1/24-836 24.1.2.2/24-833 24.3.1/24-836	- Removed Load Data Field command 0x05 - Updated Command Error Handling tables based on parent-child relationship with FTM256K2 - Corrected Error Handling table for Full Partition D-Flash, Partition D-Flash, and EEPROM Emulation Query commands - Corrected maximum allowed ERPART for Full Partition D-Flash and Partition D-Flash commands - Corrected P-Flash IFR Accessibility table - Corrected Buffer RAM size in Feature List - Corrected EEE Resource Memory Map - Changed D-Flash size from 16Kbytes to 32Kbytes - Corrected P-Flash Memory Map
V01.12	25 Sep 2009	24.1/24-832 24.3.2.1/24-843 24.4.2.4/24-870 24.4.2.6/24-871 24.4.2.11/24-875 24.4.2.11/24-875 24.4.2.11/24-875 24.4.2.19/24-884 24.3.2/24-841 24.3.2.1/24-843 24.4.1.2/24-862 24.6/24-890	- Change references for D-Flash from 16 Kbytes to 32 Kbytes - Clarify single bit fault correction for P-Flash phrase - Expand FDIV vs OSCCLK Frequency table - Add statement concerning code runaway when executing Read Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Program Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Verify Backdoor Access Key command from Flash block containing associated fields - Relate Key 0 to associated Backdoor Comparison Key address - Change “power down reset” to “reset” - Add ACCERR condition for Disable EEPROM Emulation command The following changes were made to clarify module behavior related to Flash register access during reset sequence and while Flash commands are active: - Add caution concerning register writes while command is active - Writes to FCLKDIV are allowed during reset sequence while CCIF is clear - Add caution concerning register writes while command is active - Writes to FCCOBIX, FCCOBHI, FCCOBLO registers are ignored during reset sequence

D-Flash Sector — The D-Flash sector is the smallest portion of the D-Flash memory that can be erased. The D-Flash sector consists of four 64 byte rows for a total of 256 bytes.

EEE (Emulated EEPROM) — A method to emulate the small sector size features and endurance characteristics associated with an EEPROM.

EEE IFR — Nonvolatile information register located in the D-Flash block that contains data required to partition the D-Flash memory and buffer RAM for EEE. The EEE IFR is visible in the global memory map by setting the EEEIFRON bit in the MMCCTL1 register.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes eight ECC bits for single bit fault correction and double bit fault detection within the phrase.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 1024 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Device ID, Version ID, and the Program Once field. The Program IFR is visible in the global memory map by setting the PGMIFRON bit in the MMCCTL1 register.

25.1.2 Features

25.1.2.1 P-Flash Features

- 256 Kbytes of P-Flash memory composed of two 128 Kbyte Flash blocks. The 128 Kbyte Flash blocks are each divided into 128 sectors of 1024 bytes.
- Single bit fault correction and double bit fault detection within a 64-bit phrase during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to program up to one phrase in each P-Flash block simultaneously
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

25.1.2.2 D-Flash Features

- Up to 32 Kbytes of D-Flash memory with 256 byte sectors for user access
- Dedicated commands to control access to the D-Flash memory over EEE operation
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Ability to program up to four words in a burst sequence

Table 25-9. FDIV vs OSCCLK Frequency

OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]	OSCCLK Frequency (MHz)		FDIV[6:0]
MIN ⁽¹⁾	MAX ⁽²⁾		MIN ¹	MAX ²		MIN ¹	MAX ²	
			33.60	34.65	0x20	67.20	68.25	0x40
1.60	2.10	0x01	34.65	35.70	0x21	68.25	69.30	0x41
2.40	3.15	0x02	35.70	36.75	0x22	69.30	70.35	0x42
3.20	4.20	0x03	36.75	37.80	0x23	70.35	71.40	0x43
4.20	5.25	0x04	37.80	38.85	0x24	71.40	72.45	0x44
5.25	6.30	0x05	38.85	39.90	0x25	72.45	73.50	0x45
6.30	7.35	0x06	39.90	40.95	0x26	73.50	74.55	0x46
7.35	8.40	0x07	40.95	42.00	0x27	74.55	75.60	0x47
8.40	9.45	0x08	42.00	43.05	0x28	75.60	76.65	0x48
9.45	10.50	0x09	43.05	44.10	0x29	76.65	77.70	0x49
10.50	11.55	0x0A	44.10	45.15	0x2A	77.70	78.75	0x4A
11.55	12.60	0x0B	45.15	46.20	0x2B	78.75	79.80	0x4B
12.60	13.65	0x0C	46.20	47.25	0x2C	79.80	80.85	0x4C
13.65	14.70	0x0D	47.25	48.30	0x2D	80.85	81.90	0x4D
14.70	15.75	0x0E	48.30	49.35	0x2E	81.90	82.95	0x4E
15.75	16.80	0x0F	49.35	50.40	0x2F	82.95	84.00	0x4F
16.80	17.85	0x10	50.40	51.45	0x30	84.00	85.05	0x50
17.85	18.90	0x11	51.45	52.50	0x31	85.05	86.10	0x51
18.90	19.95	0x12	52.50	53.55	0x32	86.10	87.15	0x52
19.95	21.00	0x13	53.55	54.60	0x33	87.15	88.20	0x53
21.00	22.05	0x14	54.60	55.65	0x34	88.20	89.25	0x54
22.05	23.10	0x15	55.65	56.70	0x35	89.25	90.30	0x55
23.10	24.15	0x16	56.70	57.75	0x36	90.30	91.35	0x56
24.15	25.20	0x17	57.75	58.80	0x37	91.35	92.40	0x57
25.20	26.25	0x18	58.80	59.85	0x38	92.40	93.45	0x58
26.25	27.30	0x19	59.85	60.90	0x39	93.45	94.50	0x59
27.30	28.35	0x1A	60.90	61.95	0x3A	94.50	95.55	0x5A
28.35	29.40	0x1B	61.95	63.00	0x3B	95.55	96.60	0x5B
29.40	30.45	0x1C	63.00	64.05	0x3C	96.60	97.65	0x5C
30.45	31.50	0x1D	64.05	65.10	0x3D	97.65	98.70	0x5D
31.50	32.55	0x1E	65.10	66.15	0x3E	98.70	99.75	0x5E
32.55	33.60	0x1F	66.15	67.20	0x3F	99.75	100.80	0x5F

1. FDIV shown generates an FCLK frequency of >0.8 MHz

Table 25-14. FECCRIX Field Descriptions

Field	Description
2-0 ECCRIX[2:0]	ECC Error Register Index — The ECCRIX bits are used to select which word of the FECCR register array is being read. See Section 25.3.2.13, “Flash ECC Error Results Register (FECCR)” , for more details.

25.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU or XGATE.

Offset Module Base + 0x0004

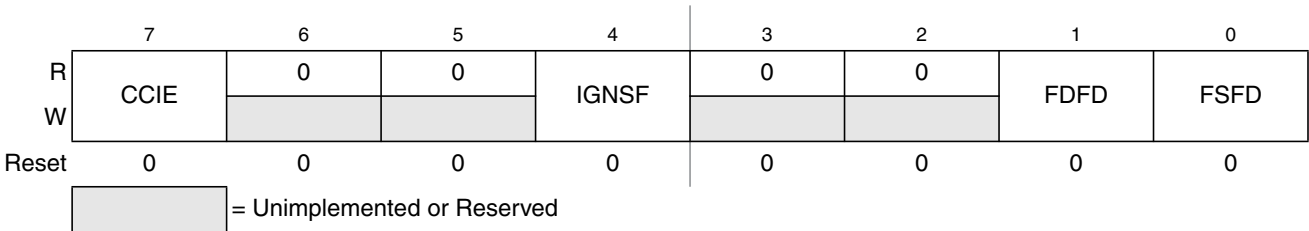


Figure 25-9. Flash Configuration Register (FCNFG)

CCIE, IGNSF, FDFD, and FSFD bits are readable and writable while remaining bits read 0 and are not writable.

Table 25-15. FCNFG Field Descriptions

Field	Description
7 CCIE	Command Complete Interrupt Enable — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 25.3.2.7)
4 IGNSF	Ignore Single Bit Fault — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 25.3.2.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated

25.4.1.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see [Section 25.3.2.3](#)).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in [Figure 25-26](#).

Table 25-32. D-Flash Commands

FCMD	Command	Function on D-Flash Memory
0x08	Erase All Blocks	Erase all D-Flash (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the EPDIS and EPOPEN bits in the EPROT register are set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x0F	Full Partition D-Flash	Erase the D-Flash block and partition an area of the D-Flash block for user access.
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.
0x13	Enable EEPROM Emulation	Enable EEPROM emulation where writes to the buffer RAM EEE partition will be copied to the D-Flash EEE partition.
0x14	Disable EEPROM Emulation	Suspend all current erase and program activity related to EEPROM emulation but leave current EEE tags set.
0x15	EEPROM Emulation Query	Returns EEE partition and status variables.
0x20	Partition D-Flash	Partition an area of the D-Flash block for user access.

25.4.2 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set and the FECCR registers will be loaded with the global address used in the invalid read operation with the data and parity fields set to all 0.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see [Section 25.3.2.7](#)).

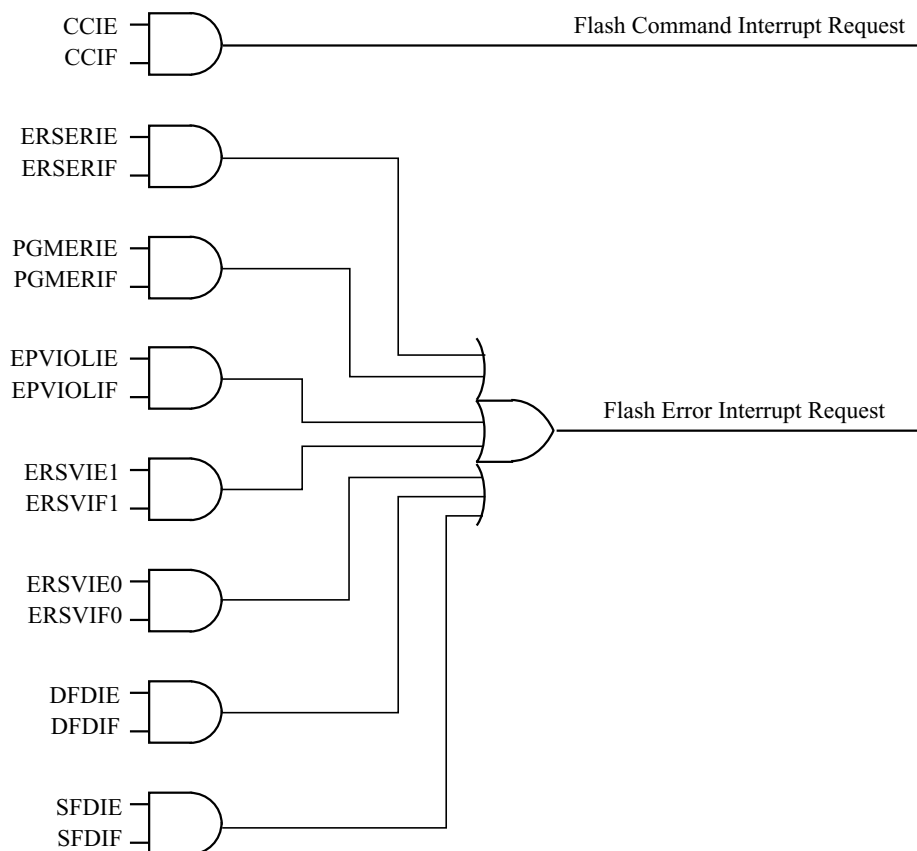


Figure 25-27. Flash Module Interrupts Implementation

25.4.4 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see [Section 25.4.3, “Interrupts”](#)).

25.4.5 Stop Mode

If a Flash command is active (CCIF = 0) or an EE-Emulation operation is pending when the MCU requests stop mode, the current Flash operation will be completed before the CPU is allowed to enter stop mode.

25.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see [Table 25-12](#)). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x7F_FF0F.

containing the EEE protection byte during the reset sequence, the EPOPEN bit will be cleared and remaining bits in the EPROT register will be set to leave the buffer RAM EEE partition fully protected.

Trying to write data to any protected area in the buffer RAM EEE partition will result in a protection violation error and the EPVIOLIF flag will be set in the FERSTAT register. Trying to write data to any protected area in the buffer RAM partitioned for user access will not be prevented and the EPVIOLIF flag in the FERSTAT register will not set.

Table 29-24. EPROT Field Descriptions

Field	Description
7 EPOPEN	Enables writes to the Buffer RAM partitioned for EEE 0 The entire buffer RAM EEE partition is protected from writes 1 Unprotected buffer RAM EEE partition areas are enabled for writes
6–4 RNV[6:4]	Reserved Nonvolatile Bits — The RNV bits should remain in the erased state for future enhancements
3 EPDIS	Buffer RAM Protection Address Range Disable — The EPDIS bit determines whether there is a protected area in a specific region of the buffer RAM EEE partition. 0 Protection enabled 1 Protection disabled
2–0 EPS[2:0]	Buffer RAM Protection Size — The EPS[2:0] bits determine the size of the protected area in the buffer RAM EEE partition as shown in Table 29-21 . The EPS bits can only be written to while the EPDIS bit is set.

Table 29-25. Buffer RAM EEE Partition Protection Address Range

EPS[2:0]	Global Address Range	Protected Size
000	0x13_FFC0 – 0x13_FFFF	64 bytes
001	0x13_FF80 – 0x13_FFFF	128 bytes
010	0x13_FF40 – 0x13_FFFF	192 bytes
011	0x13_FF00 – 0x13_FFFF	256 bytes
100	0x13_FEC0 – 0x13_FFFF	320 bytes
101	0x13_FE80 – 0x13_FFFF	384 bytes
110	0x13_FE40 – 0x13_FFFF	448 bytes
111	0x13_FE00 – 0x13_FFFF	512 bytes

29.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.