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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xet256j2maar

Figure 1-3 shows XGATE local address translation to the global memory map. It indicates also the location of used internal resources in the memory map.

Table 1-3. XGATE Resources

Internal Resource	Size /KByte	$Address
XGATE RAM	32K	XGRAM_LOW = 0x0F_8000
FLASH	30K(1)	XGFLASH_HIGH = 0x78_8000

1. This value is calculated by the following formula: (64K -2K- XGRAMSIZE)

Table 1-4. Derivative Dependent Memory Parameters

Device	FLASH_LOW	PPAGE (1)	RAM_LOW	RPAGE (2)	EE_LOW	EPAGE
9S12XEP100	0x70_0000	64	0x0F_0000	16	0x13_F000	4(3) + 32(4)
9S12XEP768	0x74_0000	48	0x0F_4000	12	0x13_F000	4 + 32
9S12XEQ512	0x78_0000	32	0x0F_8000	8	0x13_F000	4 + 32
9S12XEx384	0x78_0000(5)	24	0x0F_A000	6	0x13_F000	4 + 32
9S12XET256 9S12XEA256 (6)	0x78_0000(7)	16	0x0F_C000	4	0x13_F000	4 + 32
9S12XEG128 9S12XEA128[6]	0x78_0000(8)	8	0x0F_D000	3	0x13_F800	2 + 32

1. Number of 16K pages addressable via PPAGE register
2. Number of 4K pages addressing the RAM. RAM can also be mapped to 0x4000 - 0x7FFF
3. Number of 1K pages addressing the Cache RAM via the EPAGE register counting downwards from 0xFF
4. Number of 1K pages addressing the Data flash via the EPAGE register starting upwards from 0x00
5. The 384K memory map is split into a 128K block from 0x78_0000 to 0x79_FFFF and a 256K block from 0x7C_0000 to 0x7F_FFFF
6. The 9S12XEA devices are a special bondout for access to extra ADC channels in 80QFP. Available in 80QFP only. WARNING: NOT PIN-COMPATIBLE WITH REST OF FAMILY.
7. The 256K memory map is split into a 128K block from 0x78_0000 to 0x79_FFFF and a 128K block from 0x7E_0000 to 0x7F_FFFF
8. The 128K memory map is split into a 64K block from 0x78_0000 to 0x78_FFFF and a 64K block from 0x7F_0000 to 0x7F_FFFF

Table 1-5. Derivative Dependent Flash Block Mapping

Device	0x70_0000	0x74_0000	0x78_0000	0x7A_0000	0x7C_0000	0x7E_0000
9S12XEP100	B3	B2	B1S	B1N	B0	
9S12XEP768	—	B2	B1S	B1N	B0	
9S12XEQ512	—	—	B1S	B1N	B0	
9S12XEx384	—	—	B1S	—	B0	

Table 1-8. Peripheral - Port Routing Options[1]

	CAN0	CAN1	CAN2	CAN3	CAN4	SCI0	SCI1	SCI2	SCI3	SCI4	SCI5	SCI6	SCI7	SPI0	SPI1	SPI2	IIC0	IIC1	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	TIM
PF[0]																			X				
PF[1]																				X			
PF[2]																					X		
PF[3]																						X	
PF[5:4]																	X						
PF[7:6]									X														
PH[1:0]												O			X								
PH[3:2]													O		X								
PH[5:4]										O						X							
PH[7:6]											O					X							
PJ[0]								O														O	
PJ[1]								O															
PJ[2]																				O			
PJ[3]																							
PJ[4]																		O	O				
PJ[5]																		O			O		
PJ[7:6]	X				O												O						
PL[1:0]										X													
PL[3:2]											X												
PL[5:4]												X											
PL[7:6]													X										
PM[1:0]	O																						
PM[3:2]	X	O												X									
PM[5:4]	X		O		X									X									
PM[7:6]				O	X				O														
PP[3:0]															O								X
PP[7:4]																O							X
PR[7:0]																							O

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

2.3.24 Port T Reduced Drive Register (RDRT)

Address 0x0243 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset	0	0	0	0	0	0	0	0

Figure 2-22. Port T Reduced Drive Register (RDRT)

1. Read: Anytime.
   Write: Anytime.

Table 2-23. RDRT Register Field Descriptions

Field	Description
7-0 RDRT	**Port T reduced drive**—Select reduced drive for outputs This register configures the drive strength of output pins 7 through 0 as either full or reduced independent of the function used on the pins. If a pin is used as input this bit has no effect. 1 Reduced drive selected (approx. 1/5 of the full drive strength). 0 Full drive strength enabled.

2.3.25 Port T Pull Device Enable Register (PERT)

Address 0x0244 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset	0	0	0	0	0	0	0	0

Figure 2-23. Port T Pull Device Enable Register (PERT)

1. Read: Anytime.
   Write: Anytime.

Table 2-24. PERT Register Field Descriptions

Field	Description
7-0 PERT	**Port T pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset no pull device is enabled. 1 Pull device enabled. 0 Pull device disabled.

2.3.87 Port R Data Direction Register (DDRR)

Address 0x036A — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	DDRR7	DDRR6	DDRR5	DDRR4	DDRR3	DDRR2	DDRR1	DDRR0
Reset	0	0	0	0	0	0	0	0

Figure 2-85. Port R Data Direction Register (DDRR)

1. Read: Anytime.
   Write: Anytime.

Table 2-83. DDRR Register Field Descriptions

Field	Description
7-0 DDRR	**Port R data direction**— This register controls the data direction of pins 7 through 0. The TIM forces the I/O state to be an output for each timer port associated with an enabled output compare. In this case the data direction bits will not change. The data direction bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled. The timer Input Capture always monitors the state of the pin. 1 Associated pin is configured as output. 0 Associated pin is configured as high-impedance input.

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTR or PTIR registers, when changing the DDRR register.

2.3.88 Port R Reduced Drive Register (RDRR)

Address 0x036B — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	RDRR7	RDRR6	RDRR5	RDRR4	RDRR3	RDRR2	RDRR1	RDRR0
Reset	0	0	0	0	0	0	0	0

Figure 2-86. Port R Reduced Drive Register (RDRR)

1. Read: Anytime.
   Write: Anytime.

Table 2-86. PPSR Register Field Descriptions

Field	Description
7-0 PPSR	**Port R pull device select**—Determine pull device polarity on input pins This register selects whether a pull-down or a pull-up device is connected to the pin. 1 A pull-down device is connected to the associated pin, if enabled and if the pin is used as input. 0 A pull-up device is connected to the associated pin, if enabled and if the pin is used as input.

2.3.91 PIM Reserved Register

Address 0x036E Access: User read(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-89. PIM Reserved Register

1. Read: Always reads 0x00
   Write: Unimplemented

2.3.92 Port R Routing Register (PTRRR)

Address 0x036F Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PTRRR7	PTRRR6	PTRRR5	PTRRR4	PTRRR3	PTRRR2	PTRRR1	PTRRR0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-90. Port R Routing Register (PTRRR)

1. Read: Anytime.
   Write: Anytime.

Table 2-87. PTR Routing Register Field Descriptions

Field	Description
7 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC7 is available on PP7 0 TIMIOC7 is available on PR7
6 PTRRR	**Port R routing**— This register configures the re-routing of the associated TIM channel. 1 TIMIOC6 is available on PP6 0 TIMIOC6 is available on PR6

3.3.2.3 Global Page Index Register (GPAGE)

Address: 0x0010

	7	6	5	4	3	2	1	0
R	0	GP6	GP5	GP4	GP3	GP2	GP1	GP0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6. Global Page Index Register (GPAGE)

Read: Anytime

Write: Anytime

The global page index register is used to construct a 23 bit address in the global map format. It is only used when the CPU is executing a global instruction (GLDAA, GLDAB, GLDD, GLDS, GLDX, GLDY,GSTAA, GSTAB, GSTD, GSTS, GSTX, GSTY) (see CPU Block Guide). The generated global address is the result of concatenation of the CPU local address [15:0] with the GPAGE register [22:16] (see Figure 3-7).

CAUTION

XGATE write access to this register during an CPU access which makes use of this register could lead to unexpected results.

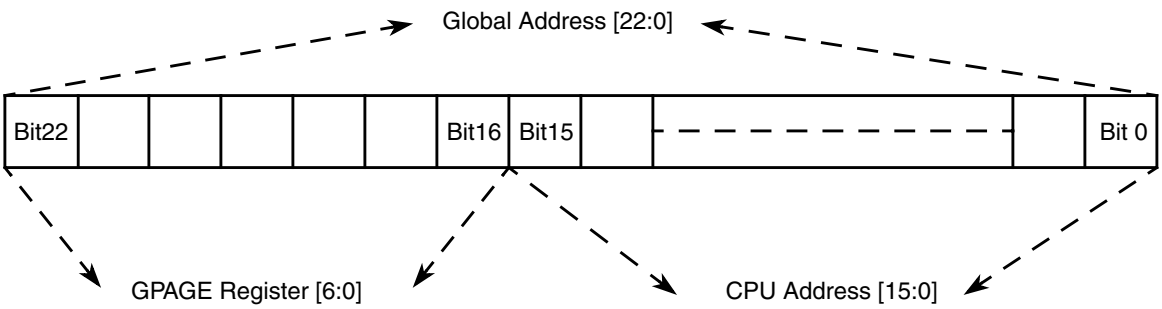

Figure 3-7. GPAGE Address Mapping

Table 3-9. GPAGE Field Descriptions

Field	Description
6–0 GP[6:0]	**Global Page Index Bits 6–0** — These page index bits are used to select which of the 128 64-kilobyte pages is to be accessed.

Example 3-1. This example demonstrates usage of the GPAGE register

```
LDX     #0x5000          ;Set GPAGE offset to the value of 0x5000
MOVB    #0x14, GPAGE     ;Initialize GPAGE register with the value of 0x14
GLDAA   X                ;Load Accu A from the global address 0x14_5000
```

7.3.2.4 BDM Global Page Index Register (BDMGPR)

Register Global Address 0x7FFF08

	7	6	5	4	3	2	1	0
R W	BGAE	BGP6	BGP5	BGP4	BGP3	BGP2	BGP1	BGP0
Reset	0	0	0	0	0	0	0	0

Figure 7-6. BDM Global Page Register (BDMGPR)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

Table 7-5. BDMGPR Field Descriptions

Field	Description
7 BGAE	**BDM Global Page Access Enable Bit** — BGAE enables global page access for BDM hardware and firmware read/write instructions The BDM hardware commands used to access the BDM registers (READ_BD_ and WRITE_BD_) can not be used for global accesses even if the BGAE bit is set. 0 BDM Global Access disabled 1 BDM Global Access enabled
6–0 BGP[6:0]	**BDM Global Page Index Bits 6–0** — These bits define the extended address bits from 22 to 16. For more detailed information regarding the global page window scheme, please refer to the S12X_MMC Block Guide.

7.3.3 Family ID Assignment

The family ID is a 8-bit value located in the firmware ROM (at global address: 0x7FFF0F). The read-only value is a unique family ID which is 0xC1 for S12X devices.

7.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

Hardware commands are used to read and write target system memory locations and to enter active background debug mode, see Section 7.4.3, “BDM Hardware Commands”. Target system memory includes all memory that is accessible by the CPU.

Firmware commands are used to read and write CPU resources and to exit from active background debug mode, see Section 7.4.4, “Standard BDM Firmware Commands”. The CPU resources referred to are the accumulator (D), X index register (X), Y index register (Y), stack pointer (SP), and program counter (PC).

Hardware commands can be executed at any time and in any mode excluding a few exceptions as highlighted (see Section 7.4.3, “BDM Hardware Commands”) and in secure mode (see Section 7.4.1, “Security”). Firmware commands can only be executed when the system is not secure and is in active background debug mode (BDM).

Table 7-7. Firmware Commands

Command[1]	Opcode (hex)	Data	Description
READ_NEXT[2]	62	16-bit data out	Increment X index register by 2 (X = X + 2), then read word X points to.
READ_PC	63	16-bit data out	Read program counter.
READ_D	64	16-bit data out	Read D accumulator.
READ_X	65	16-bit data out	Read X index register.
READ_Y	66	16-bit data out	Read Y index register.
READ_SP	67	16-bit data out	Read stack pointer.
WRITE_NEXT	42	16-bit data in	Increment X index register by 2 (X = X + 2), then write word to location pointed to by X.
WRITE_PC	43	16-bit data in	Write program counter.
WRITE_D	44	16-bit data in	Write D accumulator.
WRITE_X	45	16-bit data in	Write X index register.
WRITE_Y	46	16-bit data in	Write Y index register.
WRITE_SP	47	16-bit data in	Write stack pointer.
GO	08	none	Go to user program. If enabled, ACK will occur when leaving active background mode.
GO_UNTIL[3]	0C	none	Go to user program. If enabled, ACK will occur upon returning to active background mode.
TRACE1	10	none	Execute one user instruction then return to active BDM. If enabled, ACK will occur upon returning to active background mode.
TAGGO -> GO	18	none	(Previous enable tagging and go to user program.) This command will be deprecated and should not be used anymore. Opcode will be executed as a GO command.

1. If enabled, ACK will occur when data is ready for transmission for all BDM READ commands and will occur after the write is complete for all BDM WRITE commands.
2. When the firmware command READ_NEXT or WRITE_NEXT is used to access the BDM address space the BDM resources are accessed rather than user code. Writing BDM firmware is not possible.
3. System stop disables the ACK function and ignored commands will not have an ACK-pulse (e.g., CPU in stop or wait mode). The GO_UNTIL command will not get an Acknowledge if CPU executes the wait or stop instruction before the “UNTIL” condition (BDM active again) is reached (see Section 7.4.7, “Serial Interface Hardware Handshake Protocol” last Note).

7.4.5 BDM Command Structure

Hardware and firmware BDM commands start with an 8-bit opcode followed by a 16-bit address and/or a 16-bit data word depending on the command. All the read commands return 16 bits of data despite the byte or word implication in the command name.

8-bit reads return 16-bits of data, of which, only one byte will contain valid data. If reading an even address, the valid data will appear in the MSB. If reading an odd address, the valid data will appear in the LSB.

after a system stop mode the handshake feature must be enabled again by sending the ACK_ENABLE command.

7.4.11 Serial Communication Time Out

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD in order to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any time-out limit.

Consider now the case where the host returns BKGD to logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge marking the start of a new bit. If, however, a new falling edge is not detected by the target within 512 clock cycles since the last falling edge, a time-out occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. However, consider the behavior where the BDM is running in a frequency much greater than the CPU frequency. In this case, the command could time out before the data is ready to be retrieved. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDM and CPU) when the hardware handshake protocol is enabled, the time out between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles and still be able to retrieve the data from an issued read command. However, once the handshake pulse (ACK pulse) is issued, the time-out feature is re-activated, meaning that the target will time out after 512 clock cycles. Therefore, the host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any negative edge in the BKGD pin after the time-out period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data, has occurred the time out in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next negative edge in the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

Table 10-7. XGISP74 Field Descriptions

Field	Description
15–1 XBISP74[15:1]	**Initial Stack Pointer**— The XGISP74 register holds the initial value of RISC core register R7, for threads of priority 7 to 4.

10.3.1.6 XGATE Initial Stack Pointer for Interrupt Priorities 3 to 1 (XGISP31)

The XGISP31 register is intended to point to the stack region that is used by XGATE channels of priority 3 to 1. Every time a thread of such priority is started, RISC core register R7 will be initialized with the content of XGISP31.

Module Base +0x0006

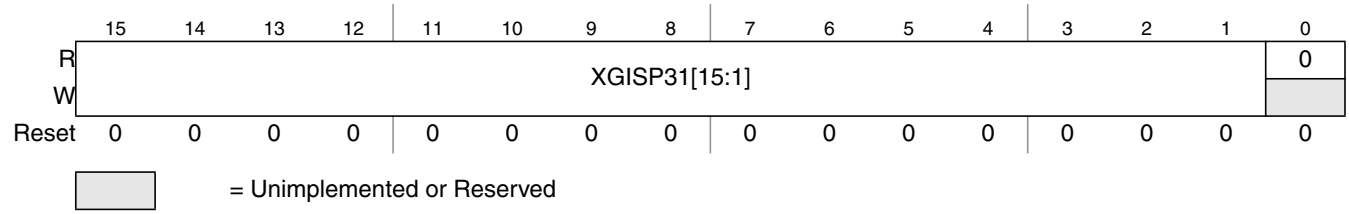

Figure 10-8. XGATE Initial Stack Pointer for Interrupt Priorities 3 to 1 (XGISP31)

Read: Anytime

Write: Only if XGATE requests are disabled (XGE = 0) and idle (XGCHID = $00))

Table 10-8. XGISP31 Field Descriptions

Field	Description
15–1 XBISP31[15:1]	**Initial Stack Pointer**— The XGISP31 register holds the initial value of RISC core register R7, for threads of priority 3 to 1.

10.3.1.7 XGATE Vector Base Address Register (XGVBR)

The Vector Base Address Register (Figure 10-9) determines the location of the XGATE vector block (see Section Figure 10-23., “XGATE Vector Block).

Module Base +0x0006

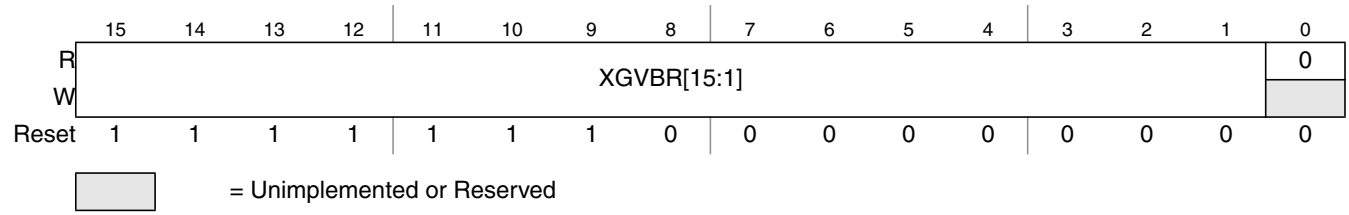

Figure 10-9. XGATE Vector Base Address Register (XGVBR)

Read: Anytime

Write: Only if XGATE requests are disabled (XGE = 0) and idle (XGCHID = $00))

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0024	ATDDR10	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0026	ATDDR11	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0028	ATDDR12	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x002A	ATDDR13	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x002C	ATDDR14	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x002E	ATDDR15	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							

= Unimplemented or Reserved

Figure 13-2. ADC12B16C Register Summary (Sheet 3 of 3)

13.3.2 Register Descriptions

This section describes in address order all the ADC12B16C registers and their individual bits.

13.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 13-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 13-2. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 13-3.

Table 13-3. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved(1)

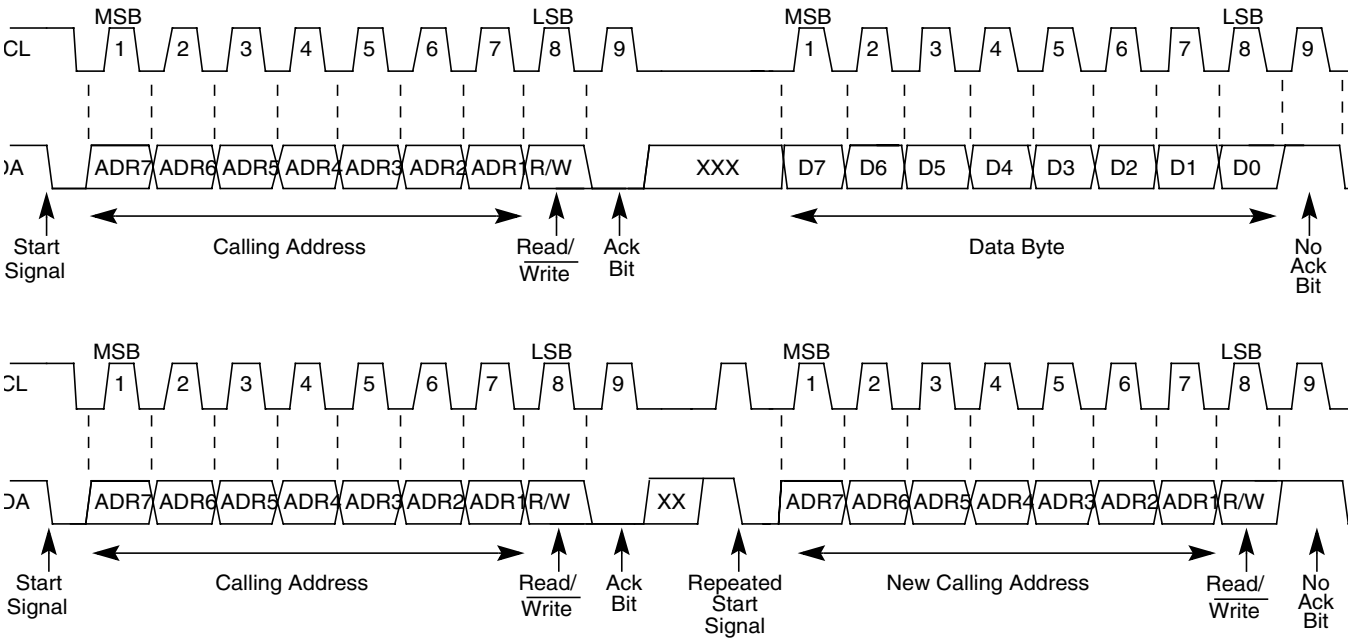

Figure 15-10. IIC-Bus Transmission Signals

15.4.1.1 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCL and SDA lines are at logical high), a master may initiate communication by sending a START signal.As shown in Figure 15-10, a START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and brings all slaves out of their idle states.

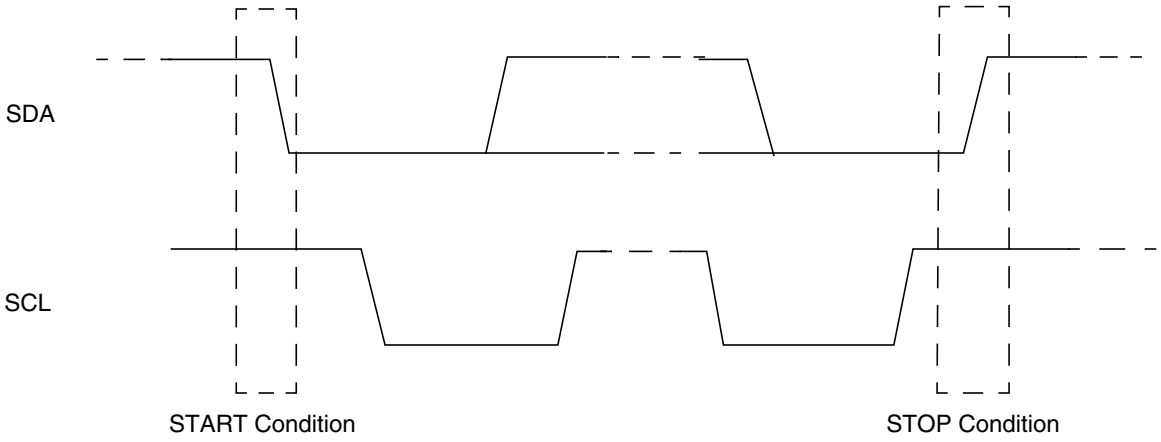

Figure 15-11. Start and Stop Conditions

Table 22-17. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 or PAEN bit of PACTL is set to one (See also TCRE control bit explanation.)

22.3.2.14 Timer Input Capture/Output Compare Registers High and Low 0–7 (TCxH and TCxL)

Module Base + 0x0010 = TC0H
0x0012 = TC1H
0x0014 = TC2H
0x0016 = TC3H
0x0018 = TC4H
0x001A = TC5H
0x001C = TC6H
0x001E = TC7H

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 22-22. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base + 0x0011 = TC0L
0x0013 = TC1L
0x0015 = TC2L
0x0017 = TC3L
0x0019 = TC4L
0x001B = TC5L
0x001D = TC6L
0x001F = TC7L

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 22-23. Timer Input Capture/Output Compare Register x Low (TCxL)

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should takes place before low byte otherwise it will give a different result.

22.3.2.15 16-Bit Pulse Accumulator Control Register (PACTL)

Module Base + 0x0020

	7	6	5	4	3	2	1	0
R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 22-24. 16-Bit Pulse Accumulator Control Register (PACTL)

When PAEN is set, the PACT is enabled.The PACT shares the input pin with IOC7.

Read: Any time

Write: Any time

Table 22-18. PACTL Field Descriptions

Field	Description
6 PAEN	**Pulse Accumulator System Enable** — PAEN is independent from TEN. With timer disabled, the pulse accumulator can function unless pulse accumulator is disabled. 0 16-Bit Pulse Accumulator system disabled. 1 Pulse Accumulator system enabled.
5 PAMOD	**Pulse Accumulator Mode** — This bit is active only when the Pulse Accumulator is enabled (PAEN = 1). See Table 22-19. 0 Event counter mode. 1 Gated time accumulation mode.
4 PEDGE	**Pulse Accumulator Edge Control** — This bit is active only when the Pulse Accumulator is enabled (PAEN = 1). For PAMOD bit = 0 (event counter mode). See Table 22-19. 0 Falling edges on IOC7 pin cause the count to be incremented. 1 Rising edges on IOC7 pin cause the count to be incremented. For PAMOD bit = 1 (gated time accumulation mode). 0 IOC7 input pin high enables M (bus clock) divided by 64 clock to Pulse Accumulator and the trailing falling edge on IOC7 sets the PAIF flag. 1 IOC7 input pin low enables M (bus clock) divided by 64 clock to Pulse Accumulator and the trailing rising edge on IOC7 sets the PAIF flag.
3:2 CLK[1:0]	**Clock Select Bits —** Refer to Table 22-20.
1 PAOVI	**Pulse Accumulator Overflow Interrupt Enable** 0 Interrupt inhibited. 1 Interrupt requested if PAOVF is set.
0 PAI	**Pulse Accumulator Input Interrupt Enable** 0 Interrupt inhibited. 1 Interrupt requested if PAIF is set.

23.2.4 VDDF — Regulator Output2 (NVM Logic) Pins

Signals VDDF/VSS are the secondary outputs of VREG_3V3 that provide the power supply for the NVM logic. These signals are connected to device pins to allow external decoupling capacitors (220 nF, X7R ceramic).

In Shutdown Mode an external supply driving VDDF/VSS can replace the voltage regulator.

23.2.5 VDDPLL, VSSPLL — Regulator Output3 (PLL) Pins

Signals VDDPLL/VSSPLL are the secondary outputs of VREG_3V3 that provide the power supply for the PLL and oscillator. These signals are connected to device pins to allow external decoupling capacitors (100 nF...220 nF, X7R ceramic).

In Shutdown Mode, an external supply driving VDDPLL/VSSPLL can replace the voltage regulator.

23.2.6 VDDX — Power Input Pin

Signals VDDX/VSS are monitored by VREG_3V3 with the LVR feature.

23.2.7 VREGEN — Optional Regulator Enable Pin

This optional signal is used to shutdown VREG_3V3. In that case, VDD/VSS and VDDPLL/VSSPLL must be provided externally. Shutdown mode is entered with VREGEN being low. If VREGEN is high, the VREG_3V3 is either in Full Performance Mode or in Reduced Power Mode.

For the connectivity of VREGEN, see device specification.

NOTE

Switching from FPM or RPM to shutdown of VREG_3V3 and vice versa is not supported while MCU is powered.

23.2.8 VREG_API — Optional Autonomous Periodical Interrupt Output Pin

This pin provides the signal selected via APIEA if system is set accordingly. See 23.3.2.3, “Autonomous Periodical Interrupt Control Register (VREGAPICL) and 23.4.8, “Autonomous Periodical Interrupt (API) for details.

For the connectivity of VREG_API, see device specification.

23.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in VREG_3V3.

If enabled in the system, the VREG_3V3 will abort all read and write accesses to reserved registers within it’s memory slice. See device level specification for details.

24.4.2.19 Disable EEPROM Emulation Command

The Disable EEPROM Emulation command causes the Memory Controller to suspend current EEE activity.

Table 24-71. Disable EEPROM Emulation Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x14	Not required

Upon clearing CCIF to launch the Disable EEPROM Emulation command, the Memory Controller will halt EEE operations at the next convenient point without clearing the EEE tag RAM or tag counter before setting the CCIF flag.

Table 24-72. Disable EEPROM Emulation Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if Full Partition D-Flash or Partition D-Flash command not previously run
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None
FERSTAT	EPVIOLIF	None

24.4.2.20 EEPROM Emulation Query Command

The EEPROM Emulation Query command returns EEE partition and status variables.

Table 24-73. EEPROM Emulation Query Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x15	Not required
001	Return DFPART	
010	Return ERPART	
011	Return ECOUNT(1)	
100	Return Dead Sector Count	Return Ready Sector Count

1. Indicates sector erase count

Upon clearing CCIF to launch the EEPROM Emulation Query command, the CCIF flag will set after the EEE partition and status variables are stored in the FCCOBIX register.If the Emulation Query command is executed prior to partitioning (Partition D-Flash Command Section 24.4.2.14), the following reset values are returned: DFPART = 0x_FFFF, ERPART = 0x_FFFF, ECOUNT = 0x_FFFF, Dead Sector Count = 0x_00, Ready Sector Count = 0x_00.

Chapter 25
256 KByte Flash Module (S12XFTM256K2V1)

Table 25-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.08	14 Nov 2007	25.5.2/25-951 25.4.2/25-927 25.4.2.8/25-933	- Changed terminology from ‘word program’ to “Program P-Flash’ in the BDM unsecuring description, Section 25.5.2 - Added requirement that user not write any Flash module register during execution of commands ‘Erase All Blocks’, Section 25.4.2.8, and ‘Unsecure Flash’, Section 25.4.2.11 - Added statement that security is released upon successful completion of command ‘Erase All Blocks’, Section 25.4.2.8
V01.09	19 Dec 2007	25.4.2.5/25-930 25.4.2/25-927 25.3.1/25-896	- Corrected Error Handling table for Load Data Field command - Corrected Error Handling table for Full Partition D-Flash, Partition D-Flash, and EEPROM Emulation Query commands - Corrected P-Flash IFR Accessibility table
V01.10	25 Sep 2009	25.1/25-891 25.3.2.1/25-903 25.4.2.4/25-930 25.4.2.7/25-932 25.4.2.12/25-936 25.4.2.12/25-936 25.4.2.12/25-936 25.4.2.20/25-945 25.3.2/25-901 25.3.2.1/25-903 25.4.1.2/25-922 25.6/25-951	- Clarify single bit fault correction for P-Flash phrase - Expand FDIV vs OSCCLK Frequency table - Add statement concerning code runaway when executing Read Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Program Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Verify Backdoor Access Key command from Flash block containing associated fields - Relate Key 0 to associated Backdoor Comparison Key address - Change “power down reset” to “reset” - Add ACCERR condition for Disable EEPROM Emulation command The following changes were made to clarify module behavior related to Flash register access during reset sequence and while Flash commands are active: - Add caution concerning register writes while command is active - Writes to FCLKDIV are allowed during reset sequence while CCIF is clear - Add caution concerning register writes while command is active - Writes to FCCOBIX, FCCOBHI, FCCOBLO registers are ignored during reset sequence

25.1 Introduction

The FTM256K2 module implements the following:

- 256 Kbytes of P-Flash (Program Flash) memory, consisting of 2 physical Flash blocks, intended primarily for nonvolatile code storage

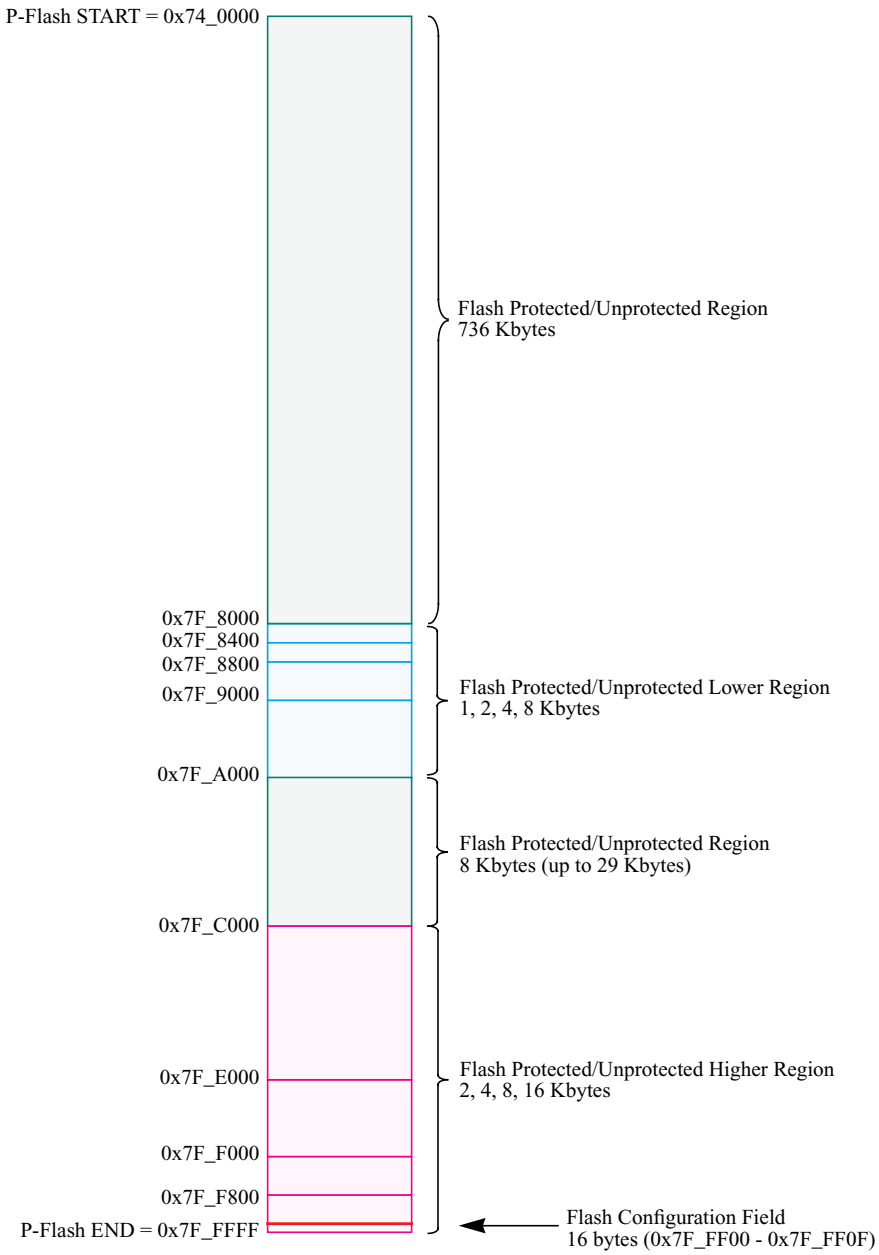

Figure 28-2. P-Flash Memory Map

A.3.1.19 Enable EEE (FCMD=0x13)

The maximum time to enable EPROM emulation is given by

$$t = \left(\left(((1100 \cdot BWN + (176 \cdot (1 + BWN) + (BWN + N_{SEC}) \cdot 32364))) \cdot \frac{1}{f_{NVMOP}}\right) + \left((3050 \cdot (1 + BWN) + (N_{SEC} + BWN) \cdot 290500) \cdot \frac{1}{f_{NVMBUS}}\right)\right)$$

where N_{SEC} is the number of sectors of constant data. A constant sector is one in which all 63 records contain the latest active data and would need to be copied. The maximum possible is 33 (2048 EEE RAM words /63 =32.5) although this is a highly unlikely scenario. The impact of a worst case brownout recovery scenario is denoted by BWN = 2 for non brownout situations BWN =0.

0x00338–0x033F Asynchronous Serial Interface (SCI7) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0338	SCI7BDH[1]	R	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x0339	SCI7BDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x033A	SCI7CR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x0338	SCI7ASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		W								
0x0339	SCI7ACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		W								
0x033A	SCI7ACR2[2]	R	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		W								
0x033B	SCI7CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x033C	SCI7SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x033D	SCI7SR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x033E	SCI7DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x033F	SCI7DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1. Those registers are accessible if the AMAP bit in the SCI7SR2 register is set to zero
2. Those registers are accessible if the AMAP bit in the SCI7SR2 register is set to one

0x00340–0x0367 – Periodic Interrupt Timer (PIT) Map (Sheet 1 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0340	PITCFLMT	R	PITE	PITSWAI	PITFRZ	0	0	0	0	0
		W							PFLMT1	PFLMT0
0x0341	PITFLT	R	0	0	0	0	0	0	0	0
		W	PFLT7	PFLT6	PFLT5	PFLT4	PFLT3	PFLT2	PFLT1	PFLT0
0x0342	PITCE	R	PCE7	PCE6	PCE5	PCE4	PCE3	PCE2	PCE1	PCE0
		W								
0x0343	PITMUX	R	PMUX7	PMUX6	PMUX5	PMUX4	PMUX3	PMUX2	PMUX1	PMUX0
		W								
0x0344	PITINTE	R	PINTE7	PINTE6	PINTE5	PINTE4	PINTE3	PINTE2	PINTE1	PINTE0
		W								
0x0345	PITTF	R	PTF7	PTF6	PTF5	PTF4	PTF3	PTF2	PTF1	PTF0
		W								
0x0346	PITMTLD0	R	PMTLD7	PMTLD6	PMTLD5	PMTLD4	PMTLD3	PMTLD2	PMTLD1	PMTLD0
		W								
0x0347	PITMTLD1	R	PMTLD7	PMTLD6	PMTLD5	PMTLD4	PMTLD3	PMTLD2	PMTLD1	PMTLD0
		W								
0x0348	PITLD0 (hi)	R	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
		W								