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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=s912xet256j2mal">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=s912xet256j2mal</a>

**Table 1-14. Interrupt Vector Locations (Sheet 2 of 4)**

Vector Address <sup>(1)</sup>	XGATE Channel ID <sup>(2)</sup>	Interrupt Source	CCR Mask	Local Enable	STOP Wake up	WAIT Wake up
Vector base + \$BE	\$5F	SPI1	I bit	SPI1CR1 (SPIE, SPTIE)	No	Yes
Vector base + \$BC	\$5E	SPI2	I bit	SPI2CR1 (SPIE, SPTIE)	No	Yes
Vector base + \$BA	\$5D	FLASH Fault Detect	I bit	FCNFG2 (FDIE)	No	No
Vector base + \$B8	\$5C	FLASH	I bit	FCNFG (CCIE, CBEIE)	No	Yes
Vector base + \$B6	\$5B	CAN0 wake-up	I bit	CAN0RIER (WUPIE)	Yes	Yes
Vector base + \$B4	\$5A	CAN0 errors	I bit	CAN0RIER (CSCIE, OVRIE)	No	Yes
Vector base + \$B2	\$59	CAN0 receive	I bit	CAN0RIER (RXFIE)	No	Yes
Vector base + \$B0	\$58	CAN0 transmit	I bit	CAN0TIER (TXEIE[2:0])	No	Yes
Vector base + \$AE	\$57	CAN1 wake-up	I bit	CAN1RIER (WUPIE)	Yes	Yes
Vector base + \$AC	\$56	CAN1 errors	I bit	CAN1RIER (CSCIE, OVRIE)	No	Yes
Vector base + \$AA	\$55	CAN1 receive	I bit	CAN1RIER (RXFIE)	No	Yes
Vector base + \$A8	\$54	CAN1 transmit	I bit	CAN1TIER (TXEIE[2:0])	No	Yes
Vector base + \$A6	\$53	CAN2 wake-up	I bit	CAN2RIER (WUPIE)	Yes	Yes
Vector base + \$A4	\$52	CAN2 errors	I bit	CAN2RIER (CSCIE, OVRIE)	No	Yes
Vector base + \$A2	\$51	CAN2 receive	I bit	CAN2RIER (RXFIE)	No	Yes
Vector base + \$A0	\$50	CAN2 transmit	I bit	CAN2TIER (TXEIE[2:0])	No	Yes
Vector base + \$9E	\$4F	CAN3 wake-up	I bit	CAN3RIER (WUPIE)	Yes	Yes
Vector base+ \$9C	\$4E	CAN3 errors	I bit	CAN3RIER (CSCIE, OVRIE)	No	Yes
Vector base+ \$9A	\$4D	CAN3 receive	I bit	CAN3RIER (RXFIE)	No	Yes
Vector base + \$98	\$4C	CAN3 transmit	I bit	CAN3TIER (TXEIE[2:0])	No	Yes
Vector base + \$96	\$4B	CAN4 wake-up	I bit	CAN4RIER (WUPIE)	Yes	Yes
Vector base + \$94	\$4A	CAN4 errors	I bit	CAN4RIER (CSCIE, OVRIE)	No	Yes
Vector base + \$92	\$49	CAN4 receive	I bit	CAN4RIER (RXFIE)	No	Yes
Vector base + \$90	\$48	CAN4 transmit	I bit	CAN4TIER (TXEIE[2:0])	No	Yes
Vector base + \$8E	\$47	Port P Interrupt	I bit	PIEP (PIEP7-PIEP0)	Yes	Yes
Vector base+ \$8C	\$46	PWM emergency shutdown	I bit	PWMSDN (PWMIE)	No	Yes

### 2.3.17 IRQ Control Register (IRQCR)

Address 0x001E Access: User read/write<sup>(1)</sup>

	7	6	5	4	3	2	1	0
R	IRQE	IRQEN	0	0	0	0	0	0
W								
Reset	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

**Figure 2-15. IRQ Control Register (IRQCR)**

1. Read: See individual bit descriptions below.  
Write: See individual bit descriptions below.

**Table 2-17. IRQCR Register Field Descriptions**

Field	Description
7 IRQE	<b>IRQ select edge sensitive only—</b> Special modes: Read or write anytime. Normal & emulation modes: Read anytime, write once. 1 $\overline{\text{IRQ}}$ configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE = 1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ configured for low level recognition.
6 IRQEN	<b>External IRQ enable—</b> Read or write anytime. 1 External IRQ pin is connected to interrupt logic. 0 External IRQ pin is disconnected from interrupt logic.
5-0	<b>Reserved—</b>

### 2.3.18 PIM Reserved Register

This register is reserved for factory testing of the PIM module and is not available in normal operation.

Address 0x001F Access: User read<sup>(1)</sup>

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

**Figure 2-16. PIM Reserved Register**

1. Read: Always reads 0x00  
Write: Unimplemented

#### NOTE

Writing to this register when in special modes can alter the pin functionality.

- Expanded modes  
Address, data, and control signals are activated in normal expanded and special test modes when accessing the external bus. Access to internal resources will not cause activity on the external bus.
- Emulation modes  
External bus is active to emulate, via an external tool, the normal expanded or the normal single chip mode.}

### 3.1.5 Block Diagram

Figure 3-1<sup>1</sup> shows a block diagram of the MMC.

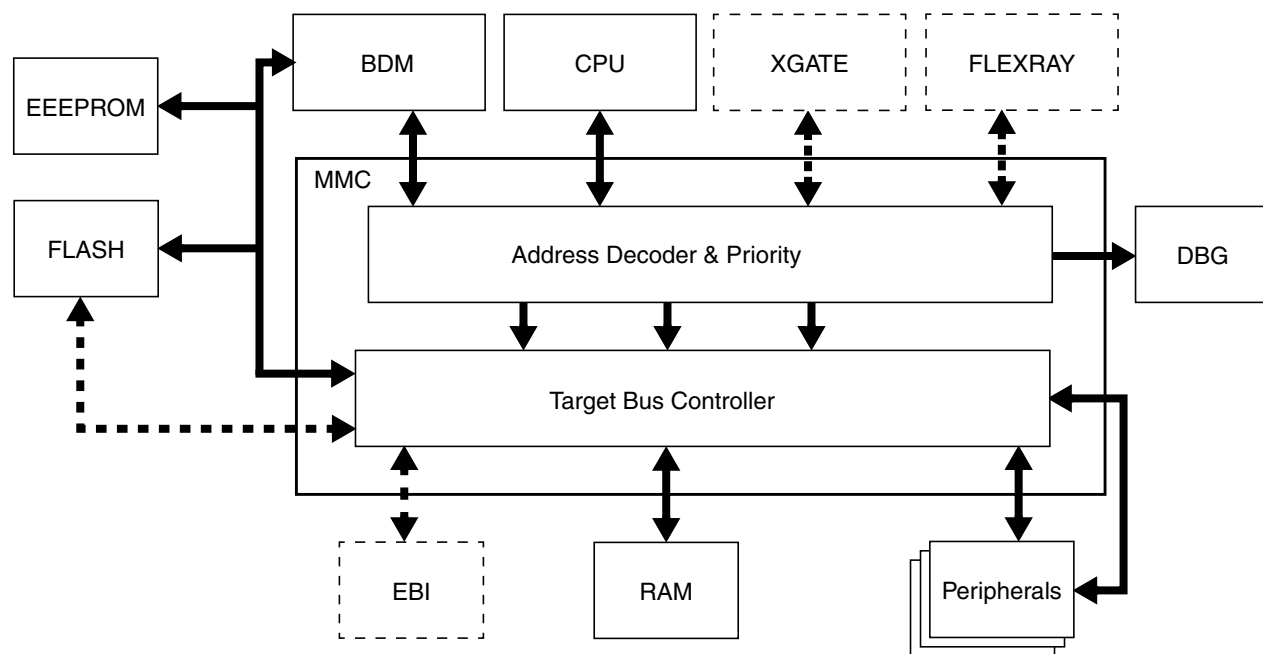


Figure 3-1. MMC Block Diagram

## 3.2 External Signal Description

The user is advised to refer to the device overview for port configuration and location of external bus signals. Some pins may not be bonded out in all implementations.

Table 3-3 and Table 3-4 outline the pin names and functions. It also provides a brief description of their operation.

1. Doted blocks and lines are optional. Please refer to the Device User Guide for their availibilities.



### 3.4.3 Chip Access Restrictions

CPU and XGATE accesses are watched in the memory protection unit (See MPU Block Guide). In case of access violation, the suspect master is acknowledged with an indication of an error; the victim target will not be accessed.

Other violations MPU is not handling are listed below.

#### 3.4.3.1 Illegal XGATE Accesses

A possible access error is flagged by the MMC and signalled to XGATE under the following conditions:

- XGATE performs misaligned word (in case of load-store or opcode or vector fetch accesses).
- XGATE accesses the register space (in case of opcode or vector fetch).
- XGATE performs a write to Flash in any modes (in case of load-store access).
- XGATE performs an access to a secured Flash in expanded modes (in case of load-store or opcode or vector fetch accesses).

For further details refer to the XGATE Block Guide.

### 3.4.4 Chip Bus Control

The MMC controls the address buses and the data buses that interface the S12X masters (CPU, BDM and XGATE) with the rest of the system (master buses). In addition the MMC handles all CPU read data bus swapping operations. All internal and external resources are connected to specific target buses (see [Figure 3-23<sup>1</sup>](#)).

1. Doted blocks and lines are optional. Please refer to the Device User Guide for their availibilities.

Table 4-9. MPUDESC1 Field Descriptions

Field	Description
7–0 LOW_ADDR[18:11]	<b>Memory range lower boundary address bits</b> — The LOW_ADDR[18:11] bits represent bits [18:11] of the global memory address that is used as the lower boundary for the described memory range.

### 4.3.1.8 MPU Descriptor Register 2 (MPUDESC2)

Address: Module Base + 0x0008

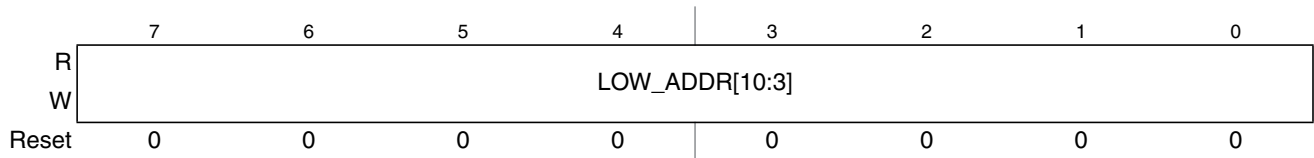


Figure 4-10. MPU Descriptor Register 2 (MPUDESC2)

Read: Anytime

Write: Anytime

Table 4-10. MPUDESC2 Field Descriptions

Field	Description
7–0 LOW_ADDR[10:3]	<b>Memory range lower boundary address bits</b> — The LOW_ADDR[10:3] bits represent bits [10:3] of the global memory address that is used as the lower boundary for the described memory range.

### 4.3.1.9 MPU Descriptor Register 3 (MPUDESC3)

Address: Module Base + 0x0009

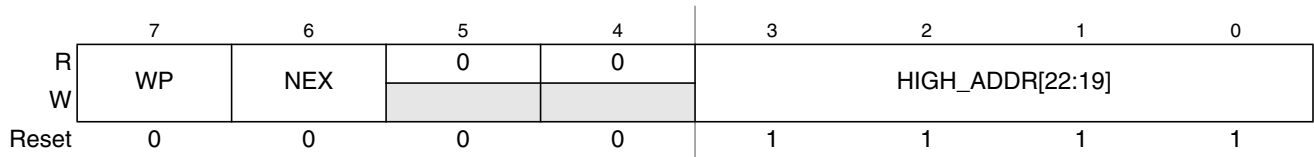


Figure 4-11. MPU Descriptor Register 3 (MPUDESC3)

Read: Anytime

Write: Anytime

Table 4-11. MPUDESC3 Field Descriptions

Field	Description
7 WP	<b>Write-Protect bit</b> — The WP bit causes the described memory range to be treated as write-protected. If this bit is set every attempt to write in the described memory range causes an access violation.

- Provides up to 108 XGATE channels, including 8 software triggered channels
- Interruptible thread execution
- Two register banks to support fast context switching between threads
- Hardware semaphores which are shared between the S12X\_CPU and the XGATE module
- Able to trigger S12X\_CPU interrupts upon completion of an XGATE transfer
- Software error detection to catch erratic application code

### 10.1.3 Modes of Operation

There are four run modes on S12XE devices.

- Run mode, wait mode, stop mode

The XGATE is able to operate in all of these three system modes. Clock activity will be automatically stopped when the XGATE module is idle.

- Freeze mode (BDM active)

In freeze mode all clocks of the XGATE module may be stopped, depending on the module configuration (see [Section 10.3.1.1, “XGATE Control Register \(XGMCTL\)”](#)).

### 10.1.4 Block Diagram

Figure 10-1 shows a block diagram of the XGATE.

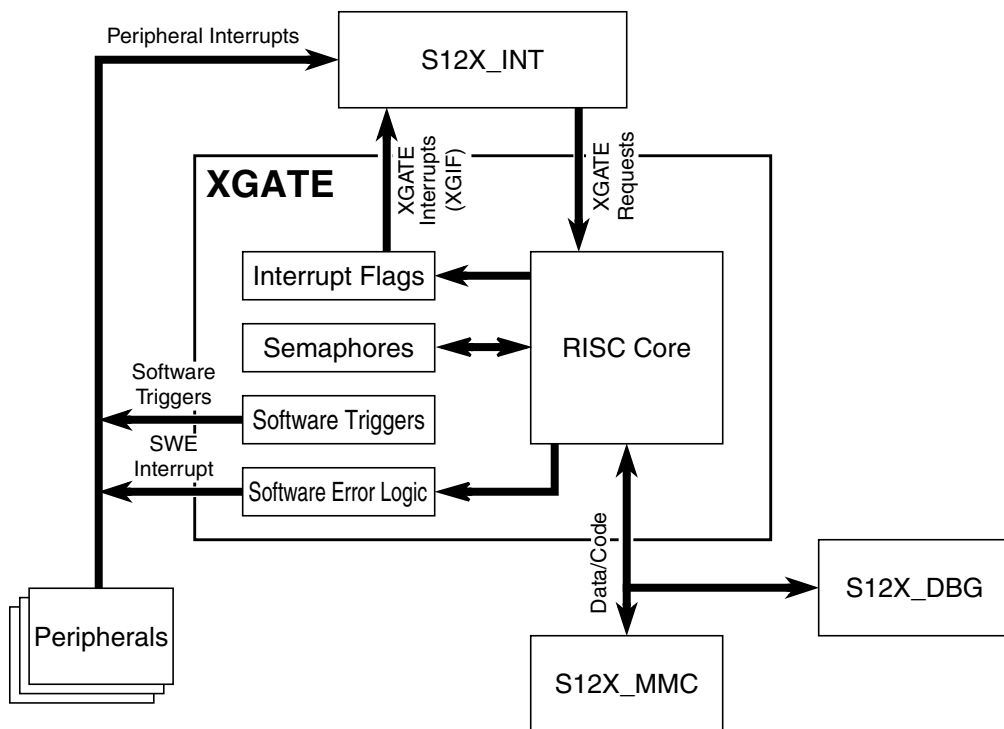


Figure 10-1. XGATE Block Diagram

Table 10-9. XGVBR Field Descriptions

Field	Description
15–1 XBVBR[15:1]	<b>Vector Base Address</b> — The XGVBR register holds the start address of the vector block in the XGATE memory map.

### 10.3.1.8 XGATE Channel Interrupt Flag Vector (XGIF)

The XGATE Channel Interrupt Flag Vector (Figure 10-10) provides access to the interrupt flags of all channels. Each flag may be cleared by writing a "1" to its bit location. Refer to Section 10.5.2, “Outgoing Interrupt Requests” for further information.

Module Base +0x0008

	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
R	0	0	0	0	0	0	0	XGIF_78	XGF_77	XGIF_76	XGIF_75	XGIF_74	XGIF_73	XGIF_72	XGIF_71	XGIF_70
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
R	XGIF_6F	XGIF_6E	XGIF_6D	XGIF_6C	XGIF_6B	XGIF_6A	XGIF_69	XGIF_68	XGF_67	XGIF_66	XGIF_65	XGIF_64	XGIF_63	XGIF_62	XGIF_61	XGIF_60
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
R	XGIF_5F	XGIF_5E	XGIF_5D	XGIF_5C	XGIF_5B	XGIF_5A	XGIF_59	XGIF_58	XGF_57	XGIF_56	XGIF_55	XGIF_54	XGIF_53	XGIF_52	XGIF_51	XGIF_50
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
R	XGIF_4F	XGIF_4E	XGIF_4D	XGIF_4C	XGIF_4B	XGIF_4A	XGIF_49	XGIF_48	XGF_47	XGIF_46	XGIF_45	XGIF_44	XGIF_43	XGIF_42	XGIF_41	XGIF_40
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 10-10. XGATE Channel Interrupt Flag Vector (XGIF)

### 11.4.3.3 Stop Mode

All clocks are stopped in STOP mode, dependent of the setting of the PCE, PRE and PSTP bit. The oscillator is disabled in STOP mode unless the PSTP bit is set. If the PRE or PCE bits are set, the RTI or COP continues to run in Pseudo Stop Mode. In addition to disabling system and core clocks the S12XECRG requests other functional units of the MCU (e.g. voltage-regulator) to enter their individual power saving modes (if available).

If the PLLSEL bit is still set when entering Stop Mode, the S12XECRG will switch the system and core clocks to OSCCLK by clearing the PLLSEL bit. Then the S12XECRG disables the IPLL, disables the core clock and finally disables the remaining system clocks.

If Pseudo Stop Mode is entered from Self-Clock Mode the S12XECRG will continue to check the clock quality until clock check is successful. In this case the IPLL and the voltage regulator (VREG) will remain enabled. If Full Stop Mode (PSTP = 0) is entered from Self-Clock Mode the ongoing clock quality check will be stopped. A complete timeout window check will be started when Stop Mode is left again.

There are two ways to restart the MCU from Stop Mode:

1. Any reset
2. Any interrupt

If the MCU is woken-up from Full Stop Mode by an interrupt and the fast wake-up feature is enabled (FSTWKP=1 and SCME=1), the system will immediately (no clock quality check) resume operation in Self-Clock Mode (see [Section 11.4.1.4, “Clock Quality Checker”](#)). The SCMIF flag will not be set for this special case. The system will remain in Self-Clock Mode with oscillator disabled until FSTWKP bit is cleared. The clearing of FSTWKP will start the oscillator and the clock quality check. If the clock quality check is successful, the S12XECRG will switch all system clocks to oscillator clock. The SCMIF flag will be set. See application examples in [Figure 11-19](#) and [Figure 11-20](#).

Because the IPLL has been powered-down during Stop Mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving Stop-Mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

#### NOTE

In Full Stop Mode or Self-Clock Mode caused by the fast wake-up feature the clock monitor and the oscillator are disabled.

An exception to this is when channels are concatenated. Once concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low order PWME<sub>x</sub> bit. In this case, the high order bytes PWME<sub>x</sub> bits have no effect and their corresponding PWM output lines are disabled.

While in run mode, if all eight PWM channels are disabled (PWME7–0 = 0), the prescaler counter shuts off for power savings.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
W								
Reset	0	0	0	0	0	0	0	0

**Figure 19-3. PWM Enable Register (PWME)**

Read: Anytime

Write: Anytime

**Table 19-2. PWME Field Descriptions**

Field	Description
7 PWME7	<b>Pulse Width Channel 7 Enable</b> 0 Pulse width channel 7 is disabled. 1 Pulse width channel 7 is enabled. The pulse modulated signal becomes available at PWM output bit 7 when its clock source begins its next cycle.
6 PWME6	<b>Pulse Width Channel 6 Enable</b> 0 Pulse width channel 6 is disabled. 1 Pulse width channel 6 is enabled. The pulse modulated signal becomes available at PWM output bit6 when its clock source begins its next cycle. If CON67=1, then bit has no effect and PWM output line 6 is disabled.
5 PWME5	<b>Pulse Width Channel 5 Enable</b> 0 Pulse width channel 5 is disabled. 1 Pulse width channel 5 is enabled. The pulse modulated signal becomes available at PWM output bit 5 when its clock source begins its next cycle.
4 PWME4	<b>Pulse Width Channel 4 Enable</b> 0 Pulse width channel 4 is disabled. 1 Pulse width channel 4 is enabled. The pulse modulated signal becomes available at PWM, output bit 4 when its clock source begins its next cycle. If CON45 = 1, then bit has no effect and PWM output bit4 is disabled.
3 PWME3	<b>Pulse Width Channel 3 Enable</b> 0 Pulse width channel 3 is disabled. 1 Pulse width channel 3 is enabled. The pulse modulated signal becomes available at PWM, output bit 3 when its clock source begins its next cycle.
2 PWME2	<b>Pulse Width Channel 2 Enable</b> 0 Pulse width channel 2 is disabled. 1 Pulse width channel 2 is enabled. The pulse modulated signal becomes available at PWM, output bit 2 when its clock source begins its next cycle. If CON23 = 1, then bit has no effect and PWM output bit2 is disabled.

**Table 23-9. Selectable Autonomous Periodical Interrupt Periods (continued)**

APICLK	APIR[15:0]	Selected Period
1	FFFF	131072 * bus clock period

1. When trimmed within specified accuracy. See electrical specifications for details.

The period can be calculated as follows depending of APICLK:


$$\text{Period} = 2 * (\text{APIR}[15:0] + 1) * 0.1 \text{ ms} \quad \text{or} \quad \text{period} = 2 * (\text{APIR}[15:0] + 1) * \text{bus clock period}$$

### 23.3.2.6 Reserved 06

The Reserved 06 is reserved for test purposes.

0x02F6

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 23-8. Reserved 06**

### 23.3.2.7 High Temperature Trimming Register (VREGHTTR)


The VREGHTTR register allows to trim the VREG temperature sense.

Figure

0x02F7

	7	6	5	4	3	2	1	0
R		0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W	HTOEN							
Reset	0	0	0	0	0 <sup>1</sup>	0 <sup>1</sup>	0 <sup>1</sup>	0 <sup>1</sup>

1. Reset value is either 0 or preset by factory. See Section 1 (Device Overview) for details.

 = Unimplemented or Reserved

**Figure 23-9. VREGHTTR**
**Table 23-10. VREGHTTR field descriptions**

Field	Description
7 HTOEN	<b>High Temperature Offset Enable Bit</b> — If set the temperature sense offset is enabled 0 The temperature sense offset is disabled 1 The temperature sense offset is enabled
3–0 HTTR[3:0]	<b>High Temperature Trimming Bits</b> — See <a href="#">Table 23-11</a> for trimming effects.

**Table 23-11. Trimming Effect**

Bit	Trimming Effect
HTTR[3]	Increases $V_{HT}$ twice of HTTR[2]

**D-Flash Sector** — The D-Flash sector is the smallest portion of the D-Flash memory that can be erased. The D-Flash sector consists of four 64 byte rows for a total of 256 bytes.

**EEE (Emulated EEPROM)** — A method to emulate the small sector size features and endurance characteristics associated with an EEPROM.

**EEE IFR** — Nonvolatile information register located in the D-Flash block that contains data required to partition the D-Flash memory and buffer RAM for EEE. The EEE IFR is visible in the global memory map by setting the EEEIFRON bit in the MMCCTL1 register.

**NVM Command Mode** — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

**Phrase** — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes eight ECC bits for single bit fault correction and double bit fault detection within the phrase.

**P-Flash Memory** — The P-Flash memory constitutes the main nonvolatile memory store for applications.

**P-Flash Sector** — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 1024 bytes.

**Program IFR** — Nonvolatile information register located in the P-Flash block that contains the Device ID, Version ID, and the Program Once field. The Program IFR is visible in the global memory map by setting the PGMIFRON bit in the MMCCTL1 register.

## 25.1.2 Features

### 25.1.2.1 P-Flash Features

- 256 Kbytes of P-Flash memory composed of two 128 Kbyte Flash blocks. The 128 Kbyte Flash blocks are each divided into 128 sectors of 1024 bytes.
- Single bit fault correction and double bit fault detection within a 64-bit phrase during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to program up to one phrase in each P-Flash block simultaneously
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

### 25.1.2.2 D-Flash Features

- Up to 32 Kbytes of D-Flash memory with 256 byte sectors for user access
- Dedicated commands to control access to the D-Flash memory over EEE operation
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Ability to program up to four words in a burst sequence



### 26.4.2.10 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

**Table 26-51. Erase P-Flash Sector Command FCCOB Requirements**

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [22:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to <a href="#">Section 26.1.2.1</a> for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

**Table 26-52. Erase P-Flash Sector Command Error Handling**

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see <a href="#">Table 26-30</a> )
		Set if an invalid global address [22:16] is supplied <sup>(1)</sup>
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
FERSTAT	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
	EPVIOLIF	None

1. As defined by the memory map for FTM512K3.

### 26.4.2.11 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and D-Flash memory space and, if the erase is successful, will release security.

**Table 26-53. Unsecure Flash Command FCCOB Requirements**

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and D-Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security

**Table 27-15. FCNFG Field Descriptions (continued)**

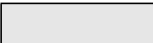
Field	Description
1 FDFD	<b>Force Double Bit Fault Detect</b> — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. The FECCR registers will not be updated during the Flash array read operation with FDFD set unless an actual double bit fault is detected. 0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected 1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see <a href="#">Section 27.3.2.7</a> ) and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see <a href="#">Section 27.3.2.6</a> )
0 FSFD	<b>Force Single Bit Fault Detect</b> — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. The FECCR registers will not be updated during the Flash array read operation with FSFD set unless an actual single bit fault is detected. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see <a href="#">Section 27.3.2.7</a> ) and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see <a href="#">Section 27.3.2.6</a> )

### 27.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

Offset Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	ERSERIE	PGMERIE	0	EPVIOLE	ERSVIE1	ERSVIE0	DFDIE	SFDIE
W								
Reset	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 27-10. Flash Error Configuration Register (FERCNFG)**

All assigned bits in the FERCNFG register are readable and writable.

**Table 27-16. FERCNFG Field Descriptions**

Field	Description
7 ERSERIE	<b>EEE Erase Error Interrupt Enable</b> — The ERSERIE bit controls interrupt generation when a failure is detected during an EEE erase operation. 0 ERSERIF interrupt disabled 1 An interrupt will be requested whenever the ERSERIF flag is set (see <a href="#">Section 27.3.2.8</a> )
6 PGMERIE	<b>EEE Program Error Interrupt Enable</b> — The PGMERIE bit controls interrupt generation when a failure is detected during an EEE program operation. 0 PGMERIF interrupt disabled 1 An interrupt will be requested whenever the PGMERIF flag is set (see <a href="#">Section 27.3.2.8</a> )
4 EPVIOLE	<b>EEE Protection Violation Interrupt Enable</b> — The EPVIOLE bit controls interrupt generation when a protection violation is detected during a write to the buffer RAM EEE partition. 0 EPVIOLIF interrupt disabled 1 An interrupt will be requested whenever the EPVIOLIF flag is set (see <a href="#">Section 27.3.2.8</a> )



Figure 29-4. FTM1024K5 Register Summary (continued)

29.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Offset Module Base + 0x0000

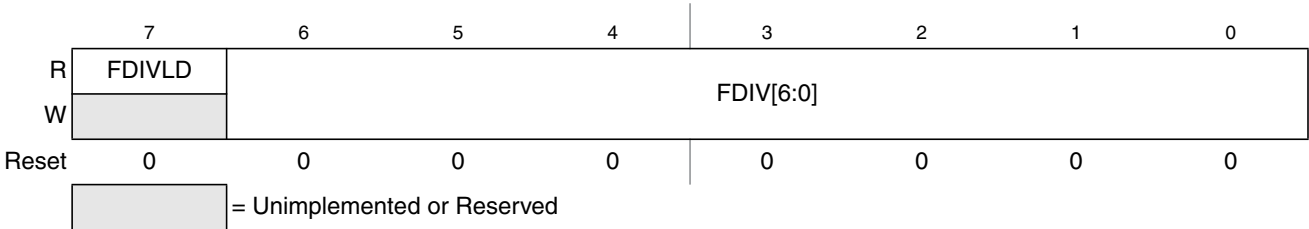


Figure 29-5. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bits 6–0 are write once and bit 7 is not writable.

Table 29-8. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	<b>Clock Divider Loaded</b> 0 FCLKDIV register has not been written 1 FCLKDIV register has been written since the last reset
6–0 FDIV[6:0]	<b>Clock Divider Bits</b> — FDIV[6:0] must be set to effectively divide OSCCLK down to generate an internal Flash clock, FCLK, with a target frequency of 1 MHz for use by the Flash module to control timed events during program and erase algorithms. Table 29-9 shows recommended values for FDIV[6:0] based on OSCCLK frequency. Please refer to Section 29.4.1, “Flash Command Operations,” for more information.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0). The FCLKDIV register is writable during the Flash reset sequence even though CCIF is clear.

**Table 29-32. D-Flash Commands**

FCMD	Command	Function on D-Flash Memory
0x08	Erase All Blocks	Erase all D-Flash (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the EPDIS and EPOPEN bits in the EPROT register are set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x0F	Full Partition D-Flash	Erase the D-Flash block and partition an area of the D-Flash block for user access.
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.
0x13	Enable EEPROM Emulation	Enable EEPROM emulation where writes to the buffer RAM EEE partition will be copied to the D-Flash EEE partition.
0x14	Disable EEPROM Emulation	Suspend all current erase and program activity related to EEPROM emulation but leave current EEE tags set.
0x15	EEPROM Emulation Query	Returns EEE partition and status variables.
0x20	Partition D-Flash	Partition an area of the D-Flash block for user access.

## 29.4.2 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set and the FECCR registers will be loaded with the global address used in the invalid read operation with the data and parity fields set to all 0.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see [Section 29.3.2.7](#)).

**Table 29-68. Program D-Flash Command Error Handling**

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see <a href="#">Table 29-30</a> )
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the global address [22:0] points to an area in the D-Flash EEE partition
		Set if the requested group of words breaches the end of the D-Flash block or goes into the D-Flash EEE partition
	FPVIOL	None
FERSTAT	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
FERSTAT	EPVIOLIF	None

### 29.4.2.18 Erase D-Flash Sector Command

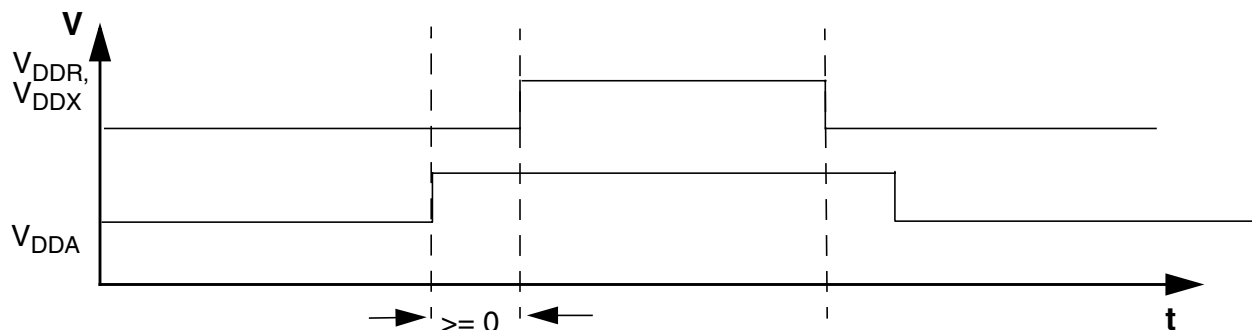
The Erase D-Flash Sector operation will erase all addresses in a sector of the D-Flash user partition.

**Table 29-69. Erase D-Flash Sector Command FCCOB Requirements**

CCOBIX[2:0]	FCCOB Parameters	
000	0x12	Global address [22:16] to identify D-Flash block
001	Global address [15:0] anywhere within the sector to be erased. See <a href="#">Section 29.1.2.2</a> for D-Flash sector size.	

Upon clearing CCIF to launch the Erase D-Flash Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase D-Flash Sector operation has completed.

Figure A-4. MC9S12XE-Family Power Sequencing



During power sequencing  $V_{DDA}$  can be powered up before  $V_{DDR}$ ,  $V_{DDX}$ .  
 $V_{DDR}$  and  $V_{DDX}$  must be powered up together adhering to the operating conditions differential.  
 $V_{RH}$  power up must follow  $V_{DDA}$  to avoid current injection.

## A.6 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for oscillator and phase-locked loop (PLL).

### A.6.1 Startup

Table A-23 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) block description

Table A-23. Startup Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reset input pulse width, minimum input time	$PW_{RSTL}$	2	—	—	$t_{osc}$
2	D	Startup from reset	$t_{RST}$	192	—	4000 <sup>(1)</sup>	$n_{bus}$
3	D	Wait recovery startup time	$t_{WRS}$	—	—	14	$t_{cyc}$
4	D	Fast wakeup from STOP <sup>(2)</sup>	$t_{fws}$	—	50	100	$\mu s$

1. This is the time between RESET deassertion and start of CPU code execution.

2. Including voltage regulator startup;  $V_{DD}/V_{DDF}$  filter capacitors 220 nF,  $V_{DD35} = 5 V$ ,  $T = 25^{\circ}C$

#### A.6.1.1 POR

The release level  $V_{PORR}$  and the assert level  $V_{PORA}$  are derived from the  $V_{DD}$  supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time  $t_{CQOUT}$  no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by  $n_{uposc}$ .

# 0x0240–0x027F Port Integration Module (PIM) Map 5 of 6 (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0248	PTS	R	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		W								
0x0249	PTIS	R	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		W								
0x024A	DDRS	R	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		W								
0x024B	RDRS	R	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		W								
0x024C	PERS	R	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		W								
0x024D	PPSS	R	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		W								
0x024E	WOMS	R	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x024F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0250	PTM	R	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		W								
0x0251	PTIM	R	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		W								
0x0252	DDRM	R	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		W								
0x0253	RDRM	R	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		W								
0x0254	PERM	R	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		W								
0x0255	PPSM	R	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		W								
0x0256	WOMM	R	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		W								
0x0257	MODRR	R	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		W								
0x0258	PTP	R	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		W								
0x0259	PTIP	R	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		W								
0x025A	DDRP	R	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		W								
0x025B	RDRP	R	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		W								
0x025C	PERP	R	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		W								
0x025D	PPSP	R	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		W								
0x025E	PIEP	R	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		W								
0x025F	PIFP	R	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		W								

## 0x0380–0x03BF XGATE Map (Sheet 2 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0396	XGIF	R	XGIF_0F	XGIF_0E	XGIF_0D	XGIF_0C	XGIF_0B	XGIF_0A	XGIF_09	0
0x0397	XGIF	R	0	0	0	0	0	0	0	0
		W								
0x0398	XGSWTM	R	0	0	0	0	0	0	0	0
		W	XGSWTM[7:0]							
0x0399	XGSWT	R	XGSWT[7:0]							
		W								
0x039A	XGSEMM	R	0	0	0	0	0	0	0	0
		W	XGSEMM[7:0]							
0x039B	XGSEM	R	XGSEM[7:0]							
		W								
0x039C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x039D	XGCCR	R	0	0	0	0	XGN	XGZ	XGV	XGC
		W								
0x039E	XGPC (hi)	R	XGPC[15:8]							
		W								
0x039F	XGPC (lo)	R	XGPC[7:0]							
		W								
0x03A0	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03A1	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03A2	XGR1 (hi)	R	XGR1[15:8]							
		W								
0x03A3	XGR1 (lo)	R	XGR1[7:0]							
		W								
0x03A4	XGR2 (hi)	R	XGR2[15:8]							
		W								
0x03A5	XGR2 (lo)	R	XGR2[7:0]							
		W								
0x03A6	XGR3 (hi)	R	XGR3[15:8]							
		W								
0x03A7	XGR3 (lo)	R	XGR3[7:0]							
		W								
0x03A8	XGR4 (hi)	R	XGR4[15:8]							
		W								
0x03A9	XGR4 (lo)	R	XGR4[7:0]							
		W								
0x03AA	XGR5 (hi)	R	XGR5[15:8]							
		W								
0x03AB	XGR5(lo)	R	XGR5[7:0]							
		W								
0x03AC	XGR6 (hi)	R	XGR6[15:8]							
		W								





0x0400–0x07FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0400– 0x07FF	Reserved	R	0	0	0	0	0	0	0	0
		W								