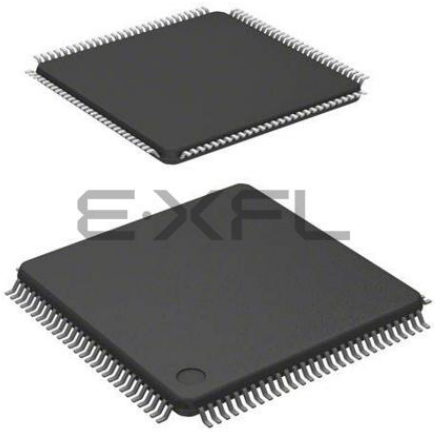

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xet256w1mal

Table 1-5. Derivative Dependent Flash Block Mapping (continued)

Device	0x70_0000	0x74_0000	0x78_0000	0x7A_0000	0x7C_0000	0x7E_0000
9S12XET256 9S12XEA256 (1)	—	—	B1S	—	—	B0(128K)
9S12XEG128 9S12XEA128[1]	—	—	B1S (64K)	—	—	B0 (64K)

1. The 9S12XEA devices are special bondouts for access to extra ADC channels in 80QFP. Available in 80QFP only. WARNING: NOT PIN-COMPATIBLE WITH REST OF FAMILY.

Block B1 is divided into two 128K blocks. The XGATE is always mapped to block B1S.

On the 9S12XEG128 the flash is divided into two 64K blocks B0 and B1S, the B1S range extending from 0x78_0000 to 0x78_FFFF, the B0 range extending from 0x7F_0000 to 0x7F_FFFF.

The block B0 is a reduced size 128K block on the 256K derivative. On the larger derivatives B0 is a 256K block. The block B0 is a reduced size 64K block on the 128K derivative.

1.4.2.4 XGATE Fake Activity Mode

This mode is entered if the CPU executes the STOP instruction when the XGATE is not executing a thread and the XGFACT bit in the XGMCTL register is set. The oscillator remains active and any enabled peripherals continue to function.

1.4.2.5 Wait Mode

This mode is entered when the CPU executes the WAI instruction. In this mode the CPU will not execute instructions. The internal CPU clock is switched off. All peripherals and the XGATE can be active in system wait mode. For further power consumption the peripherals can individually turn off their local clocks. Asserting $\overline{\text{RESET}}$, $\overline{\text{XIRQ}}$, $\overline{\text{IRQ}}$ or any other interrupt that is not masked and is not routed to XGATE ends system wait mode.

1.4.2.6 Run Mode

Although this is not a low-power mode, unused peripheral modules should not be enabled in order to save power.

1.4.3 Freeze Mode

The enhanced capture timer, pulse width modulator, analog-to-digital converters, and the periodic interrupt timer provide a software programmable option to freeze the module status when the background debug module is active. This is useful when debugging application software. For detailed description of the behavior of the ATD0, ATD1, ECT, PWM, and PIT when the background debug module is active consult the corresponding Block Guides.

1.4.4 System States

To facilitate system integrity the MCU can run in Supervisor state or User state. The System States strategy is implemented by additional features on the S12X CPU and a Memory Protection Unit. This is designed to support restricted access for code modules executed by kernels or operating systems supporting access control to system resources.

The current system state is indicated by the U bit in the CPU condition code register. In User state certain CPU instructions are restricted. See the CPU reference guide for details of the U bit and of those instructions affected by User state.

In the case that software task accesses resources outside those defined for it in the MPU a non-maskable interrupt is generated.

1.4.4.1 Supervisor State

This state is intended for configuring the MPU for different tasks that are then executed in User state, returning to Supervisor state on completion of each task. This is the default ’state’ following reset and can be re-entered from User state by an exception (interrupt). If the SVSEN bit in the MPUSEL register of the

Table 2-15. RDRIV Register Field Descriptions (continued)

Field	Description
1 RDPB	**Port B reduced drive**—Select reduced drive for outputs This bit configures the drive strength of all output pins as either full or reduced independent of the function used on the pins. If a pin is used as input this bit has no effect. 1 Reduced drive selected (approx. 1/5 of the full drive strength). 0 Full drive strength enabled.
0 RDPA	**Port A reduced drive**—Select reduced drive for outputs This bit configures the drive strength of all output pins as either full or reduced independent of the function used on the pins. If a pin is used as input this bit has no effect. 1 Reduced drive selected (approx. 1/5 of the full drive strength). 0 Full drive strength enabled.

2.3.15 ECLK Control Register (ECLKCTL)

Address 0x001C (PRR) Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	NECLK	NCLKX2	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
Reset(2):	Mode Depen-dent	1	0	0	0	0	0	0
SS	0	1	0	0	0	0	0	0
ES	1	1	0	0	0	0	0	0
ST	0	1	0	0	0	0	0	0
EX	0	1	0	0	0	0	0	0
NS	1	1	0	0	0	0	0	0
NX	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-13. ECLK Control Register (ECLKCTL)

1. Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.
   Write: Anytime. In emulation modes, write operations will also be directed to the external bus.
2. Reset values in emulation modes are identical to those of the target mode.

2.3.48 Port P Reduced Drive Register (RDRP)

Address 0x025B Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset	0	0	0	0	0	0	0	0

Figure 2-46. Port P Reduced Drive Register (RDRP)

1. Read: Anytime.
   Write: Anytime.

Table 2-44. RDRP Register Field Descriptions

Field	Description
7-0 RDRP	**Port P reduced drive**—Select reduced drive for outputs This register configures the drive strength of output pins 7 through 0 as either full or reduced independent of the function used on the pins. If a pin is used as input this bit has no effect. 1 Reduced drive selected (approx. 1/5 of the full drive strength). 0 Full drive strength enabled.

2.3.49 Port P Pull Device Enable Register (PERP)

Address 0x025C Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Reset	0	0	0	0	0	0	0	0

Figure 2-47. Port P Pull Device Enable Register (PERP)

1. Read: Anytime.
   Write: Anytime.

Table 2-45. PERP Register Field Descriptions

Field	Description
7-0 PERP	**Port P pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset no pull device is enabled. 1 Pull device enabled. 0 Pull device disabled.

Chapter 9
Security (S12XE9SECV2)

Table 9-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.00	27 Aug 2004		- Reviewed and updated for S12XD architecture
V02.01	21 Feb 2007		- Added S12XE, S12XF and S12XS architectures
V02.02	19 Apr 2007		- Corrected statement about Backdoor key access via BDM on XE, XF, XS

9.1 Introduction

This specification describes the function of the security mechanism in the S12XE chip family (9SEC).

NOTE

No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH and/or EEPROM difficult for unauthorized users.

9.1.1 Features

The user must be reminded that part of the security must lie with the application code. An extreme example would be application code that dumps the contents of the internal memory. This would defeat the purpose of security. At the same time, the user may also wish to put a backdoor in the application program. An example of this is the user downloads a security key through the SCI, which allows access to a programming routine that updates parameters stored in another section of the Flash memory.

The security features of the S12XE chip family (in secure mode) are:

- Protect the content of non-volatile memories (Flash, EEPROM)
- Execution of NVM commands is restricted
- Disable access to internal memory via background debug module (BDM)
- Disable access to internal Flash/EEPROM in expanded modes
- Disable debugging features for the CPU and XGATE

ASR — Arithmetic Shift Right — ASR

Operation

n = RS or IMM4

Shifts the bits in register RD *n* positions to the right. The higher *n* bits of the register RD become filled with the sign bit (RD[15]). The carry flag will be updated to the bit contained in RD[n-1] before the shift for *n* > 0.

n can range from 0 to 16.

In immediate address mode, *n* is determined by the operand IMM4. *n* is considered to be 16 if IMM4 is equal to 0.

In dyadic address mode, *n* is determined by the content of RS. *n* is considered to be 16 if the content of RS is greater than 15.

CCR Effects

N	Z	V	C
Δ	Δ	Δ	Δ

N: Set if bit 15 of the result is set; cleared otherwise.

Z: Set if the result is $0000; cleared otherwise.

V: Set if a two´s complement overflow resulted from the operation; cleared otherwise.
$RD[15]_{old}$ ^ $RD[15]_{new}$

C: Set if *n* > 0 and RD[n-1] = 1; if n = 0 unaffected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code												Cycles
ASR RD, #IMM4	IMM4	0	0	0	0	1	RD	IMM4		1	0	0	1	P
ASR RD, RS	DYA	0	0	0	0	1	RD	RS	1	0	0	0	1	P

Table 14-29. Delay Counter Select Examples when PRNT = 1

DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0	Delay
0	0	0	0	0	1	1	1	32 bus clock cycles
0	0	0	0	1	1	1	1	64 bus clock cycles
0	0	0	1	1	1	1	1	128 bus clock cycles
0	0	1	1	1	1	1	1	256 bus clock cycles
0	1	1	1	1	1	1	1	512 bus clock cycles
1	1	1	1	1	1	1	1	1024 bus clock cycles

14.3.2.23 Input Control Overwrite Register (ICOVW)

Module Base + 0x002A

	7	6	5	4	3	2	1	0
R W	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
Reset	0	0	0	0	0	0	0	0

Figure 14-46. Input Control Overwrite Register (ICOVW)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 14-30. ICOVW Field Descriptions

Field	Description
7:0 NOVW[7:0]	**No Input Capture Overwrite** 0 The contents of the related capture register or holding register can be overwritten when a new input capture or latch occurs. 1 The related capture register or holding register cannot be written by an event unless they are empty (see Section 14.4.1.1, “IC Channels”). This will prevent the captured value being overwritten until it is read or latched in the holding register.

14.3.2.24 Input Control System Control Register (ICSYS)

Module Base + 0x002B

	7	6	5	4	3	2	1	0
R W	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
Reset	0	0	0	0	0	0	0	0

Figure 14-47. Input Control System Register (ICSYS)

Read: Anytime

Write: Once in normal modes

Table 17-5. PITMUX Field Descriptions

Field	Description
7:0 PMUX[7:0]	**PIT Multiplex Bits for Timer Channel 7:0** — These bits select if the corresponding 16-bit timer is connected to micro time base 1 or 0. If PMUX is modified, the corresponding 16-bit timer is immediately switched to the other micro time base. 0 The corresponding 16-bit timer counts with micro time base 0. 1 The corresponding 16-bit timer counts with micro time base 1.

17.3.0.5 PIT Interrupt Enable Register (PITINTE)

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	PINTE7	PINTE6	PINTE5	PINTE4	PINTE3	PINTE2	PINTE1	PINTE0
Reset	0	0	0	0	0	0	0	0

Figure 17-7. PIT Interrupt Enable Register (PITINTE)

Read: Anytime

Write: Anytime

Table 17-6. PITINTE Field Descriptions

Field	Description
7:0 PINTE[7:0]	**PIT Time-out Interrupt Enable Bits for Timer Channel 7:0** — These bits enable an interrupt service request whenever the time-out flag PTF of the corresponding PIT channel is set. When an interrupt is pending (PTF set) enabling the interrupt will immediately cause an interrupt. To avoid this, the corresponding PTF flag has to be cleared first. 0 Interrupt of the corresponding PIT channel is disabled. 1 Interrupt of the corresponding PIT channel is enabled.

17.3.0.6 PIT Time-Out Flag Register (PITTF)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R W	PTF7	PTF6	PTF5	PTF4	PTF3	PTF2	PTF1	PTF0
Reset	0	0	0	0	0	0	0	0

Figure 17-8. PIT Time-Out Flag Register (PITTF)

Read: Anytime

Write: Anytime (write to clear)

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000F PITCNT1 (Low)	R	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
	W								
0x0010 PITLD2 (High)	R	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
	W								
0x0011 PITLD2 (Low)	R	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
	W								
0x0012 PITCNT2 (High)	R	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8
	W								
0x0013 PITCNT2 (Low)	R	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
	W								
0x0014 PITLD3 (High)	R	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
	W								
0x0015 PITLD3 (Low)	R	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
	W								
0x0016 PITCNT3 (High)	R	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8
	W								
0x0017 PITCNT3 (Low)	R	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
	W								
0x0018–0x0027 RESERVED	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 18-2. PIT Register Summary (Sheet 2 of 2)

18.3.0.1 PIT Control and Force Load Micro Timer Register (PITCFLMT)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	PITE	PITSWAI	PITFRZ	0	0	0	0	0
W							PFLMT1	PFLMT0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-3. PIT Control and Force Load Micro Timer Register (PITCFLMT)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Write: Anytime (any value written causes PWM counter to be reset to $00).

19.3.2.13 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

See Section 19.4.2.3, “PWM Period and Duty” for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)
- PWMx Period = Channel Clock Period * PWMPERx Center Aligned Output (CAEx = 1)

  PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 19.4.2.8, “PWM Boundary Cases”.

Module Base + 0x0014 = PWMPER0, 0x0015 = PWMPER1, 0x0016 = PWMPER2, 0x0017 = PWMPER3
Module Base + 0x0018 = PWMPER4, 0x0019 = PWMPER5, 0x001A = PWMPER6, 0x001B = PWMPER7

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 19-15. PWM Channel Period Registers (PWMPERx)

Read: Anytime

Write: Anytime

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 22-3. CFORC Field Descriptions

Field	Description
7:0 FOC[7:0]	**Force Output Compare Action for Channel 7:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. **Note:** A channel 7 event, which can be a counter overflow when TTOV[7] is set or a successful output compare on channel 7, overrides any channel 6:0 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

22.3.2.3 Output Compare 7 Mask Register (OC7M)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
Reset	0	0	0	0	0	0	0	0

Figure 22-8. Output Compare 7 Mask Register (OC7M)

Read: Anytime

Write: Anytime

Table 22-4. OC7M Field Descriptions

Field	Description
7:0 OC7M[7:0]	**Output Compare 7 Mask** — A channel 7 event, which can be a counter overflow when TTOV[7] is set or a successful output compare on channel 7, overrides any channel 6:0 compares. For each OC7M bit that is set, the output compare action reflects the corresponding OC7D bit. 0 The corresponding OC7Dx bit in the output compare 7 data register will not be transferred to the timer port on a channel 7 event, even if the corresponding pin is setup for output compare. 1 The corresponding OC7Dx bit in the output compare 7 data register will be transferred to the timer port on a channel 7 event. **Note:** The corresponding channel must also be setup for output compare (IOSx = 1 and OCPDx = 0) for data to be transferred from the output compare 7 data register to the timer port.

Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 25-45. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

Table 25-46. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 25-30)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed(1)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
FERSTAT	EPVIOLIF	None

1. If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

25.4.2.8 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and D-Flash memory space including the EEE nonvolatile information register.

26.4.1.3 Valid Flash Module Commands

Table 26-30. Flash Commands by Mode

FCMD	Command	Unsecured				Secured			
		NS (1)	NX (2)	SS(3)	ST(4)	NS (5)	NX (6)	SS(7)	ST(8)
0x01	Erase Verify All Blocks	*	*	*	*	*	*	*	*
0x02	Erase Verify Block	*	*	*	*	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	*	*			
0x04	Read Once	*	*	*	*	*			
0x05	Load Data Field	*	*	*	*	*			
0x06	Program P-Flash	*	*	*	*	*			
0x07	Program Once	*	*	*	*	*			
0x08	Erase All Blocks			*	*			*	*
0x09	Erase P-Flash Block	*	*	*	*	*			
0x0A	Erase P-Flash Sector	*	*	*	*	*			
0x0B	Unsecure Flash			*	*			*	*
0x0C	Verify Backdoor Access Key	*				*			
0x0D	Set User Margin Level	*	*	*	*	*			
0x0E	Set Field Margin Level			*	*				
0x0F	Full Partition D-Flash			*	*				
0x10	Erase Verify D-Flash Section	*	*	*	*	*			
0x11	Program D-Flash	*	*	*	*	*			
0x12	Erase D-Flash Sector	*	*	*	*	*			
0x13	Enable EEPROM Emulation	*	*	*	*	*	*	*	*
0x14	Disable EEPROM Emulation	*	*	*	*	*	*	*	*
0x15	EEPROM Emulation Query	*	*	*	*	*	*	*	*
0x20	Partition D-Flash	*	*	*	*	*	*	*	*

1. Unsecured Normal Single Chip mode.
2. Unsecured Normal Expanded mode.
3. Unsecured Special Single Chip mode.
4. Unsecured Special Mode.
5. Secured Normal Single Chip mode.
6. Secured Normal Expanded mode.
7. Secured Special Single Chip mode.
8. Secured Special Mode.

Table 29-6. EEE Resource Fields

Global Address	Size (Bytes)	Description
0x10_0000 – 0x10_7FFF	32,768	D-Flash Memory (User and EEE)
0x10_8000 – 0x11_FFFF	98,304	Reserved
0x12_0000 – 0x12_007F	128	EEE Nonvolatile Information Register (EEEIFRON[(1)] = 1)
0x12_0080 – 0x12_0FFF	3,968	Reserved
0x12_1000 – 0x12_1EFF	3,840	Reserved
0x12_1F00 – 0x12_1FFF	256	EEE Tag RAM (TMGRAMON[1] = 1)
0x12_2000 – 0x12_3BFF	7,168	Reserved
0x12_3C00 – 0x12_3FFF	1,024	Memory Controller Scratch RAM (TMGRAMON[1] = 1)
0x12_4000 – 0x12_DFFF	40,960	Reserved
0x12_E000 – 0x12_FFFF	8,192	Reserved
0x13_0000 – 0x13_EFFF	61,440	Reserved
0x13_F000 – 0x13_FFFF	4,096	Buffer RAM (User and EEE)

1. MMCCTL1 register bit

- Program a duplicate DFPART to the EEE nonvolatile information register at global address 0x12_0002 (see Table 29-7)
- Program ERPART to the EEE nonvolatile information register at global address 0x12_0004 (see Table 29-7)
- Program a duplicate ERPART to the EEE nonvolatile information register at global address 0x12_0006 (see Table 29-7)

The D-Flash user partition will start at global address 0x10_0000. The buffer RAM EEE partition will end at global address 0x13_FFFF. After the Partition D-Flash operation has completed, the CCIF flag will set.

Running the Partition D-Flash command a second time will result in the ACCERR bit within the FSTAT register being set. The data value written corresponds to the number of 256 byte sectors allocated for either direct D-Flash access (DFPART) or buffer RAM EEE access (ERPART).

Table 29-78. Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 29-30)
		Set if partitions have already been defined
		Set if an invalid DFPART or ERPART selection is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

This section describes the characteristics of all I/O pins except EXTAL, XTAL, TEST and supply pins.

Table A-7. 3.3-V I/O Characteristics

Conditions are 3.13 V < V_{DD35} < 3.6 V temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input high voltage	V_{IH}	0.65*V_{DD35}	—	—	V
	T	Input high voltage	V_{IH}	—	—	V_{DD35} + 0.3	V
2	P	Input low voltage	V_{IL}	—	—	0.35*V_{DD35}	V
	T	Input low voltage	V_{IL}	V_{SS35} – 0.3	—	—	V
3	T	Input hysteresis	V_{HYS}	—	250	—	mV
4a	P	Input leakage current (pins in high impedance input mode)[1] V_{in} = V_{DD35} or V_{SS35} **M** Temperature range -40°C to 150°C **V** Temperature range -40°C to 130°C **C** Temperature range -40°C to 110°C	I_{in}	 –1 –0.75 –0.5	 — — —	 1 0.75 0.5	µA
4b	C	Input leakage current (pins in high impedance input mode) V_{in} = V_{DD35} or V_{SS35} -40°C 27°C 70°C 85°C 100°C 105°C 110°C 120°C 125°C 130°C 150°C	I_{in}	—	— — ±1 ±1 ±8 ±14 ±26 ±32 40 ±60 ±74 ±92 ±240	—	nA
5	C	Output high voltage (pins in output mode) Partial drive I_{OH} = –0.75 mA	V_{OH}	V_{DD35} – 0.4	—	—	V
6	P	Output high voltage (pins in output mode) Full drive I_{OH} = –4 mA	V_{OH}	V_{DD35} – 0.4	—	—	V
7	C	Output low voltage (pins in output mode) Partial Drive I_{OL} = +0.9 mA	V_{OL}	—	—	0.4	V
8	P	Output low voltage (pins in output mode) Full Drive I_{OL} = +4.75 mA	V_{OL}	—	—	0.4	V
9	P	Internal pull up resistance V_{IH} min > input voltage > V_{IL} max	R_{PUL}	25	—	50	KΩ
10	P	Internal pull down resistance V_{IH} min > input voltage > V_{IL} max	R_{PDH}	25	—	50	KΩ
11	D	Input capacitance	C_{in}	—	6	—	pF
12	T	Injection current[2] Single pin limit Total device limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA
13	D	Port H, J, P interrupt input pulse filtered (STOP)[3]	t_{PULSE}	—	—	3	µs

Table A-10. Module Configurations for Typical Run Supply Current V_{DD35}=5V

Peripheral	Configuration
S12XCPU	420 cycle loop: 384 DBNE cycles plus subroutine entry to stimulate stacking (RAM access)
XGATE	XGATE fetches code from RAM, XGATE runs in an infinite loop, reading the Status and Flag registers of CAN's, SPI's, SCI's in sequence and doing some bit manipulation on the data
MSCAN	Configured to loop-back mode using a bit rate of 500kbit/s
SPI	Configured to master mode, continuously transmit data (0x55 or 0xAA) at 2Mbit/s
SCI	Configured into loop mode, continuously transmit data (0x55) at speed of 19200 baud
IIC	Operate in master mode and continuously transmit data (0x55 or 0xAA) at 100Kbit/s
PWM	Configured to toggle its pins at the rate of 1kHz
ECT	The peripheral shall be configured in output compare mode. Pulse accumulator and modulus counter enabled.
ATD	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.
PIT	PIT is enabled, Micro-timer register 0 and 1 loaded with $0F and timer registers 0 to 3 are loaded with $03/07/0F/1F.
RTI	Enabled with RTI Control Register (RTICTL) set to $59
Overhead	VREG supplying 1.8V from a 5V input voltage, core clock tree active, PLL on

Table A-11. Module Configurations for Maximum Run Supply Current V_{DD35}=5.5V

Peripheral	Configuration
S12XCPU	420 cycle loop: 384 DBNE cycles plus subroutine entry to stimulate stacking (RAM access)
XGATE	XGATE fetches code from RAM, XGATE runs in an infinite loop, reading the Status and Flag registers of CAN's, SPI's, SCI's in sequence and doing some bit manipulation on the data
MSCAN	Configured to loop-back mode using a bit rate of 1Mbit/s
SPI	Configured to master mode, continuously transmit data (0x55 or 0xAA) at 4Mbit/s
SCI	Configured into loop mode, continuously transmit data (0x55) at speed of 57600 baud
IIC	Operate in master mode and continuously transmit data (0x55 or 0xAA) at 100Kbit/s
PWM	Configured to toggle its pins at the rate of 40kHz
ECT	The peripheral shall be configured in output compare mode. Pulse accumulator and modulus counter enabled.
ATD	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.
Overhead	VREG supplying 1.8V from a 5V input voltage, PLL on

Table D-2. Peripheral Options of MC9S12XE-Family Members

Device	Package	XGATE	CAN	SCI	SPI	IIC	ECT	TIM[1]	PIT	A/D	I/O
9S12XEP100	208 MAPBGA	yes	5	8	3	2	8ch	8ch	8ch	2/32	152
	144LQFP		5	8	3	2	8ch	8ch	8ch	2/24	119
	112LQFP		5	8	3	1	8ch	8ch	8ch	2/16[2]	91
9S12XEP768	208 MAPBGA		5	8	3	2	8ch	8ch	8ch	2/32	152
	144LQFP		5	8	3	2	8ch	8ch	8ch	2/24	119
	112LQFP		5	8	3	1	8ch	8ch	8ch	2/16 (2)	91
9S12XEQ512	144LQFP		4	6	3	2	8ch	0	4ch	2/24	119
	112LQFP		4	6	3	1	8ch	0	4ch	2/16[2]	91
	80QFP		4	2	3	1	8ch	0	4ch	2/8[2]	59
9S12XEQ384	144LQFP		4	6	3	2	8ch	0	4ch	2/24	119
	112LQFP		4	6	3	1	8ch	0	4ch	2/16[2]	91
	80QFP		4	2	3	1	8ch	0	4ch	2/8[2]	59
9S12XEG384	144LQFP		2	6	3	2	8ch	0	4ch	2/24	119
	112LQFP		2	6	3	1	8ch	0	4ch	2/16[2]	91
	80QFP		2	2	3	1	8ch	0	4ch	2/8[2]	59
9S12XES384	144LQFP	no	1	2	1	2	8ch	0	4ch	2/24	119
	112LQFP		1	2	1	1	8ch	0	4ch	2/16[2]	91
	80QFP		1	2	1	1	8ch	0	4ch	2/8[2]	59
9S12XET256	144LQFP	yes	3	4	3	1	8ch	0	4ch	2/24	119
	112LQFP		3	4	3	1	8ch	0	4ch	2/16[2]	91
	80QFP		3	2	3	1	8ch	0	4ch	2/8[2]	59
9S12XEA256 (3)	80QFP		3	2	3	1	8ch	0	4ch	2/12[2]	59
9S12XEG256	112LQFP		2	4	3	1	8ch	0	4ch	2/16[2]	91
9S12XEG128	112LQFP		2	2	2	1	8ch	0	2ch	1/16	91
	80QFP		2	2	2	1	8ch	0	2ch	1/8	59
9S12XEA128[3]	80QFP		2	2	2	1	8ch	0	2ch	2/12[2]	59

1. TIM available via rerouting on EP100,EP768 devices 112/144 pinout options.
   TIM not available on EG128,ET256,EA256, EQ384,EQ512 devices.
2. The device features 2 16-channel ATD modules, only one of which is bonded out in this package option
3. This is a special bondout for access to extra ADC channels in 80QFP.
   WARNING: NOT PIN-COMPATIBLE WITH REST OF FAMILY.
   The 9S12XET256/9S12XEG128 use the standard 80QFP bondouts, compatible with other family members.

0x0180–0x01BF MSCAN (CAN1) Map (Sheet 2 of 2)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0196	CAN1IDMR2	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0197	CAN1IDMR3	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0198	CAN1IDAR4	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0199	CAN1IDAR5	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x019A	CAN1IDAR6	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x019B	CAN1IDAR7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x019C	CAN1IDMR4	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x019D	CAN1IDMR5	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x019E	CAN1IDMR6	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x019F	CAN1IDMR7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x01A0–0x01AF	CAN1RXFG	R	FOREGROUND RECEIVE BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								
0x01B0–0x01BF	CAN1TXFG	R	FOREGROUND TRANSMIT BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								

0x01C0–0x01FF MSCAN (CAN2) Map (Sheet 1 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01C0	CAN2CTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x01C1	CAN2CTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		W								
0x01C2	CAN2BTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x01C3	CAN2BTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x01C4	CAN2RFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x01C5	CAN2RIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x01C6	CAN2TFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x01C7	CAN2TIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								

0x0200–0x023F MSCAN (CAN3) (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0216	CAN3IDMR2	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0217	CAN3IDMR3	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0218	CAN3IDAR4	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0219	CAN3IDAR5	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x021A	CAN3IDAR6	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x021B	CAN3IDAR7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x021C	CAN3IDMR4	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x021D	CAN3IDMR5	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x021E	CAN3IDMR6	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x021F	CAN3IDMR7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0220–0x022F	CAN3RXFG	R	FOREGROUND RECEIVE BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								
0x0230–0x023F	CAN3TXFG	R	FOREGROUND TRANSMIT BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								

0x0240–0x027F Port Integration Module (PIM) Map 5 of 6

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x0241	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x0242	DDRT	R	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x0243	RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		W								
0x0244	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0245	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0246	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0247	Reserved	R	0	0	0	0	0	0	0	0
		W								