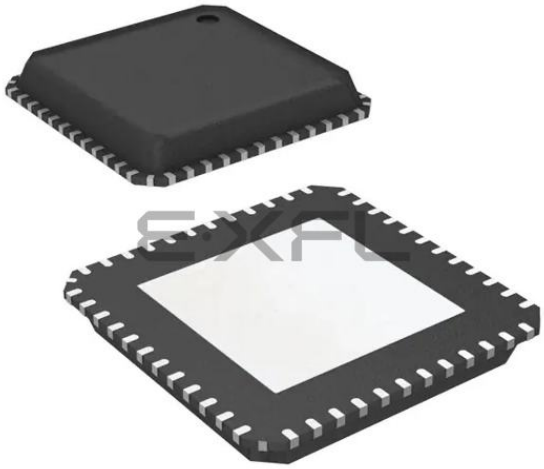

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 175°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9867qxw20xuma1

2 Block Diagram

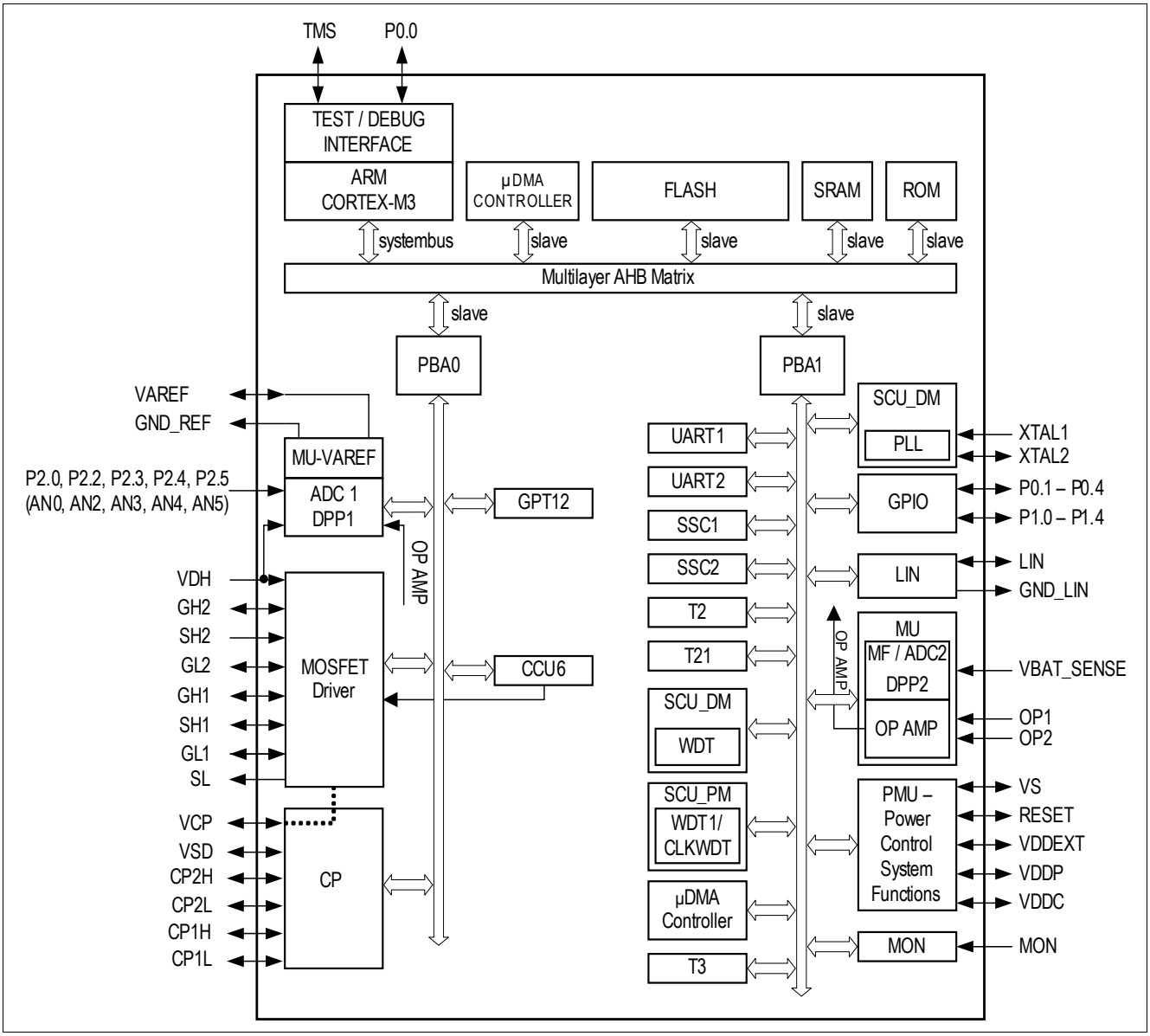

Figure 1 Block Diagram

- f_{MI_CLK} Measurement interface clock
- f_{TFILT_CLK} Analog module filter clock
- LP_CLK Clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- NMI (Non-Maskable Interrupt)
- INTISR<15,13:4,1,0> External interrupt signals

RCU (Reset Control Unit)

- PMU_1V5DidPOR Undervoltage reset of power down supply
- PMU_PIN Reset generated by reset pin
- PMU_ExtWDT WDT1 reset
- PMU_IntWDT WDT (SCU) reset
- PMU_SOFT Software reset
- PMU_Wake Sleep Mode/Stop Mode exit with reset
- RESET_TYPE_3 Peripheral reset (contains all resets)
- RESET_TYPE_4 Peripheral reset (without SOFT and WDT reset)

Port Control

- P0_POCONy.PDMx driver strength control
- P1_POCONy.PDMx driver strength control

MISC Control

- MODPISELx Mode selection registers for UART (source section) and Timer (trigger or count selection)

6.3 Clock Generation Unit

The Clock Generation Unit (CGU) enables a flexible clock generation for TLE9867QXW20. During user program execution, the frequency can be modified to optimize the performance/power consumption ratio, allowing power consumption to be adapted to the actual application state.

The CGU in the TLE9867QXW20 consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module with an internal oscillator (OSC_PLL), and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated from of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

Table 5 External CAP Capacitors

Fundamental Mode Crystal Frequency (approx., MHz)	Load Caps C_1, C_2 (pF)
4	33
8	18
12	12
16	10
20	10
25	8

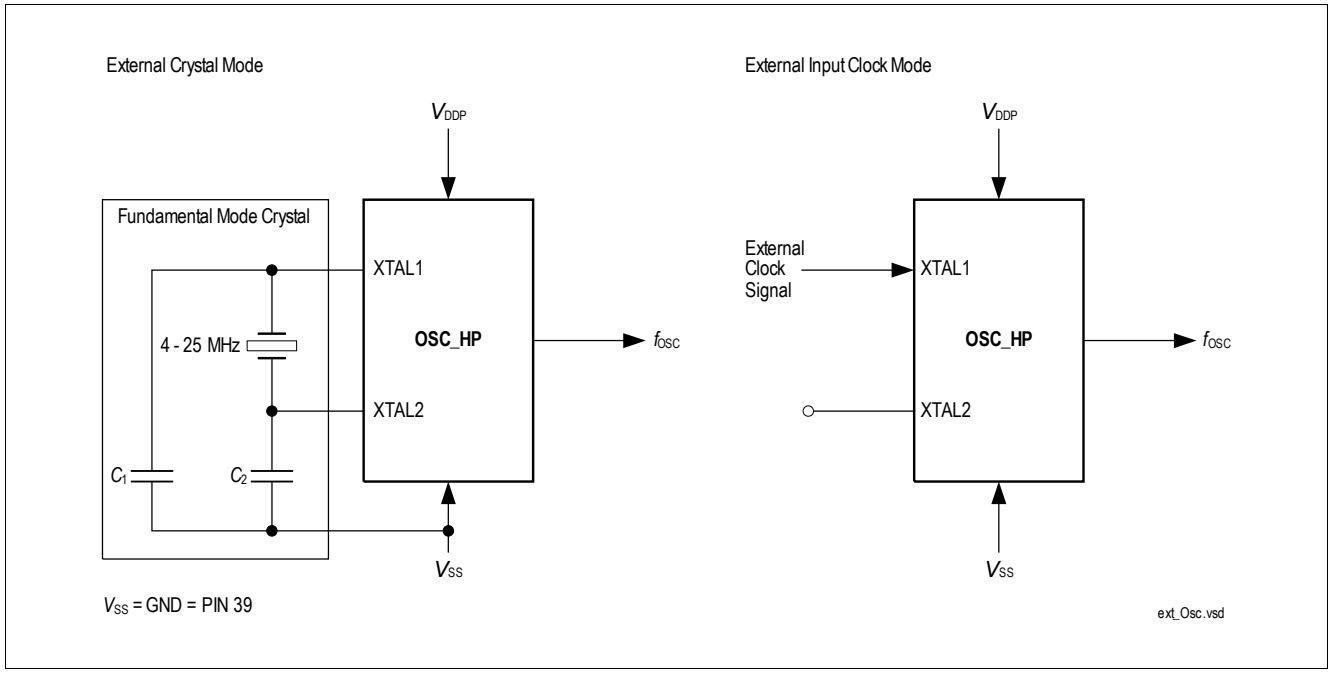

Figure 10 TLE9867QXW20 External Circuitry for the OSC_HP

WDT1 (System Watchdog)

- LP_CLK clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI supply prewarning NMI request
- PREWARN_SUP_INT supply prewarning interrupt
- grouping of peripheral interrupts for external interupt nodes:
  - grouping single peripheral interrupts for interrupt node INT<2> (Measurement Unit (MU))
  - grouping single peripheral interrupts for interrupt node INT<3> (ADC1-VAREF)
  - grouping single peripheral interrupts for interrupt node INT<10> (UART1-LIN Transceiver)
  - grouping single peripheral interrupts for interrupt node INT<14> (Bridge Driver)

8 ARM Cortex-M3 Core

8.1 Features

The key features of the Cortex-M3 implemented are listed below.

Processor Core; a low gate count core, with low latency interrupt processing:

- A subset of the Thumb®-2 Instruction Set
- Banked stack pointer (SP) only
- 32-bit hardware divide instructions, SDIV and UDIV (Thumb-2 instructions)
- Handler and Thread Modes
- Thumb and debug states
- Interruptible-continued instructions LDM/STM, Push/Pop for low interrupt latency
- Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
- ARM architecture v7-M Style BE8/LE support
- ARMv6 unaligned accesses

Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing:

- Interrupts, configurable from 1 to 16
- Bits of priority (4)
- Dynamic reprioritization of interrupts
- Priority grouping. This enables selection of preemptive interrupt levels and non-preemptive interrupt levels
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

Bus interfaces

- Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, DCode, and System bus interface
- Memory access alignment
- Write buffer for buffering of write data

9.3 Functional Description

9.3.1 DMA Mode Overview

The DMA controller implements the following 13 hardware DMA requests:

- ADC1 complete sequence 1 done: DMA transfer is requested on completion of the ADC1 channel conversion sequence.
- ADC1 exceptional sequence 2 (ESM) done: DMA transfer is requested on completion of the ADC1 conversion sequence triggered by an exceptional measurement request.
- SSC1/2 transmit byte: DMA transfer is requested upon the completion of data transmission via SSC1/2
- SSC1/2: receive byte: DMA transfer is requested upon the completion of data reception via SSC1/2.
- ADC1 channel 0 conversion done: DMA transfer is requested on completion of the ADC1 channel 0 conversion.
- ADC1 channel 1 conversion done: DMA transfer is requested on completion of the ADC1 channel 1 conversion.
- ADC1 channel 2 conversion done: DMA transfer is requested on completion of the ADC1 channel 2 conversion.
- ADC1 channel 3 conversion done: DMA transfer is requested on completion of the ADC1 channel 3 conversion.
- ADC1 channel 4 conversion done: DMA transfer is requested on completion of the ADC1 channel 4 conversion.
- ADC1 channel 5 conversion done: DMA transfer is requested on completion of the ADC1 channel 5 conversion.
- ADC1 channel 6 conversion done: DMA transfer is requested on completion of the ADC1 channel 6 conversion.
- ADC1 channel 7 conversion done: DMA transfer is requested on completion of the ADC1 channel 7 conversion.
- Timer3 ccu6_int: DMA transfer is requested following a timer trigger.

12 Interrupt System

12.1 Features

- Up to 16 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 16 interrupt nodes

12.2 Introduction

Before enabling an interrupt, all corresponding interrupt status flags should be cleared.

12.2.1 Overview

The TLE9867QXW20 supports 16 interrupt vectors with 16 priority levels. Fifteen of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC, CCU6, DMA, Bridge Driver and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 6 Interrupt Vector Table

Service Request	Node ID	Description
GPT12	0/1	GPT interrupt (T2-T6, CAPIN)
MU- ADC8/T3	2	Measurement Unit, VBG, Timer3
ADC1	3	ADC1 interrupt / VREF5V Overload / VREF5V OV/UV, 10-bit ADC
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 (ASC-LIN) interrupt (receive, transmit), Timer2, linsync1, LIN
UART2	11	UART2 interrupt (receive, transmit), Timer21, External interrupt (EINT2)
EXINT0	12	External interrupt (EINT0), MON
EXINT1	13	External interrupt (EINT1)
BDRV/CP	14	Bridge Driver / Charge Pump
DMA	15	DMA Controller

Table 7 NMI Interrupt Table

Service Request	Node	Description
Watchdog Timer NMI	NMI	Watchdog Timer overflow
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature

Table 8 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.2	Input	GPI	P0_DATA.P2	
		INP1	CCPOS2_1	CCU6
		INP2	T2EUDA	GPT12T2
		INP3	MTSR_1	SSC1
		INP4	T21EX_0	Timer 21
		INP5	T6INA	GPT12T6
	Output	GPO	P0_DATA.P2	–
		ALT1	COUT60_0	CCU6
		ALT2	MTSR_1	SSC1
		ALT3	EXF2_0	Timer 2
P0.3	Input	GPI	P0_DATA.P3	
		INP1	SCK_1	SSC1
		INP2	CAPINB	GPT12
		INP3	T5INA	GPT12T5
		INP4	T4EUDA	GPT12T4
		INP5	CCPOS0_1	CCU6
	Output	GPO	P0_DATA.P3	
		ALT1	SCK_1	SSC1
		ALT2	EXF21_2	Timer 21
		ALT3	T6OUT	GPT12T6
P0.4	Input	GPI	P0_DATA.P4	
		INP1	MRST_1_0	SSC1
		INP2	CC60_0	CCU6
		INP3	T21_2	Timer 21
		INP4	EXINT2_2	SCU
		INP5	T3EUDA	GPT12T3
		INP6	CCPOS1_1	CCU6
	Output	GPO	P0_DATA.P4	
		ALT1	MRST_1_0	SSC1
		ALT2	CC60_0	CCU6
		ALT3	CLKOUT_0	SCU

16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode

16.2 Introduction

The timer modules are general-purpose 16-bit timers. Timer 2/21 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{PCLK}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{PCLK}/24$ (if prescaler is disabled).

16.2.1 Timer2 and Timer21 Modes Overview

Table 11 Timer2 and Timer21 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated by reload or capture events

19 UART1/UART2

19.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch byte detection

19.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

19.2.1 Block Diagram

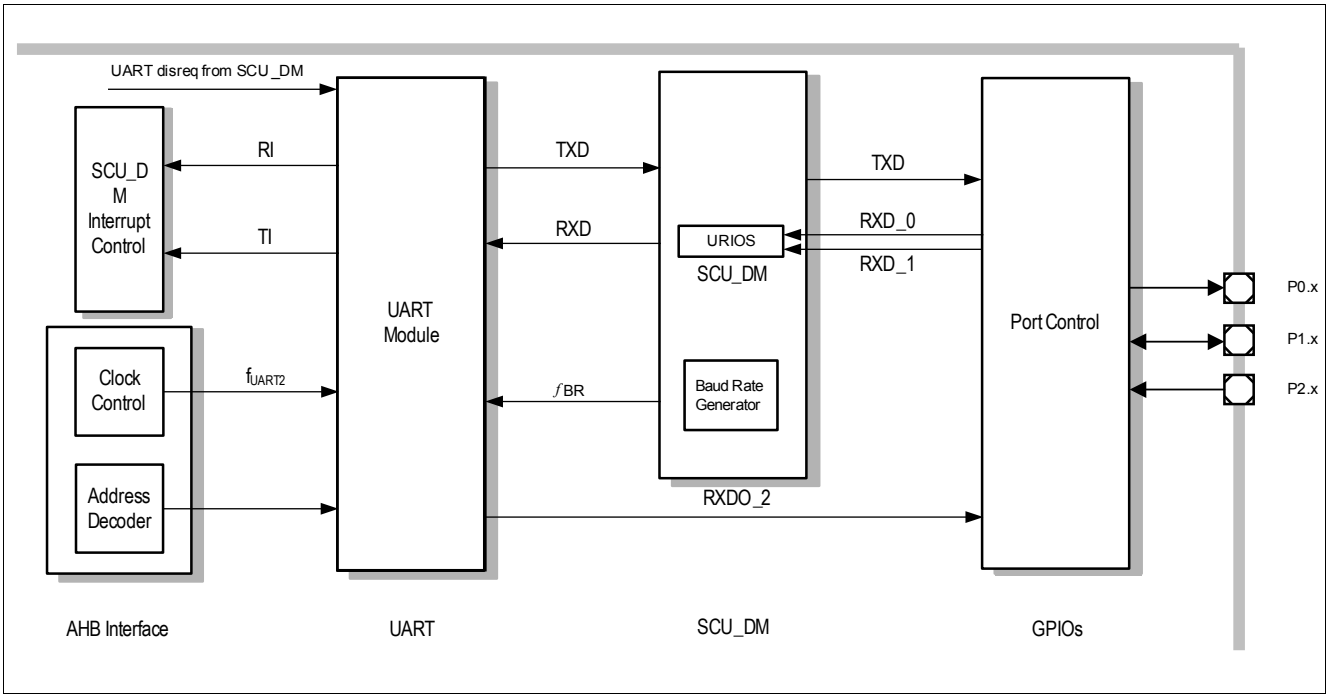

Figure 22 UART Block Diagram

19.3 UART Modes

The UART can be used in four different modes. In mode 0, it operates as an 8-bit shift register. In mode 1, it operates as an 8-bit serial port. In modes 2 and 3, it operates as a 9-bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting bits SM0 and SM1 to their corresponding values, as shown in Table 13.

Table 13 UART Modes

SM0	SM1	Operating Mode	Baud Rate
0	0	Mode 0: 8-bit shift register	$f_{PCLK}/2$
0	1	Mode 1: 8-bit shift UART	Variable
1	0	Mode 2: 9-bit shift UART	$f_{PCLK}/64$
1	1	Mode 3: 9-bit shift UART	Variable

The UART1 is connected to the integrated LIN transceiver, and to GPIO for test purpose. The UART2 is connected to GPIO only.

22 Measurement Unit

22.1 Features

- 1 x 8-bit ADC with 10 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VBAT_SENSE**, **VS**, **VDDP** and **VDDC**.
- VBG monitoring of 8-bit ADC to guarantee functional safety requirements.
- Bridge Driver Diagnosis Measurement (VDH, VCP).
- Temperature Sensor for monitoring the chip temperature and PMU Regulator temperature.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

22.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 14 Measurement Functions and Associated Modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the NVM module
8-bit ADC (ADC2)	8-bit ADC module with 10 multiplexed inputs, including HV input attenuator	5 high voltage full supply range capable inputs (2.5V...30,7V(FS)) 2 medium voltage inputs (0..5V/7V FS). 3 low voltage inputs (0..1.2V/1.6V FS) (allocation see following overview figure)
10-bit ADC (ADC1)	10-bit ADC module with 8 multiplexed inputs	Five (5V) analog inputs from Port 2.x
VDH Input Voltage Attenuator	VDH input voltage attenuator	Scales down V(VDH) to the input voltage range of ADC1.CH6
Temperature Sensor	Temperature sensor with two multiplexed sensing elements: • PMU located sensor • Central chip located sensor	Generates output voltage which is a linear function of the local chip (junction) temperature.
Measurement Core Module	Digital signal processing and ADC2 control unit	1. Generates the control signal for the 8-bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

26 Bridge Driver (incl. Charge Pump)

26.1 Features

The MOSFET Driver is intended to drive external normal level NFET transistors in bridge configuration. The driver provides many diagnostic possibilities to detect faults.

Functional Features

- External Power NFET Transistor Driver Stage with driver capability for max. 100 nC gate charge @ 25 kHz switching frequency.
- Implemented adjustable cross conduction protection.
- Supply voltage (VSD) monitoring incl. adjustable over- and undervoltage shutdown with configurable interrupt signalling.
- VSD operating range down to 5.4 V
- VDS comparators for short circuit detection in on- and off-state
- Open-Load detection in off-state

26.2 Introduction

The MOSFET Driver Stage can be used for controlling external Power NFET Transistors (normal level). The module output is controlled by SFR or System PWM Machine (CCU6).

26.2.1 Block Diagram

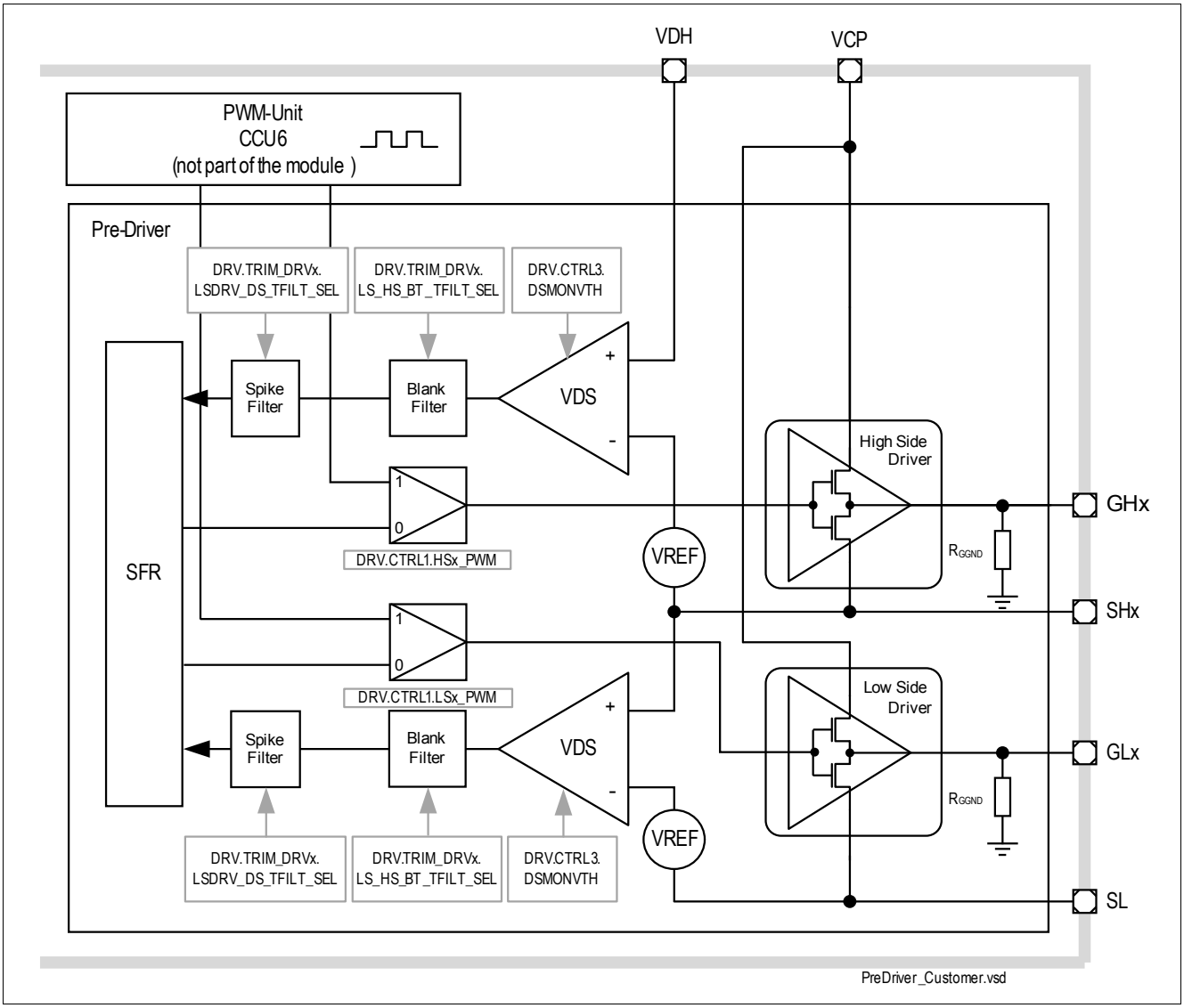

Figure 29 Driver Module Block Diagram (incl. system connections)

26.2.2 General

The Driver can be controlled in two different ways:

- In Normal Mode the output stage is fully controllable through the SFR registers CTRLx (x = 1,2,3). Protection functions such as overcurrent and open-load detection are available.
- The PWM Mode can also be enabled by the corresponding bit in CTRL1 and CTRL2. The PWM must be configured in the System PWM Module (CCU6). All protection functions are available in PWM mode as well.

Protection Functions

- Overcurrent detection and shutdown feature for external MOSFET by Drain Source measurement
- Programmable minimum cross current protection time
- Open-load detection feature in Off-state for external MOSFET.

29.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

29.2.1 PMU I/O Supply (VDDP) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the pad-supply VDDP and the transition times between the system modes are specified here.

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDP}	0	–	50	mA	1)	P_2.1.1
Specified output current	I_{VDDP}	0	–	30	mA	1)2)	P_2.1.22
Required decoupling capacitance	C_{VDDP1}	0.47	–	2.2	µF	3)4) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.1.2
Required buffer capacitance for stability (load jumps)	C_{VDDP2}	1	–	2.2	µF	3)4) The specified capacitor value is a typical value.	P_2.1.20
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	5) I_{load} < 90mA; V_S > 5.5V	P_2.1.3
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	2)5) I_{load} < 70mA; V_S > 5.5V	P_2.1.23
Output voltage including line and load regulation @ Stop Mode	$V_{DDPOUTSTOP}$	4.5	5.0	5.5	V	5) I_{load} is only internal; V_S > 5.5V; -40°C ≤ T_j ≤ -150°C.	P_2.1.21
Output voltage including line and load regulation @ Stop Mode - Extended temperature range	$V_{DDPOUTSTOP\_HT}$	3.5	5.0	5.8	V	5) I_{load} is only internal; V_S > 5.5V; 150°C < T_j ≤ 175°C.	P_2.1.29
Output drop @ Active Mode	$V_{SVDDPout}$	–	50	400	mV	I_{VDDP} = 30mA6); 3.5V < V_S < 5.0V	P_2.1.4
Load regulation @ Active Mode	$V_{VDDPLOR}$	-50	–	50	mV	2 ... 90mA; C = 570nF -40°C < T_j ≤ 150°C	P_2.1.5
Load regulation @ Active Mode-Extended temperature range	$V_{VDDPLOR\_HT}$	-70	–	70	mV	2 ... 90mA; C = 570nF 150°C < T_j ≤ 175°C	P_2.1.30
Line regulation @ Active Mode	$V_{VDDPLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.1.6
Overvoltage detection	V_{DDPOV}	5.14	–	5.4	V	V_S > 5.5V; Overvoltage leads to SUPPLY_NMI	P_2.1.7
Overvoltage detection filter time	t_{FILT_VDDPOV}	–	735	–	µs	3)7)	P_2.1.24

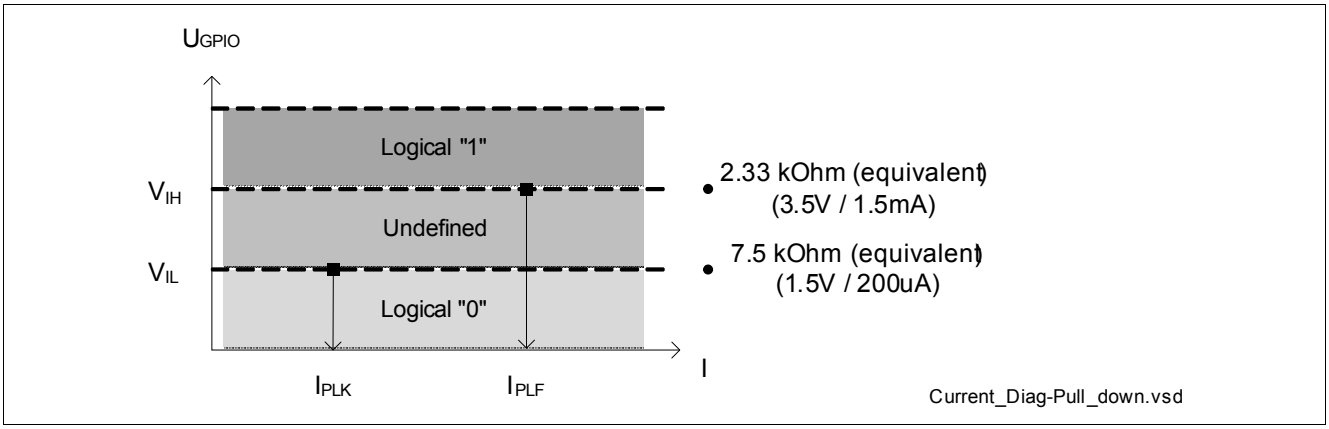

Figure 35 Pull-Down Keep and Force Current

29.5.2 DC Parameters of Port 0, Port 1, TMS and Reset

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the maximum allowed ocurrent which can be taken out of VDDP.

Table 30 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Maximum Output Current (I_{OLnom} , - I_{OHnom})		Number
	V_{DDP} ≥ 4.5V	2.6V < V_{DDP} < 4.5V	V_{DDP} ≥ 4.5V	2.6V < V_{DDP} < 4.5V	
Strong driver[2)]	5 mA	3 mA	1.6 mA	1.0 mA	P_5.1.15
Medium driver[3)]	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.1.1
Weak driver[3)]	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.1.2

1) Not subject to production test, specified by design.
2) Not available for port pins P0.4, P1.0, P1.1 and P1.2
3) All P0.x and P1.x

Table 31 DC Characteristics Port0, Port1

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input hysteresis	HYS_{P0_P1}	0.11 x V_{DDP}	–	–	V	[1)] Series resistance = 0 Ω; 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.5
Input hysteresis	$HYS_{P0\_P1\_exend}$	–	0.09 x V_{DDP}	–	V	[1)] Series resistance = 0 Ω; 2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.16

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.31
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.5	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_6.1.33
Duty cycle D7 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty1}	0.399	–	–		5) duty cycle D7 THRec(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus\_rec(min)}$/2 t_{bit};	P_6.1.34
Duty cycle D8 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty2}	–	–	0.578		5) duty cycle 8 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S;V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus\_rec(max)}$/2 t_{bit};	P_6.1.35
LIN input capacity	C_{LIN_IN}	–	15	30	pF	6)	P_6.1.69
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.36
Thermal Shutdown (Junction Temperature)							
Thermal shutdown temp.	T_{jSD}	190	200	215	°C	6)	P_6.1.65
Thermal shutdown hyst.	ΔT	–	10	–	K	6)	P_6.1.66

1) Maximum limit specified by design.
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) Bus load concerning LIN Spec 2.2:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Not subject to production test, specified by design.

Table 35 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating input voltage range V_{AREF}	$V_{AREF,range}$	0	–	5.62	V	1)	P_8.1.51
Accuracy of V_{AREF} sense after calibration	ΔV_{AREF}	-79	–	79	mV	V_S = 5.5V to 18V	P_8.1.48
8-Bit ADC Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: V_{BG}	ATT_{VBG}	–	0.75	–		–	P_8.1.57
Nominal operating input voltage range V_{BG}	$V_{BG,range}$	0.8	–	1.64	V	1)	P_8.1.52
Value of ADC2-V_{BG} measurement after calibration	V_{BG_PMU}	1.01	1.07	1.18	V	-40°C ≤ T_j ≤ 150°C	P_8.1.73
Value of ADC2-V_{BG} measurement after calibration-Extended temperature range	$V_{BG\_PMU\_HT}$	1.01	1.07	1.44	V	150°C < T_j ≤ 175°C	P_8.1.75
Core supply Voltage Measurement V_{DDC}							
Input-to-output voltage attenuation: V_{DDC}	ATT_{VDDC}	–	0.75	–		–	P_8.1.34
Nominal operating input voltage range V_{DDC}	$V_{DDC,range}$	0.8	–	1.64	V	1)	P_8.1.53
Accuracy of V_{DDC} sense after calibration	ΔV_{DDC_SENSE}	-22	–	22	mV	V_S = 5.5 to 18V	P_8.1.6
VDH Input Voltage Measurement $V_{VDH10BITADC}$							
VDH Input to output voltage attenuation:	ATT_{VDH_1}	–	0.166	–		SFR setting 1	P_8.1.64
VDH Input to output voltage attenuation:	ATT_{VDH_2}	–	0.224	–		SFR setting 2	P_8.1.65
VDH Input to output voltage attenuation:	ATT_{VDH_3}	–	0.226	–		1)SFR setting 2 -40°C ≤ Tj ≤ 85°C	P_8.1.81
Nominal operating input voltage range V_{VDH}, Attenuation Range 1	$V_{VDH,range1}$	–	–	30	V	SFR setting 1	P_8.1.66
Nominal operating input voltage range V_{VDH}, Attenuation Range 2	$V_{VDH,range2}$	–	–	20	V	SFR setting 2	P_8.1.67

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.29
Absolute input propagation time difference between propagation times for all LSx (LSx on)	$t_{Pon(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.30
Absolute input propagation time difference between propagation times for all LSx (LSx off)	$t_{Poff(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.41
Absolute input propagation time difference between propagation times for all HSx (HSx on)	$t_{Pon(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.42
Absolute input propagation time difference between propagation times for all HSx (HSx off)	$t_{Poff(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.43
Drain source monitoring							
Drain source monitoring threshold	$V_{DSMONVTH}$	– 0.07 0.35 0.55 0.65 0.90 1.00 1.20 1.40	– 0.25 0.50 0.75 1.00 1.25 1.5 1.75 2.00	– 0.40 0.650 0.90 1.25 1.45 1.80 2.10 2.40	V	DRV_CTRL3.DSMONVTH<2:0> xxx 000 001 010 011 100 101 110 111	P_12.1.46
Open load diagnosis currents							
Pull-up diagnosis current	I_{PUDiag}	-220	-370	-520	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.47
Pull-down diagnosis current	I_{PDDiag}	650	900	1100	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.48
Charge pump							
Output voltage VCP vs. VSD	V_{CPmin1}	8.5	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, C_{CP1}, C_{CP2} = 220 nF, Bridge Driver enabled -40°C ≤ T_j ≤ 150°C	P_12.1.53

Table 43 Electrical Characteristics Operational Amplifier (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Adjusted output offset voltage-Extended temperature range	V_{OOS_HT}	-50	10	50	mV	V_{AIP}= V_{AIN} = 0 V and G = 40, 150°C < T_j ≤ 175°C	P_13.1.28
DC input voltage common mode rejection ratio	DC-CMRR	58	80	–	dB	CMRR (in dB)=-20*log (differential mode gain/ common mode gain) V_{CMI}= -2V... 2V, V_{AIP}-V_{AIN}=0V, -40°C ≤ T_j ≤ 150°C	P_13.1.8
DC input voltage common mode rejection ratio-Extended temperature range	DC-CMRR_HT	57	80	–	dB	CMRR (in dB)=-20*log (differential mode gain/ common mode gain) V_{CMI}= -2V... 2V, V_{AIP}-V_{AIN}=0V, 150°C ≤ T_j ≤ 175°C	P_13.1.27
Settling time to 98%	T_{SET}	–	800	1400	ns	Derived from 80 - 20 % rise fall times for ± 2V overload condition (3 Tau value of settling time constant)[2]	P_13.1.9
Current Sense Amplifier Input Resistance @ OP1, OP2	$R_{in\_OP1\_OP2}$	1	1.25	1.5	kΩ	[2]–	P_13.1.25

1) Typical V_{ZERO} = 0,4 * **VAREF**.

2) This parameter is not subject to production test.