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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk02fn128vlf10

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Figure 1. Functional block diagram

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	_	3	_	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	$2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}, \text{ I}_{\text{OL}} = 3 \text{ mA}$	—	_	0.5	V	
	$1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 1.5 \text{ mA}$	_	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	—	100	mA	
I _{IN}	I _{IN} Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	_	0.002	0.5	μA	1, 2
	High drive port pins	_	0.004	0.5	μA	
I _{IN}	Input leakage current (total all pins) for full temperature range		_	1.0	μA	2
R _{PU}	Internal pullup resistors	20	—	50	kΩ	3
R _{PD}	PD Internal pulldown resistors		_	50	kΩ	4

Table 3. Voltage and current operating behaviors (continued)

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.

2. Measured at VDD=3.6V

3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz
- MCG mode: FEI

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	_	_	300	μs	1
	• VLLS0 \rightarrow RUN	_	_	135	μs	
	• VLLS1 → RUN	_	_	135	μs	
	• VLLS2 → RUN			75	μs	

General



Figure 3. Run mode supply current vs. core frequency

4. IEC Level Maximums: N \leq 12dBmV, M \leq 18dBmV, L \leq 24dBmV, K \leq 30dBmV, I \leq 36dBmV .

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	_	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
	High Speed run mo	ode			_
f _{SYS}	System and core clock	—	100	MHz	
f _{BUS}	Bus clock	—	50	MHz	
	Normal run mode (and High Speed run mode ur	nless otherwis	se specified a	bove)	
f _{SYS}	System and core clock	—	72	MHz	
f _{BUS}	Bus clock	—	50	MHz	
f _{FLASH}	f _{FLASH} Flash clock		25	MHz	
f _{LPTMR}	LPTMR clock	—	25	MHz	
	VLPR mode ¹	•	•	•	•
f _{SYS}	System and core clock	—	4	MHz	
f _{BUS}	Bus clock	—	4	MHz	
f _{FLASH}	SH Flash clock		1	MHz	
f _{ERCLK}	External reference clock		16	MHz	
f _{LPTMR_pin}	LPTMR clock	—	25	MHz	

Symbol	Description	Min.	Max.	Unit	Notes
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	

Table 9. Device clock specifications (continued)

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

T.I.I. 40

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

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Table 10.	General	switchi	ng sp	Deciti	cations	
						_

Symbol De	escription	Min.	Max.	Unit	Notes
GPI disa	IO pin interrupt pulse width (digital glitch filter abled) — Synchronous path	1.5	_	Bus clock cycles	1, 2
Exte Asy	ternal RESET and NMI pin interrupt pulse width — ynchronous path	100	_	ns	3
GPI disa pati	IO pin interrupt pulse width (digital glitch filter abled, passive filter disabled) — Asynchronous h	50		ns	4
Por	rt rise and fall time				5
	Slew disabled	—			
	• $1.71 \le V_{DD} \le 2.7V$	—	10	ns	
	• $2.7 \le V_{DD} \le 3.6V$		5	ns	
	Slew enabled	—			
	• $1.71 \le V_{DD} \le 2.7V$	—	30	ns	
	• $2.7 \le V_{DD} \le 3.6V$		16	ns	

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater of synchronous and asynchronous timing must be met.
- 3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
- 4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
- 5. 25 pF load

2.4 Thermal specifications

Peripheral operating requirements and behaviors

Board type	Symbol	Descriptio n	64 LQFP	48 LQFP	32 QFN	Unit	Notes
		on parameter, junction to package top outside center (natural convection)					

- 1. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air), or EIA/JEDEC Standard JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air).
- 2. Determined according to JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board.
- 3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 4. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 12. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation			
	Serial wire debug	0	33	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width			
	Serial wire debug	15	_	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5		ns



Figure 5. Serial wire clock input timing





3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
		50	_	ns

Symbol	Description	Min.	Max.	Unit
	Boundary Scan	25	—	ns
	JTAG and CJTAG			
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 13. JTAG limited voltage range electricals (continued)

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	_	ns
	JTAG and CJTAG	33	_	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	_	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	_	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	_	26.2	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns



Figure 9. Test Access Port timing





3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.3 Oscillator electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71		3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	_	μA	
	• 8 MHz (RANGE=01)	—	300	_	μA	
	• 16 MHz	_	950	_	μA	
	• 24 MHz	_	1.2	_	mA	
	• 32 MHz	_	1.5	_	mA	
I _{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	_	25	_	μA	
	• 4 MHz	_	400	_	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C _x	EXTAL load capacitance					2, 3
Cy	XTAL load capacitance	_	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—			MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	_	MΩ	
	Feedback resistor — high-frequency, low- power mode (HGO=0)	—	_	_	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200	_	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	

3.3.3.1 Oscillator DC electrical specifications Table 17. Oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	_	V	

 Table 17. Oscillator DC electrical specifications (continued)

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x and C_y can be provided by using either integrated capacitors or external components.

4. When low-power mode is selected, R_F is integrated and must not be attached externally.

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 18. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low- frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high- frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	_	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	_	_	50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	_	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	_	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode	VREFL		31/32 * VREFH	V	
		All other modes	VREFL	—	VREFH		
C _{ADIN}	Input	16-bit mode	_	8	10	pF	
	capacitance	 8-bit / 10-bit / 12-bit modes 	_	4	5		
R _{ADIN}	Input series resistance		—	2	5	kΩ	
R _{AS}	Analog source	13-bit / 12-bit modes					3
	(external)	f _{ADCK} < 4 MHz	—	_	5	kΩ	
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	_	12.0	MHz	4
C _{rate}	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging	20	—	1200	Ksps	
		Continuous conversions enabled, subsequent conversion time					
C _{rate}	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37	—	461	Ksps	
		Continuous conversions enabled, subsequent conversion time					

3.6.1.1 16-bit ADC operating conditions Table 23. 16-bit ADC operating conditions

- Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
		 <12-bit modes 	—	±0.5	-0.7 to +0.5		
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	$V_{ADIN} = V_{DDA}^5$
		 <12-bit modes 	—	-1.4	-1.8		
EQ	Quantization error	16-bit modes	_	-1 to 0	_	LSB ⁴	
		 ≤13-bit modes 	_	-	±0.5		
ENOB	Effective number of	16-bit differential mode					6
	bits	• Avg = 32	12.8	14.5	_	bits	
		• Avg = 4	11.9	13.8	_	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9	_	bits	
		• Avg = 4	11.4	13.1	_		
						bits	
SINAD	distortion	See ENOB	6.02 ×	ENOB +	1.76	dB	
THD	Total harmonic	16-bit differential mode				dB	7
	distortion	• Avg = 32		-94	_	dB	
		16-bit single-ended mode		-85			
		• Avg = 32					
SFDR	Spurious free	16-bit differential mode	00	05	_	dB	7
	dynamic range	• Avg = 32	02	95		dB	
		16-hit single-ended mode	78	90			
		• Avg = 32	70	30			
		,					
E _{IL}	Input leakage error			I _{In} × R _{AS}		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}

Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.



Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements Table 26. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
CL	Output load capacitance	—	100	pF	2
١L	Output load current	_	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.8.1 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	_	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

Table 32. Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 18. DSPI classic SPI timing — master mode

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t _{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) - 4	(t _{SCK/2)} + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	25	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	25	ns





Figure 21. DSPI classic SPI timing — slave mode

3.8.3 Inter-Integrated Circuit Interface (I²C) timing Table 36. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	_	0.6		μs
LOW period of the SCL clock	t _{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7		0.6	_	μs



Figure 24. K02F 48 LQFP pinout diagram

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	C°
V _{DD}	Supply voltage	3.3	V

7.4 Relationship between ratings and operating requirements



7.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes
		 Removed Section 6, "Ordering parts." Added "48-pin LQFP part marking" section Added "32-pin QFN part marking" section
2	8/2014	 On p. 1, under "Memories and memory interfaces," added bullet, "Preprogrammed Kinetis flashloader for one-time, in-system factory programming" On p. 1, added parenthetical element to the following bullet under "Analog modules": <i>Accurate internal voltage reference (not available for 32-pin QFN package)</i> On p. 1, added parenthetical element to the following bullet under "Timers": <i>Two 2-channel motor-control general-purpose timers with quadrature decoder functionality (FTM2 does not have external pins on the 32-pin QFN or the 48-pin LQFP package)</i> In "Voltage and current operating ratings" section, updated digital supply current maximum value In "Voltage and current operating behaviors" section, updated input leakage information In "Power consumption operating behaviors table": Updated existing typical and maximum power measurements Added new typical power measurements for the following: IDD_HSRUN (High Speed Run mode, all peripheral clocks disabled, current executing While(1) loop) IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, exercuting While(1) loop) IDD_RUN (Run mode current in Compute operation, all peripheral clocks disabled, executing While(1) loop) IDD_VLPR (Very Low Power Run mode current in Compute operation, all peripheral clocks disabled, executing CoreMark code) IDD_VLPR (Very Low Power Run mode current in Compute operation, all peripheral clocks disabled, executing While(1) loop) Updated section, "EMC radiated emissions operating behaviors for 64 LQFP package" In "Thermal attributes" section, added 64-pin LQFP and 32-pin QFN package values
1	3/2014	Initial public release

Table 41. Revision History (continued)