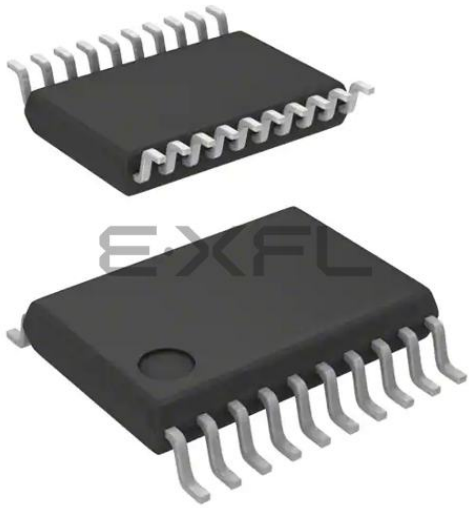

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 14 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10266dsp-v0 |

### 2.2.2 Description of Functions

| Function Name | I/O | Functions |
|---|---|---|
| ANI0 to ANI3, ANI16 to ANI22 | input | Analog input pins of A/D converter<br>(see **Figure 10-44 Analog Input Pin Connection**) |
| $AV_{REFP}$ | input | Inputs the A/D converter reference potential (+ side) |
| $AV_{REFM}$ | input | Inputs the A/D converter reference potential (− side) |
| INTP0 to INTP5 | input | External interrupt request input<br>Specified available edge : rising edge, falling edge, or both rising and falling edges |
| KR0 to KR9 | input | Key interrupt input |
| PCLBUZ0, PCLBUZ1 | output | Clock/buzzer output |
| REGC | − | Connecting regulator output stabilization capacitance for internal operation. Connect this pin to $V_{SS}$ via a capacitor (0.47 to 1 μF) |
| $\overline{RESET}$ | input | External reset input for low level active<br>When the external reset pin is not used, connect this pin directly or via a resistor to $V_{DD}$. |
| RxD0 to RxD2 | input | Serial data input for serial interfaces UART0, UART1, and UART2 |
| TxD0 to TxD2 | output | Serial data output for serial interfaces UART0, UART1, and UART2 |
| SCK00, SCK01, SCK11, SCK20 | I/O | Serial clock I/O for serial interfaces CSI00, CSI01, CSI11, and CSI20 |
| SI00, SI01, SI11, SI20 | input | Serial data input for serial interfaces CSI00, CSI01, CSI11, and CSI20 |
| SO00, SO01, SO11, SO20 | output | Serial data output for serial interfaces CSI00, CSI01, CSI11, and CSI20 |
| SCLA0 | I/O | Serial clock I/O for serial interface IICA |
| SDAA0 | I/O | Serial data I/O for serial interface IICA |
| SCL00, SCL01, SCL11, SCL20 | output | Clock output for simplified $I^2C$ serial interfaces IIC00, IIC01, IIC11, IIC20 |
| SDA00, SDA01, SDA11, SDA20 | I/O | Serial data I/O for simplified $I^2C$ serial interfaces IIC00, IIC01, IIC11, IIC20 |
| TI00 to TI07 | input | Inputting an external count clock/capture trigger to 16-bit timers 00 to 07 |
| TO00 to TO07 | output | Timer output pins of 16-bit timers 00 to 07 |
| X1, X2 | − | Connecting a resonator for main system clock |
| EXCLK | input | External clock input pin for main system clock |
| $V_{DD}$ | − | Positive power supply |
| $V_{SS}$ | − | Ground potential |
| TOOLRxD | input | This UART serial data input pin for an external device connection is used during flash memory programming |
| TOOLTxD | output | This UART serial data output pin for an external device connection is used during flash memory programming |
| TOOL0 | I/O | Data I/O pin for a flash memory programmer/debugger |

**Caution** The following shows the relationship between P40/TOOL0 and the operation mode when reset is released.

**Table 2-1. Relationship between P40/TOOL0 and the Operation Mode When Reset Is Released**

| P40/TOOL0 | Operation mode |
|---|---|
| $V_{DD}$ | Normal operation mode |
| 0 V | Flash memory programming mode |

For details, see **24.4 Serial Programming Method**.

**Remark** Use bypass capacitors (about 0.1 μF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to $V_{DD}$ to $V_{SS}$ lines.

**(2) CALLT instruction table area**

The 64-byte area of 00080H to 000BFH can store the subroutine entry address of a 2-byte call instruction (CALLT). Set the subroutine entry address to a value in a range of 00000H to 0FFFFH (because an address code is 2 bytes).

**(3) Option byte area**

The 4-byte area of 000C0H to 000C3H can be used as an option byte area. For details, see **CHAPTER 23 OPTION BYTE**.

**(4) On-chip debug security ID setting area**

The 10-byte areas of 000C4H to 000CDH and 010C4H to 010CDH can be used as an on-chip debug security ID setting area. For details, see **CHAPTER 25 ON-CHIP DEBUG FUNCTION**.

### 3.1.4 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area of FFF00H to FFFFFH (see **Table 3-6** in **3.2.4 Special function registers (SFRs)**).

**Caution** Do not access addresses to which SFRs are not assigned.

### 3.1.5 Extended special function register (2nd SFR: 2nd Special Function Register) area

On-chip peripheral hardware special function registers (2nd SFRs) are allocated in the area of F0000H to F07FFH (see **Table 3-7** in **3.2.5 Extended Special function registers (2nd SFRs: 2nd Special Function Registers)**).

SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

**Caution** Do not access addresses to which extended SFRs are not assigned.

**Table 4-5. PMxx, Pxx, PUxx, PIMx, POMx, PMCxx Registers and the Bits (30-pin Products)**

| Port | | Bit name | | | | | |
|---|---|---|---|---|---|---|---|
| | | PMxx register | Pxx register | PUxx register | PIMx register | POMx register | PMCxx register |
| Port 0 | 0 | PM00 | P00 | PU00 | – | POM00 | PMC00 |
| | 1 | PM01 | P01 | PU01 | PIM01 | – | PMC01 |
| Port 1 | 0 | PM10 | P10 | PU10 | PIM10 | POM10 | – |
| | 1 | PM11 | P11 | PU11 | PIM11 | POM11 | – |
| | 2 | PM12 | P12 | PU12 | – | POM12 | – |
| | 3 | PM13 | P13 | PU13 | PIM13 | POM13 | – |
| | 4 | PM14 | P14 | PU14 | PIM14 | POM14 | – |
| | 5 | PM15 | P15 | PU15 | PIM15 | POM15 | – |
| | 6 | PM16 | P16 | PU16 | PIM16 | – | – |
| | 7 | PM17 | P17 | PU17 | PIM17 | POM17 | – |
| Port 2 | 0 | PM20 | P20 | – | – | – | – |
| | 1 | PM21 | P21 | – | – | – | – |
| | 2 | PM22 | P22 | – | – | – | – |
| | 3 | PM23 | P23 | – | – | – | – |
| Port 3 | 0 | PM30 | P30 | PU30 | – | – | – |
| | 1 | PM31 | P31 | PU31 | – | – | – |
| Port 4 | 0 | PM40 | P40 | PU40 | – | – | – |
| Port 5 | 0 | PM50 | P50 | PU50 | – | POM50 | – |
| | 1 | PM51 | P51 | PU51 | – | – | – |
| Port 6 | 0 | PM60 | P60 | – | – | – | – |
| | 1 | PM61 | P61 | – | – | – | – |
| Port 12 | 0 | PM120 | P120 | PU120 | – | – | PMC120 |
| | 1 | – | P121 | – | – | – | – |
| | 2 | – | P122 | – | – | – | – |
| Port 13 | 7 | – | P137 | – | – | – | – |
| Port 14 | 7 | PM147 | P147 | PU147 | – | – | PMC147 |

### 6.3.10 Timer output register 0 (TO0)

The TO0 register is a buffer register of timer output of each channel.

The value of each bit in this register is output from the timer output pin (TO0n) of each channel.

The TO0n bit oh this register can be rewritten by software only when timer output is disabled (TOE0n = 0). When timer output is enabled (TOE0n = 1), rewriting this register by software is ignored, and the value is changed only by the timer operation.

To use the TO00, TO01, TO02, TO03, (TO04), (TO05), (TO06), or (TO07) pin as a port function pin, set the corresponding TO0n bit to 0.

The TO0 register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TO0 register can be set with an 8-bit memory manipulation instruction with TO0L.

Reset signal generation clears this register to 0000H.

**Figure 6-16. Format of Timer Output register 0 (TO0)**

Address: F01B8H, F01B9H After reset: 0000H R/W

20- and 24-pin products

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TO0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TO03 | TO02 | TO01 | TO00 |

30-pin products

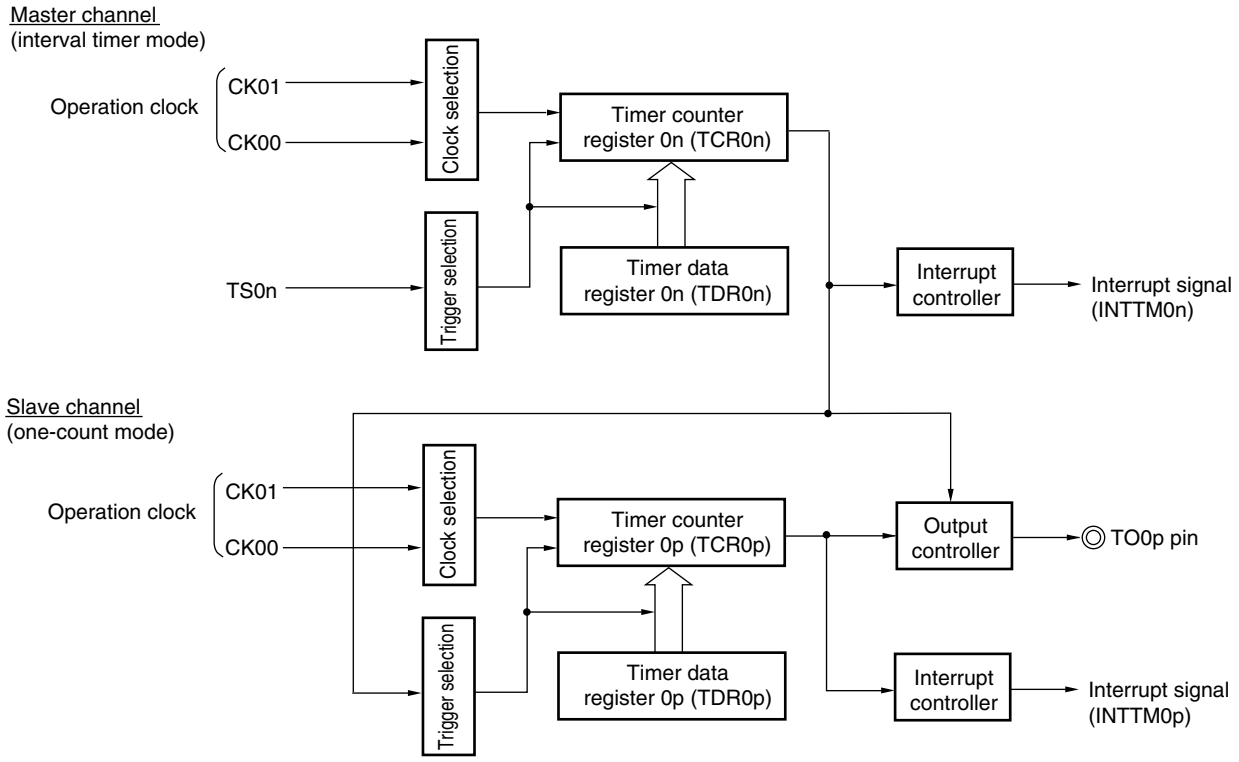
| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TO0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TO07 | TO06 | TO05 | TO04 | TO03 | TO02 | TO01 | TO00 |

| TO0n | Timer output of channel n |
|---|---|
| 0 | Timer output value is "0". |
| 1 | Timer output value is "1". |

**Caution** Be sure to clear undefined bits to "0".

**Remark** n: Channel number (n = 0 to 7)

**Figure 6-67. Block Diagram of Operation as PWM Function**




**Remark** n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

○ Scan mode (ADMD = 1)

| ADS4 | ADS3 | ADS2 | ADS1 | ADS0 | Analog input channel | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Scan 0 | Scan 1 | Scan 2 | Scan 3 |
| 0 | 0 | 0 | 0 | 0 | ANI0 | ANI1 | ANI2 | ANI3 |
| 0 | 0 | 0 | 0 | 1 | ANI1 | ANI2 | ANI3 | – |
| 0 | 0 | 0 | 1 | 0 | ANI2 | ANI3 | – | – |
| 0 | 0 | 0 | 1 | 1 | ANI3 | – | – | – |
| Other than the above | | | | | Setting prohibited | | | |

**Remark** – : Ignore the conversion result because it is undefined.

**Cautions 1.** Be sure to clear bits 5 and 6 to 0.

**2.** Set a channel to be set the analog input by ADPC and PMCx registers in the input mode by using port mode registers 0, 1, 2, 4, 12, or 14 (PM0, PM1, PM2, PM4 PM12, PM14).

**3.** Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.

**4.** Do not set the pin that is set by port mode control registers 0, 1, 4, 12, 14 (PMC0, PMC1, PMC4, PMC12, PMC14) as digital I/O by the ADS register.

**5.** Only rewrite the value of the ADISS bit while A/D conversion comparator operation is stopped(ADCS = 0, ADCE = 0)

**6.** If using $AV_{REFP}$ as the + side reference voltage of the A/D converter, do not select ANI0 as an A/D conversion channel.

**7.** If using $AV_{REFM}$ as the – side reference voltage of the A/D converter, do not select ANI1 as an A/D conversion channel.

**8.** If the ADISS bit is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For details about the setting flow, see 10.7.4 Setup when temperature sensor output voltage/internal reference voltage is selected.

**9.** Do not set the ADISS bit to 1 when shifting to the STOP mode or HALT mode. If the ADISS bit is set to 1, the A/D converter reference voltage current ($I_{ADREF}$) indicated in 28.3.2 or 29.3.2 Supply current characteristics will be added.

### 10.3.10 A/D test register (ADTES)

This register is used to select the + side or - side reference voltage of the A/D converter, an analog input channel (ANIxx), the temperature sensor output voltage, and the internal reference voltage (1.45 V) as the target for A/D conversion. For details, see **21.3.7 A/D test function**.

When using this register to test the A/D converter, set as follows.

- For zero-scale measurement, select the - side reference voltage as the target for conversion.
- For full-scale measurement, select the + side reference voltage as the target for conversion.

The ADTES register is set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 10-14. Format of A/D Test Register (ADTES)**

Address: F0013H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADTES | 0 | 0 | 0 | 0 | 0 | 0 | ADTES1 | ADTES0 |

| ADTES1 | ADTES0 | A/D conversion target |
|---|---|---|
| 0 | 0 | ANIxx/temperature sensor output voltage Note/internal reference voltage (1.45 V) Note (This is specified using the analog input channel specification register (ADS).) |
| 1 | 0 | The - side reference voltage (selected by the ADREFM bit of the ADM2 register) |
| 1 | 1 | The + side reference voltage (selected by the ADREFP1 and ADREFP0 bits of the ADM2 register) |
| Other than the above | | Setting prohibited |

**Note** The temperature sensor output voltage and internal reference voltage (1.45 V) can be selected only in HS (high-speed main) mode.

### 10.3.11 Registers controlling port function of analog input pins

Set up the port mode registers (PMxx), port mode control registers (PMCxx), and A/D port configuration register (ADPC), which are used for controlling the functions of the ports shared with the analog input pins of the A/D converter. For details, see **4.3.1 Port mode registers (PMxx)**, **4.3.6 Port mode control registers (PMCxx)**, and **4.3.7 A/D port configuration register**.

When using the ANI0 to ANI3 pins for analog input of the A/D converter, set the port mode register (PMxx) bit corresponding to each port to 1, and specify analog input by using the A/D port configuration register (ADPC).

When using the ANI16 to ANI22 pins for analog input of the A/D converter, set the port mode register (PMxx) bit and the port mode control register (PMCxx) bit to 1.

## 11.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI11, CSI20) Communication

This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate[Note]

  During master communication: Max. $f_{CLK}$/2 (CSI00 only)
  Max. $f_{CLK}$/4
  During slave communication: Max. $f_{MCK}$/6

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 (channel 0 of unit 0) supports the SNOOZE mode. When SCK00 pin input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.

**Note** Use the clocks within a range satisfying the SCK cycle time ($t_{KCY}$) characteristics. For details, see **CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: $T_A$ = -40 to +85°C)** or **CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: $T_A$ = -40 to +105°C)**.

The channels supporting 3-wire serial I/O (CSI00, CSI01, CSI11, CSI20) are channels 0, 1, 3 of SAU0 and channel 0 of SAU1.

20- or 24-pin products

| Unit | Channel | Used as CSI | Used as UART | Used as Simplified $I^2C$ |
|---|---|---|---|---|
| 0 | 0 | CSI00 | UART0 | IIC00[Note] |
| | 1 | CSI01[Note] | | IIC01[Note] |

30-pin products

| Unit | Channel | Used as CSI | Used as UART | Used as Simplified $I^2C$ |
|---|---|---|---|---|
| 0 | 0 | CSI00 | UART0 | IIC00 |
| | 1 | – | | – |
| | 2 | – | UART1[Note] | – |
| | 3 | CSI11[Note] | | IIC11[Note] |
| 1 | 0 | CSI20[Note] | UART2[Note] | IIC20[Note] |
| | 1 | – | | – |

**Note** Provided in the R5F102 products only.

### 11.5.8 Calculating transfer clock frequency

The transfer clock frequency for 3-wire serial I/O (CSI00, CSI01, CSI11, CSI20) communication can be calculated by the following expressions.

(1) Master

| (Transfer clock frequency) = {Operation clock ($f_{MCK}$) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [Hz] |
|---|

(2) Slave

| (Transfer clock frequency) = {Frequency of serial clock (SCK) supplied by master}[Note] [Hz] |
|---|

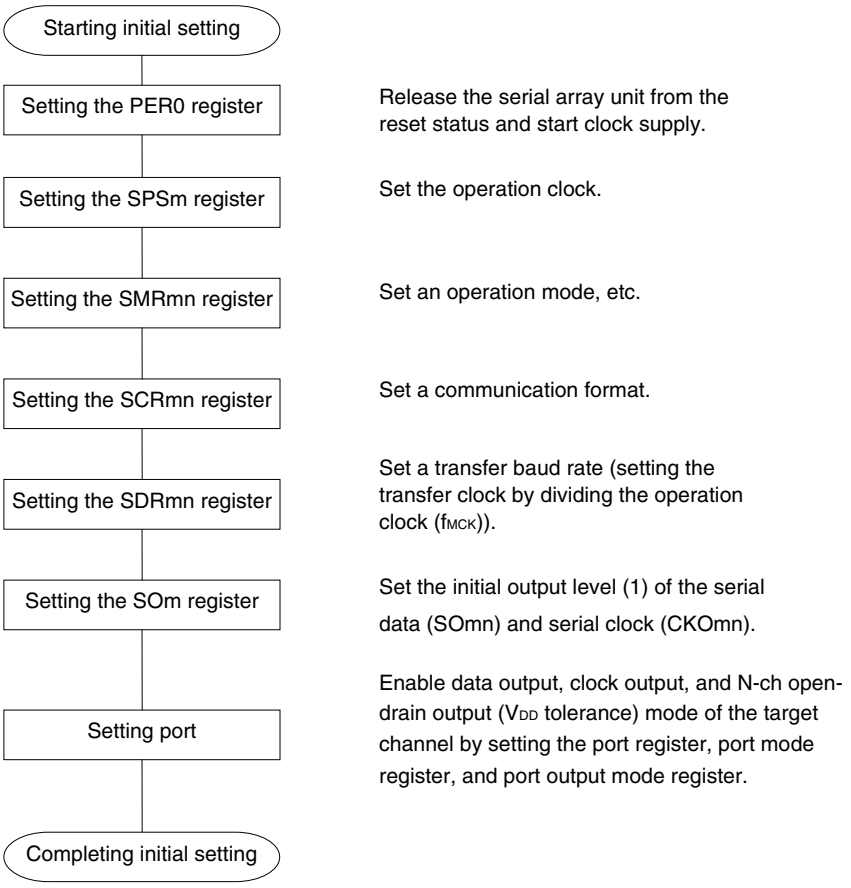
**Note** The permissible maximum transfer clock frequency is $f_{MCK}$/6.

**Remark** The value of SDRmn[15:9] is the value of bits 15 to 9 of serial data register mn (SDRmn) (0000000B to 1111111B) and therefore is 0 to 127.

The operation clock ($f_{MCK}$) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

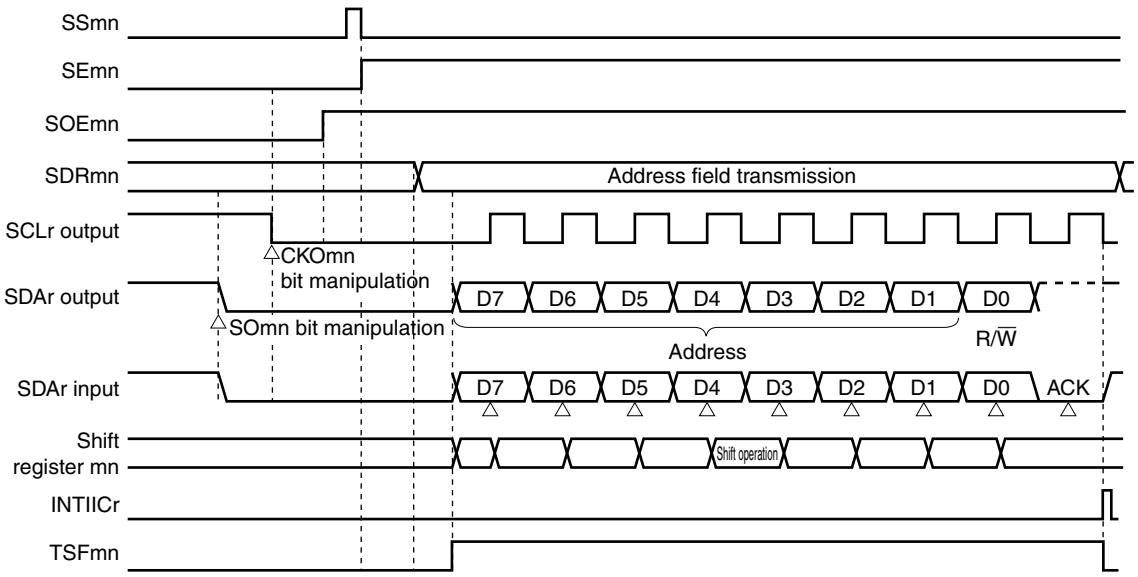
### (2) Operation procedure

**Figure 11-99. Initial Setting Procedure for simplified I²C Address Field Transmission**




### (3) Processing flow

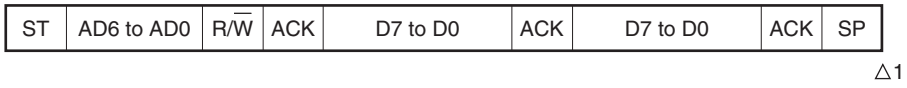
**Figure 11-100. Timing Chart of Address Field Transmission**




**Remark** m: Unit number, n: Channel number (mn = 00, 01, 03, 10), r: IIC number (r = 00, 01, 11, 20)

**(4) Operation without communication**

**(a) Start ~ Code ~ Data ~ Data ~ Stop**




△1: IICS0 = 00000001B

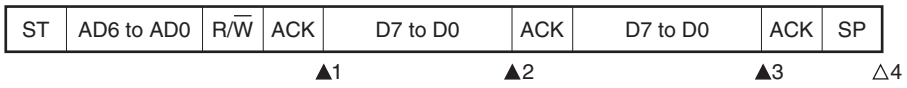
**Remark** △: Generated only when SPIE0 = 1

**(5) Arbitration loss operation (operation as slave after arbitration loss)**

When the device is used as a master in a multi-master system, read the MSTS0 bit each time interrupt request signal INTIICA0 has occurred to check the arbitration result.

**(a) When arbitration loss occurs during transmission of slave address data**

**(i) When WTIM0 = 0**




▲1: IICS0 = 0101×110B
▲2: IICS0 = 0001×000B
▲3: IICS0 = 0001×000B
△4: IICS0 = 00000001B

**Remark** ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

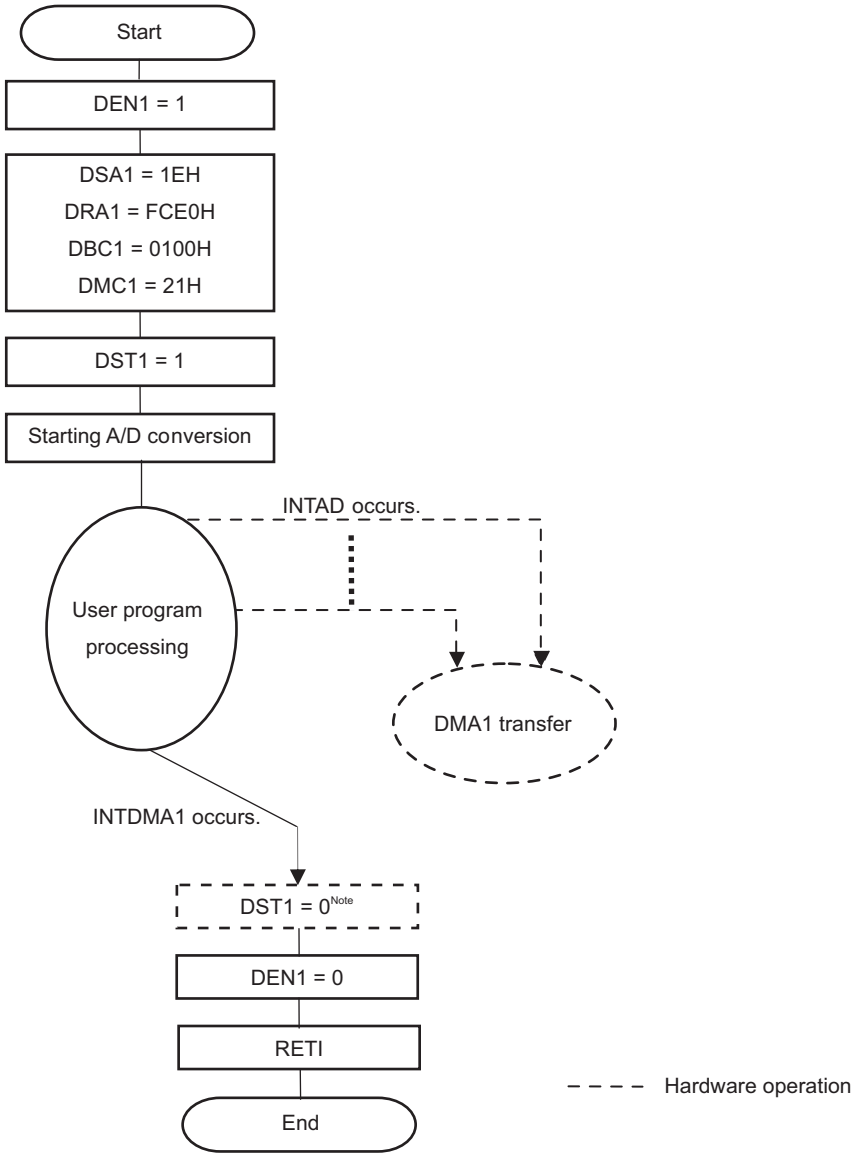
### 14.5.2 Consecutive capturing of A/D conversion results

A flowchart of an example of setting for consecutively capturing A/D conversion results is shown below.

- Consecutive capturing of A/D conversion results.
- DMA channel 1 is used for DMA transfer.
- DMA start source: INTAD
- Interrupt of A/D is specified by IFC13 to IFC10 = 0001B.
- Transfers FFF1EH and FFF1FH (2 bytes) of the 10-bit A/D conversion result register (ADCR) to 512 bytes of FFCE0H to FFEDFH of RAM.

**Remark** IFC13 to IFC10: Bits 3 to 0 of DMA mode control registers 1 (DMC1)

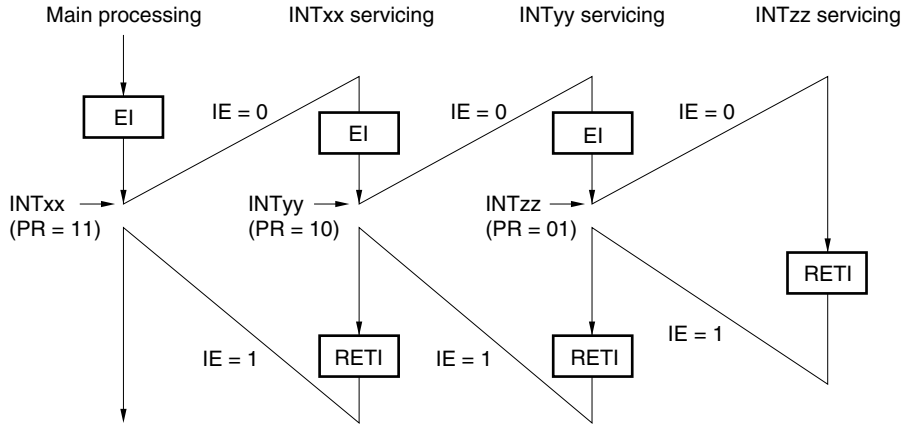
**Figure 14-8. Example of Setting of Consecutively Capturing A/D Conversion Results**




**Note** The DST1 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN1 flag is enabled only when DST1 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA1 (INTDMA1), set the DST1 bit to 0 and then the DEN1 bit to 0 (for details, refer to **14.5.5 Forced termination by software**).

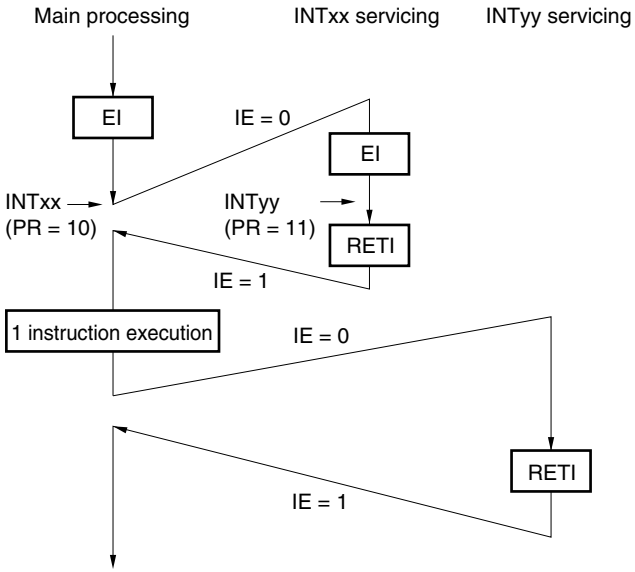
**Figure 15-13. Examples of Multiple Interrupt Servicing (1/2)**

**Example 1. Multiple interrupt servicing occurs twice**




During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

**Example 2. Multiple interrupt servicing does not occur due to priority control**




Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

## 16.2 Configuration of Key Interrupt

The key interrupt includes the following hardware.

**Table 16-2. Configuration of Key Interrupt**

| Item | Configuration |
|---|---|
| Control register | Key return control register (KRCTL)<br>Key return mode control registers (KRM0, KRM1)<br>Key return flag register (KRF)<br>Port mode registers 0, 4, 6 (PM0, PM4, PM6) |

**Notes 1.** The LVIMK flag is set to “1” by reset signal generation.

**2.** After an interrupt is generated, perform the processing according to **Figure 20-8 Processing Procedure After an Interrupt Is Generated**.

**3.** After a reset is released, perform the processing according to **Figure 20-9 Initial Setting of Interrupt and Reset Mode**.

**Remark** $V_{POR}$: POR power supply rise detection voltage

$V_{PDR}$: POR power supply fall detection voltage

**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**

**($T_A$ = −40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | ns |
| SCK00 high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2– 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCK00 low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | ns |
| SI00 hold time (from SCK00↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | ns |
| SI00 setup time (to SCK00↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↑ to SO00 output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 10 | | 10 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**LVD detection voltage of interrupt & reset mode**

**($T_A$ = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 1.94 | 1.98 | 2.02 | V |
| | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.05 | 2.09 | 2.13 | V |
| | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.07 | 3.13 | 3.19 | V |
| | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 2.56 | 2.61 | 2.66 | V |
| | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.66 | 2.71 | 2.76 | V |
| | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.68 | 3.75 | 3.82 | V |
| | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC1}$ = 0, 1, 1, falling reset voltage | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.96 | 3.02 | 3.08 | V |
| | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.98 | 4.06 | 4.14 | V |
| | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

### 28.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 28.4 AC Characteristics.

(7/17)

| Edition | Description | Chapter |
|---|---|---|
| 2.00 | Modification of Note 2 in Table 27-5 (16/17) | CHAPTER 27 INSTRUCTION SET |
| | Modification of Note 2 in Table 27-5 (17/17) | |
| | Modification of description of table in 28.1 Absolute Maximum Ratings (TA = 25° C) | CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: TA = − 40 to +85°C) |
| | Modification of table, Note, and Caution in 28.2.1 X1 oscillator characteristics | |
| | Modification of table in 28.2.2 On-chip oscillator characteristics | |
| | Modification of Note 3 in 28.3.1 Pin characteristics (1/4) | |
| | Modification of Note 3 in 28.3.1 Pin characteristics (2/4) | |
| | Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2) | |
| | Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2) | |
| | Modification of Notes 1 and 2 in (2) 30-pin products (1/2) | |
| | Modification of Notes 1 and 3 in (2) 30-pin products (2/2) | |
| | Modification of (3) Peripheral functions (Common to all products) | |
| | Modification of table in 28.4 AC Characteristics | |
| | Addition of Minimum Instruction Execution Time during Main System Clock Operation | |
| | Modification of figures of AC Timing Test Point and External Main System Clock Timing | |
| | Modification of figure of AC Timing Test Point | |
| | Modification of description and Note 2 in (1) During communication at same potential (UART mode) | |
| | Modification of description in (2) During communication at same potential (CSI mode) | |
| | Modification of description in (3) During communication at same potential (CSI mode) | |
| | Modification of description in (4) During communication at same potential (CSI mode) | |
| | Modification of table and Note 2 in (5) During communication at same potential (simplified I2C mode) | |
| | Modification of table and Notes 1 to 9 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) | |
| | Modification of Remarks 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) | |
| | Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) | |
| | Modification of Caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) | |
| | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) | |
| | Modification of table and Notes 1 and 2 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) | |
| | Modification of table, Note 1, and Caution 1 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) | |
| | Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) | |
| | Modification of table, Note 1, and Caution 1 in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I2C mode) | |
| | Modification of Remark in 28.5.2 Serial interface IICA | |
| | Addition of table to 28.6.1 A/D converter characteristics | |
| | Modification of description in 28.6.1 (1) | |
| | Modification of Notes 3 to 5 in 28.6.1 (1) | |
| | Modification of description and Notes 2 to 4 in 28. 6. 1 (2) | |
| | Modification of description and Notes 3 and 4 in 28. 6. 1 (3) | |
| | Modification of description and Notes 3 and 4 in 28. 6. 1 (4) | |
| | Modification of table in 28.6.2 Temperature sensor/internal reference voltage characteristics | |
| | Modification of table and Note in 28.6.3 POR circuit characteristics | |
| | Modification of table in 28.6.4 LVD circuit characteristics | |
| | Modification of table of LVD detection voltage of interrupt & reset mode | |
| | Modification of number and title to 28.6.5 Power supply voltage rising slope characteristics | |
| | Modification of table, figure, and Remark in 28.10 Timing of Entry to Flash Memory Programming Modes | |

(10/17)

| Edition | Description | Chapter |
|---|---|---|
| 1.00 | Modification of description in Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On (When voltage detector (LVD) is used) | CHAPTER 5 CLOCK GENERATOR |
| | Addition of description to 5.6.2 Example of setting X1 oscillation clock | |
| | Addition of description to Figure 5-14. CPU Clock Status Transition Diagram | |
| | Addition of description to (2) CPU operating with high-speed system clock (C) after reset release (A) | |
| | Modification and deletion of description in Table 5-4. Changing CPU Clock | |
| | Modification of description in Table 5-5. Maximum Number of Clocks Required for $f_{IH} \leftrightarrow f_{MX}$, and Table 5-6. Conditions Before the Clock Oscillation Is Stopped and Flag Settings | |
| | Addition of Figure to (7) Delay counter | CHAPTER 6 TIMER ARRAY UNIT |
| | Addition of description to Figure 6-2. Entire Configuration of Timer Array Unit (30-pin products) | |
| | Addition of Figure 6-3. Internal Block Diagram of Channel of Timer Array Unit | |
| | Addition of description to (1) Timer/counter register 0n (TCR0n) | |
| | Addition of description to (2) Timer data register 0n (TDR0n) | |
| | Modification of description and addition of caution to Figure 6-8. Format of Timer Clock Select register 0 (TPS0) | |
| | Modification of description in Table 6-4. Interval Times Available for Operation Clock CKS02 or CKS03, and addition of Caution in (3) Timer mode register 0n (TMR0n) | |
| | Modification of Figure 6-9. Format of Timer Mode Register 0n (TMR0n) | |
| | Addition of description to (5) Timer channel enable status register 0 (TE0) | |
| | Modification of Figure 6-12. Format of Timer Channel Start register 0 (TS0) | |
| | Addition of description to Figure 6-13. Format of Timer Channel Stop register 0 (TT0) | |
| | Addition of description to (8) Timer input select register 0 (TIS0) | |
| | Modification of description to Figure 6-15. Format of Timer Output Enable register 0 (TOE0) | |
| | Addition of description to (14) Port mode registers 0, 1, 3, or 4 (PM0, PM1, PM3, or PM4) | |
| | Addition of description to 6.4.1 Basic Rules of Simultaneous Channel Operation Function | |
| | Addition of description to 6.5.1 Count clock ($f_{TCLK}$) | |
| | Modification of description to Table 6-6. Operations from Count Operation Enabled State to Timer count Register 0n (TCR0n) Count Start | |
| | Addition of title to 6.5.3 Operation of counter | |
| | Modification of Figure 6-27. Operation Timing (In Capture & One-count Mode: High-level Width Measurement) | |
| | Addition of description to 6.6.2 TO0n Pin Output Setting | |
| | Modification of description to Figure 6-39, 43, 51, 55, 59, 64, 69, 74 Example of Set Contents of Registers | |
| | Modification of Figure 6-41, 45, 49, 53, 61 | |
| | Addition of 6.9 Cautions When Using Timer Array Unit | |
| | Addition of description to (2) Operation speed mode control register (OSMC) | CHAPTER 7 INTERVAL TIMER |
| | Addition of Caution to Figure 7-4. Format of Interval Timer Control Register (ITMC) | |
| | Modification of Figure 7-5. 12-Bit Interval Timer Operation Timing | |
| | Modification of Figure 8-1. Block Diagram of Clock Output/Buzzer Output Controller | CHAPTER 8 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER |
| | Modification of Figure 8-2. Format of Clock Output Select Register n (CKSn) | |
| | Addition of description to (2) Port mode register 1, 3 (PM1, PM3) | |
| | Addition of Caution to 8.4.1 Operation as output pin | |
| | Modification of description to 9.1 Functions of Watchdog Timer, 9.4.4 Setting watchdog timer interval interrupt | CHAPTER 9 WATCHDOG TIMER |
| | Modification of Figure 10-1. Block Diagram of A/D Converter | CHAPTER 10 A/D CONVERTER |
| | Modification of description to (3) A/D voltage comparator | |
| | Addition of Caution to Figure 10-3. Format of A/D Converter Mode Register 0 (ADM0) | |
| | Modification of description to Figure 10-4. Timing Chart When A/D Voltage Comparator Is Used | |