E·XFL Renesas Electronics America Inc - R5F10266DSP#X0 Datasheet

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What is "Embedded - Microcontrollers"?

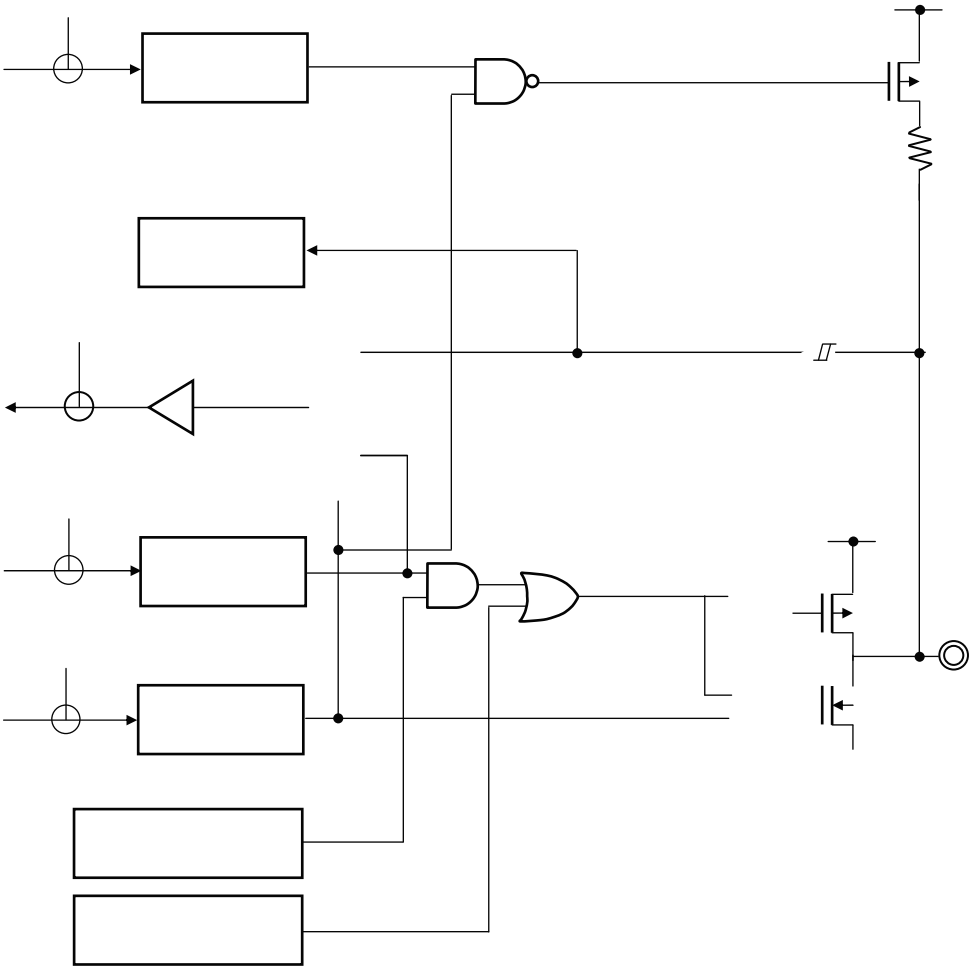
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10266dsp-x0

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 2-6. Pin Block Di agram for Pin Type 7-1-1



(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = 40 to +105°C, 2.4 V d V_{DD} d 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V d V_{DD} d 5.5 V, 2.7 V d V_b d 4.0 V	20 MHz < f_{MCK} d 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} d 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} d 8 MHz	16/f_{MCK}		ns
			f_{MCK} d 4 MHz	12/f_{MCK}		ns
		2.7 V d V_{DD} < 4.0 V, 2.3 V d V_b d 2.7 V	20 MHz < f_{MCK} d 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} d 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} d 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} d 8 MHz	16/f_{MCK}		ns
			f_{MCK} d 4 MHz	12/f_{MCK}		ns
		2.4 V d V_{DD} < 3.3 V, 1.6 V d V_b d 2.0 V	20 MHz < f_{MCK} d 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} d 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} d 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} d 8 MHz	32/f_{MCK}		ns
			f_{MCK} d 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V d V_{DD} d 5.5 V, 2.7 V d V_b d 4.0 V		t_{KCY2}/2 24		ns
		2.7 V d V_{DD} < 4.0 V, 2.3 V d V_b d 2.7 V		t_{KCY2}/2 36		ns
		2.4 V d V_{DD} < 3.3 V, 1.6 V d V_b d 2.0 V		t_{KCY2}/2 100		ns
SIp setup time (to SCKpn) Note 2	t_{SIK2}	4.0 V d V_{DD} d 5.5 V, 2.7 V d V_{DD} d 4.0 V		1/f_{MCK} + 40		ns
		2.7 V d V_{DD} < 4.0 V, 2.3 V d V_b d 2.7 V		1/f_{MCK} + 40		ns
		2.4 V d V_{DD} < 3.3 V, 1.6 V d V_{DD} d 2.0 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKpn) Note 3	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKpp to SOp output Note 4	t_{KSO2}	4.0 V d V_{DD} d 5.5 V, 2.7 V d V_b d 4.0 V, C_b = 30 pF, R_b = 1.4 k:			2/f_{MCK} + 240	ns
		2.7 V d V_{DD} < 4.0 V, 2.3 V d V_b d 2.7 V, C_b = 30 pF, R_b = 2.7 k:			2/f_{MCK} + 428	ns
		2.4 V d V_{DD} < 3.3 V, 1.6 V d V_b d 2.0 V, C_b = 30 pF, R_b = 5.5 k:			2/f_{MCK} + 1146	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKpp" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKpp" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKpn" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

2. CSI01 and CSI11 cannot communicate at different potential.