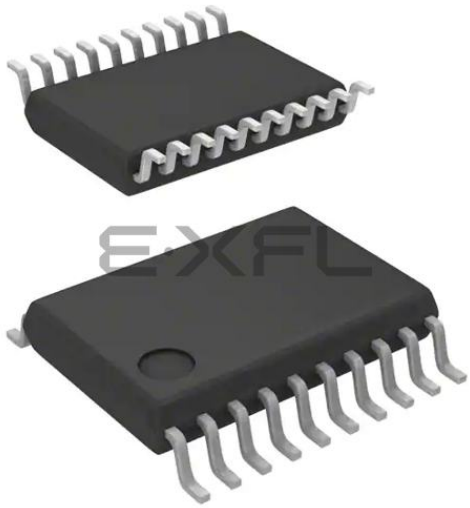
Renesas Electronics America Inc - R5F10266GSP#X0 Datasheet



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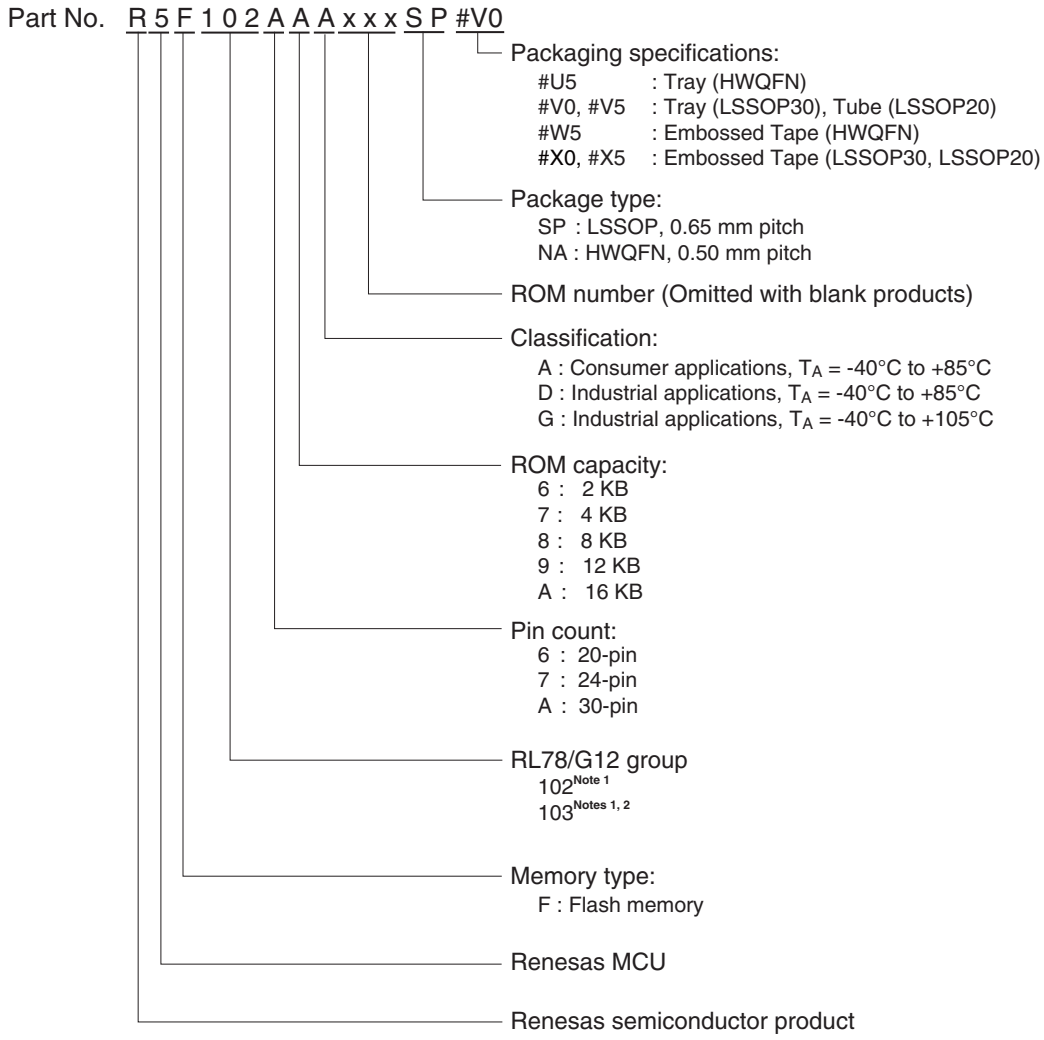
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10266gsp-x0

1.3 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G12

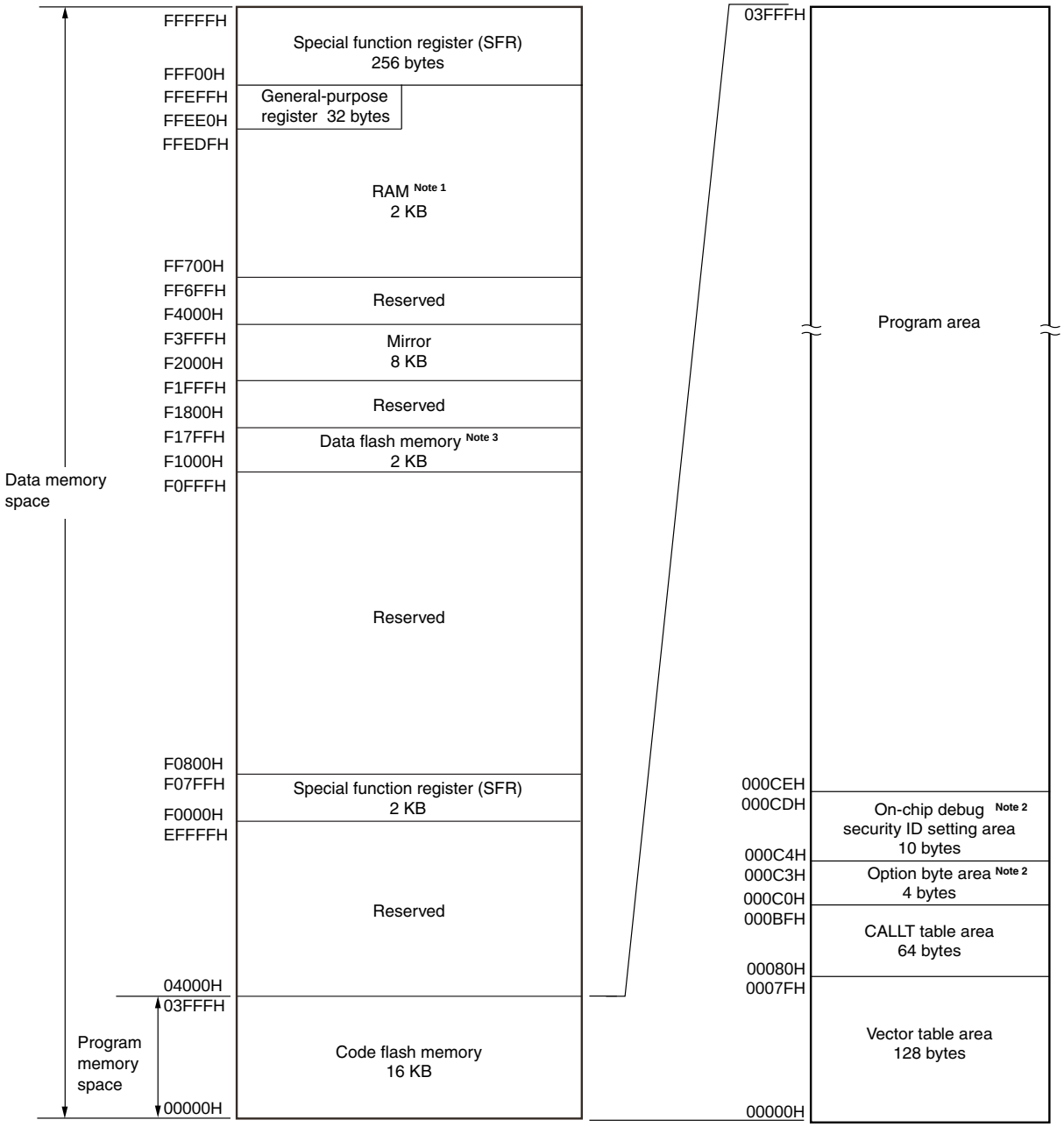
<R>



Notes 1. For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.1 Differences between the R5F102 Products and the R5F103 Products**.

2. Products only for "A: Consumer applications (T_A = -40 to +85°C)" and "D: Industrial applications (T_A = -40 to +85°C)"

Figure 3-6. Memory Map for the R5F10xAA (x = 2 or 3)



<R> **Notes 1.** Do not allocate the stack area, data buffers for use by the flash library, arguments of library functions, branch destinations in the processing of vectored interrupts, or destinations or sources for DMA transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory.

2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

4. The areas are reserved in the R5F103AA.

Caution While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area +10 bytes when instructions are fetched from RAM areas, respectively. Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 21.3.2 RAM parity error detection.

Table 3-6. SFR List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	–	√	√	0000H
FFF45H		–			–	–		
FFF46H	Serial data register 03	RXD1/ SIO11	SDR03	R/W	–	√	√	0000H
FFF47H		–			–	–		
FFF48H	Serial data register 10	TXD2/ SIO20	SDR10	R/W	–	√	√	0000H
FFF49H		–			–	–		
FFF4AH	Serial data register 11	RXD2/ SIO21	SDR11	R/W	–	√	√	0000H
FFF4BH		–			–	–		
FFF50H	IICA shift register 0	IICA0		R/W	–	√	–	00H
FFF51H	IICA status register 0	IICS0		R	√	√	–	00H
FFF52H	IICA flag register 0	IICF0		R/W	√	√	–	00H
FFF64H	Timer data register 02	TDR02		R/W	–	–	√	0000H
FFF65H								
FFF66H	Timer data register 03	TDR03L	TDR03	R/W	–	√	√	00H
FFF67H		TDR03H			–	√		00H
FFF68H	Timer data register 04	TDR04		R/W	–	–	√	0000H
FFF69H								
FFF6AH	Timer data register 05	TDR05		R/W	–	–	√	0000H
FFF6BH								
FFF6CH	Timer data register 06	TDR06		R/W	–	–	√	0000H
FFF6DH								
FFF6EH	Timer data register 07	TDR07		R/W	–	–	√	0000H
FFF6FH								
FFF90H	Interval timer control register	ITMC		R/W	–	–	√	0FFFH
FFF91H								
FFFA0H	Clock operation mode control register	CMC		R/W	–	√	–	00H
FFFA1H	Clock operation status control register	CSC		R/W	√	√	–	C0H
FFFA2H	Oscillation stabilization time counter status register	OSTC		R	√	√	–	00H
FFFA3H	Oscillation stabilization time select register	OSTS		R/W	–	√	–	07H
FFFA4H	System clock control register	CKC		R/W	√	√	–	00H
FFFA5H	Clock output select register 0	CKS0		R/W	√	√	–	00H
FFFA6H	Clock output select register 1	CKS1		R/W	√	√	–	00H
FFFA8H	Reset control flag register	RESF		R	–	√	–	Undefined Note 1
FFFA9H	Voltage detection register	LVIM		R/W	√	√	–	00H Note 1
FFFAAH	Voltage detection level register	LVIS		R/W	√	√	–	00H/01H/81H Note 1
FFFABH	Watchdog timer enable register	WDTE		R/W	–	√	–	1A/9A Note 2
FFFACH	CRC input register	CRCIN		R/W	–	√	–	00H

4.5.3 Register setting examples for using the port and alternate functions

Table 4-7 shows register setting examples for used port and alternate functions. Set the registers used to control the port function as shown in Table 4-7. See the following remark for legends used in Table 4-7.

Remark –: Not applicable
×: don't care
PIORx: Peripheral I/O redirection register
POMxx: Port output mode register
PMCxx: Port mode control register
PMxx: Port mode register
Pxx: Port output latch
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).

Table 4-7. Setting Examples of Registers and Output Latches When Using Alternate Function (20-, 24-Pin Products) (1/5)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P00[Note 1]	P00	Input	–	–	–	1	×	–	–
		Output	–	–	–	0	0/1	–	–
	KR6	Input	–	–	–	1	×	–	–
	(SI01)[Note 2]	Input	PIOR3 = 1	–	–	1	×	–	–
P01[Note 1]	P01	Input	–	×	–	1	×	×	–
		Output	–	0	–	0	0/1	(SO01)/(SDA01) = 1	–
		N-ch open drain output	–	1	–	0	0/1		–
	KR7	Input	–	×	–	1	×	×	–
	(SO01)[Note 2]	Output	PIOR3 = 1	0/1	–	0	1	×	–
	(SDA01)[Note 2]	I/O	PIOR3 = 1	1	–	0	1	×	–
P02[Note 1]	P02	Input	–	–	–	1	×	×	–
		Output	–	–	–	0	0/1	(SCK01)/(SCL01) = 1	–
	KR8	Input	–	–	–	1	×	×	–
	(SCK01)[Note 2]	Input	PIOR3 = 1	–	–	1	×	×	–
		Output	PIOR3 = 1	–	–	0	1	×	–
	(SCL01)[Note 2]	Output	PIOR3 = 1	–	–	0	1	×	–
P03[Note 1]	P03	Input	–	–	–	1	×	–	–
		Output	–	–	–	0	0/1	–	–
	KR9	Input	–	–	–	1	×	–	–
P10	P10	Input	–	×	0	1	×	×	×
		Output	–	0	0	0	0/1	SCK00/ SCL00 = 1	PCLBZ0 = 0
		N-ch open drain output	–	1	0	0	0/1		
	ANI16	Input	–	×	1	1	×	×	×
	PCLBZ0	Output	–	0	0	0	0	SCK00/SCL00 = 1	×
	SCK00	Input	–	×	0	1	×	×	PCLBZ0 = 0
		Output	–	0/1	0	0	1	×	PCLBZ0 = 0
	SCL00[Note 2]	Output	–	0/1	0	0	1	×	PCLBZ0 = 0

Notes 1. Provided only in 24-pin products.
2. Provided only in the R5F102 products.

6.2 Configuration of Timer Array Unit

Timer array unit includes the following hardware.

Table 6-1. Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer/counter register 0n (TCR0n)
Register	Timer data register 0n (TDR0n)
Timer input	TI00 to TI07
Timer output	TO00 to TO07 pins, output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register 0 (TPS0) • Timer channel enable status register 0 (TE0) • Timer channel start register 0 (TS0) • Timer channel stop register 0 (TT0) • Timer input select register 0 (TIS0) • Timer output enable register 0 (TOE0) • Timer output register 0 (TO0) • Timer output level register 0 (TOL0) • Timer output mode register 0 (TOM0)
	<Registers of each channel> • Timer mode register 0n (TMR0n) • Timer status register 0n (TSR0n) • Noise filter enable register 1 (NFEN1) • Port mode control register (PMCxx)[Note] • Port mode register (PMxx)[Note] • Port register (Pxx)[Note]

Note The Port mode control register (PMCxx), port mode registers (PMxx), and port registers (Pxx) to be set differ depending on the product. For details, see **4.5.3 Register setting examples for using the port and alternate functions**.

Remark n: Channel number (n = 0 to 7)

Alternate port for timer I/O of the timer array unit channels varies depending on products.

Table 6-2. Timer I/O Pins in the Products

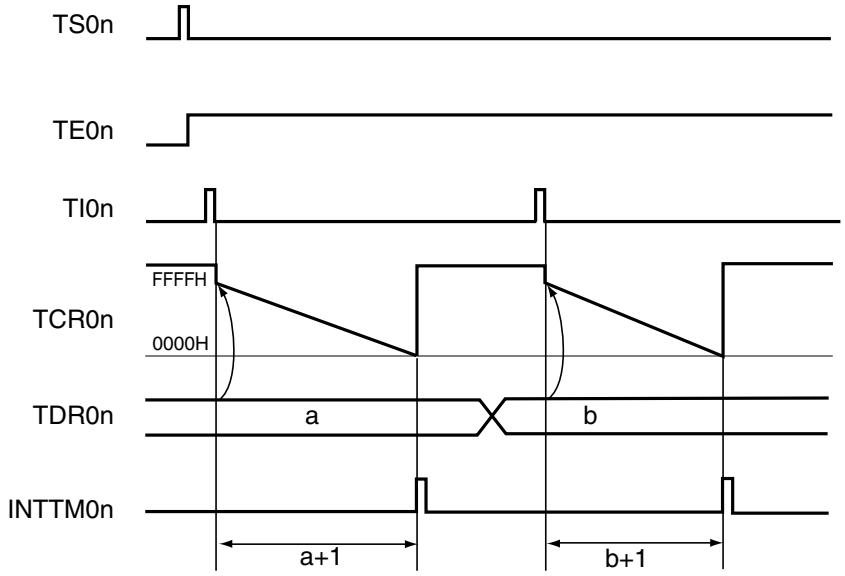
Timer array unit channel	30-pin products	20, 24-pin products
Channel 0	TI00/TO00	TI00/TO00
Channel 1	TI01/TO01	TI01/TO01
Channel 2	TI02/TO02	TI02/TO02
Channel 3	TI03/TO03	TI03/TO03
Channel 4	(TI04/TO04)	×
Channel 5	(TI05/TO05)	×
Channel 6	(TI06/TO06)	×
Channel 7	(TI07/TO07)	×

Remarks 1. If a pin is to be used for both timer input and timer output, it can be used only for timer input or timer output.

2. ×: The channel is not available

3. Pins in the parentheses indicate an alternate port when the bit 0 (PIOR0) of the peripheral I/O redirection register (PIOR) is set to "1" in 30-pin products.

Figure 6-59. Example of Basic Timing of Operation as Delay Counter



Remarks 1. n: Channel number (n = 0 to 7)

2. TS0n: Bit n of timer channel start register 0 (TS0)
TE0n: Bit n of timer channel enable status register 0 (TE0)
TI0n: TI0n pin input signal
TCR0n: Timer count register 0n (TCR0n)
TDR0n: Timer data register 0n (TDR0n)

8.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by the clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by the clock output select register 1 (CKS1).

8.4.1 Operation as output pin

The PCLBUZn pin is output as the following procedure.

<1> Set 0 in the bit of the port mode register (PMxx) and port register (Px) which correspond to the port which has a pin used as the PCLBUZn pin.

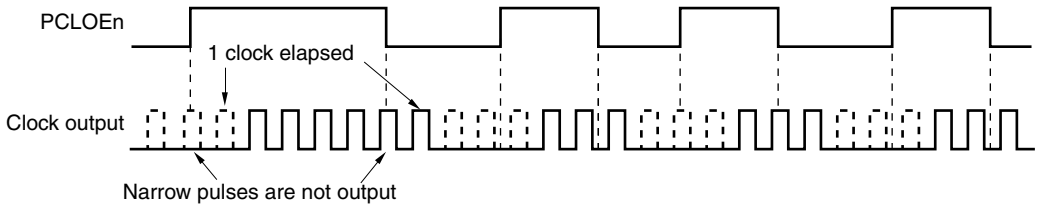
<2> Select the output frequency with bits 0 to 2 (CCSn0 to CCSn2) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled).

<3> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

Remarks 1. The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output. Figure 8-3 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

2. n = 0 or 1

Figure 8-3. Timing of Outputting Clock from PCLBUZn Pin



8.5 Cautions of Clock Output/Buzzer Output Controller

If STOP mode is entered within 1.5 clock cycles output from the PCLBUZn pin after the output is disabled (PCLOEn = 0), the PCLBUZn output width becomes shorter.

CHAPTER 10 A/D CONVERTER

The number of analog input channels of the A/D converter differs depending on the product.

	20- and 24-pin	30-pin
Analog input channels	11 ch (ANI0 to ANI3, ANI6 to ANI22)	8 ch (ANI0 to ANI3, ANI16 to ANI19)

10.1 Function of A/D Converter

The A/D converter converts analog input signals into digital values, and is configured to control analog inputs, including up to 11 channels of A/D converter analog inputs (ANI0 to ANI3 and ANI16 to ANI22). 10-bit or 8-bit resolution can be selected by using the ADTYP bit of the A/D converter mode register 2 (ADM2).

The A/D converter has the following function.

- **10-bit/8-bit resolution A/D conversion**
  10-bit or 8-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI3 and ANI16 to ANI22 (ANI0 to ANI3 and ANI16 to ANI19 for 30-pin products). Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated (when in the select mode).

Various A/D conversion modes can be specified by using the mode combinations below.

Trigger mode	Software trigger	Conversion is started by software.
	Hardware trigger no-wait mode	Conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	The power is turned on by detecting a hardware trigger while the system is off and in the conversion standby state, and conversion is then started automatically after the A/D power supply stabilization wait time passes. Select hardware trigger wait mode when using the SNOOZE mode function.
Channel selection mode	Select mode	A/D conversion is performed on the analog input of one channel.
	Scan mode	A/D conversion is performed on the analog input of four channels in order. ANI0 to ANI3 can be selected as analog input.
Conversion operation mode	One-shot conversion mode	A/D conversion is performed on the selected channel once.
	Sequential conversion mode	A/D conversion is sequentially performed on the selected channels until it is stopped by software.
Operation voltage mode	Normal 1 or normal 2 mode	Conversion is done in the operation voltage range of 2.7 V ≤ V_{DD} ≤ 5.5 V.
	Low-voltage 1 or low-voltage 2 mode	Conversion is done in the operation voltage range of 1.8 V ≤ V_{DD} ≤ 5.5 V. Select this mode for conversion at a low voltage. Because the operation voltage is low, it is internally boosted during conversion.
Sapling time selection	Sampling clock cycles: 7 f_{AD}	The sampling time in normal 1 or low-voltage 1 mode is seven cycles of the conversion clock (f_{AD}). Select this mode when the output impedance of the analog input source is high and a longer sampling time is required.
	Sampling clock cycles: 5 f_{AD}	The sampling time in normal 2 or low-voltage 2 mode is five cycles of the conversion clock (f_{AD}). Select this mode when enough sampling time is ensured (for example, when the output impedance of the analog input source is low).

11.3.14 Serial standby control register 0 (SSC0)

The SSC0 register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

The SSC0 register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSC0 register can be set with an 8-bit memory manipulation instruction as SSC0L.

Reset signal generation clears the SSC0 register to 0000H.

Caution The maximum transfer rate in the SNOOZE mode is as follows.

- When using CSI00: Up to 1 Mbps
- When using UART0: 4800 bps only

Figure 11-20. Format of Serial Standby Control Register 0 (SSC0)

Address: F0138H, F0139H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSCm	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSEC0	SWC0

SSEC0	Selection of whether to enable or disable the generation of communication error interrupts in the SNOOZE mode
0	Enable the generation of error interrupts (INTSRE0).
1	Stop the generation of error interrupts (INTSRE0).
• The SSEC0 bit can be set to 1 or 0 only when both the SWC0 and EOC01 bits are set to 1 during UART reception in the SNOOZE mode. In other cases, clear the SSEC0 bit to 0. • Setting SSEC0, SWC0 = 1, 0 is prohibited.	

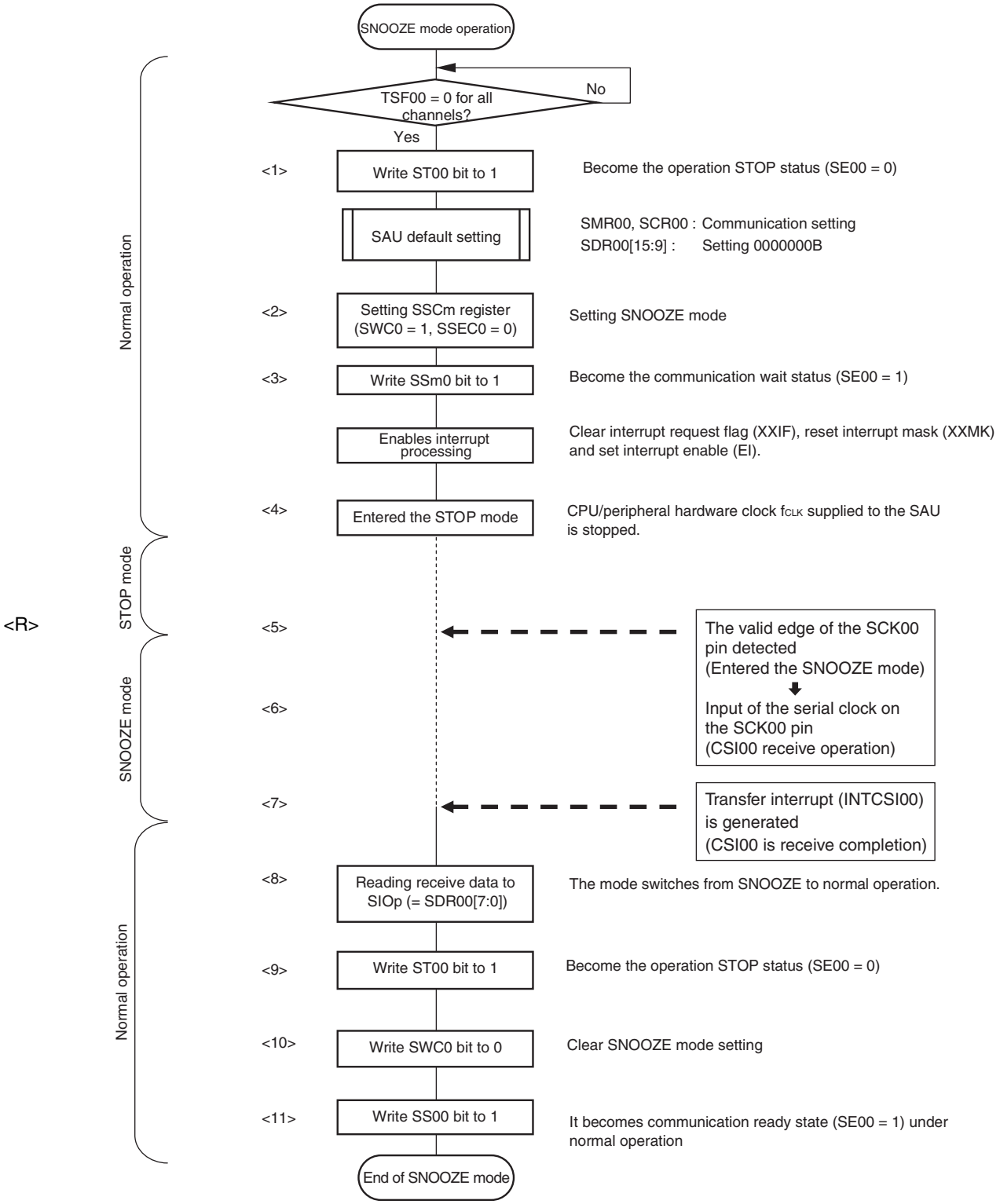
SWC0	Setting the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.
• When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode). • The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited. • Even when using SNOOZE mode, be sure to set the SWC0 bit to 0 in normal operation and change it to 1 just before shifting to STOP mode. Also, be sure to change the SWC0 bit to 0 after returning from STOP mode to normal operation.	

Figure 11-21. Interrupt in UART Reception Operation in SNOOZE Mode

EOC01 Bit	SSEC0 Bit	Reception Ended Successfully	Reception Ended in an Error
0	0	INTSR0 is generated.	INTSR0 is generated.
0	1	INTSR0 is generated.	INTSR0 is generated.
1	0	INTSR0 is generated.	INTSRE0 is generated.
1	1	INTSR0 is generated.	No interrupt is generated.

Remark <1> to <11> in the figure correspond to <1> to <11> in **Figure 11-72 Flowchart of SNOOZE Mode Operation (once startup)**.

Figure 11-72. Flowchart of SNOOZE Mode Operation (once startup)



<R>

Remark <1> to <11> in the figure correspond to <1> to <11> in **Figure 11-71 Timing Chart of SNOOZE Mode Operation (once startup)**.

11.7.3 Data reception

Data reception is an operation to receive data to the target for transfer (slave) after transmission of an address field. After all data are received to the slave, a stop condition is generated and the bus is released.

Simplified I^2C	IIC00	IIC01	IIC11	IIC20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1
Pins used	SCL00, SDA00Note 1	SCL01, SDA01Note 1	SCL11, SDA11Note 1	SCL20, SDA20Note 1
Interrupt	INTIIC00	INTIIC01	INTIIC11	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)			
Error detection flag	ACK error detection flag (OVFmn)			
Transfer data length	8 bits			
Transfer rateNote 2	Max. f_{MCK}/4 [Hz] (SDRmn[15:9] = 1 or more) f_{MCK}: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (fast mode) • Max. 100 kHz (standard mode)			
Data level	Non-inversion output (default: high level)			
Parity bit	No parity bit			
Stop bit	Appending 1 bit (ACK transmission)			
Data direction	MSB first			

Notes 1. To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POMxx = 1 (POM11, POM41 = 1 for 20- or 24- pin products, POM11, POM14, POM50 = 1 for 30-pin products)) for the port output mode registers (POMxx). For details, see **4.3 Registers Controlling Port Function** and **4.5 Register Settings When Using Alternate Function**.
When IIC00 and IIC20 is communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POMxx = 1 (POM10 = 1 for 20- or 24- pin products, POM10, POM15 = 1 for 30-pin products)) also for the clock input/output pins (SCL00, SCL20). For details, see **4.4.4 Handling different potentials (1.8 V, 2.5 V, and 3 V) by using I/O buffers**.

2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: T_A = -40 to +85°C)** or **CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)**).

Remark m: Unit number, n: Channel number (mn = 00, 01, 03, 10)

12.3.2 IICA control register 00 (IICCTL00)

This register is used to enable/stop I^2C operations, set wait timing, and set other I^2C operations.

The IICCTL00 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIE0, WTIM0, and ACKE0 bits while IICE0 = 0 or during the wait period. These bits can be set at the same time when the IICE0 bit is set from "0" to "1".

Reset signal generation clears this register to 00H.

Figure 12-6. Format of IICA Control Register 00 (IICCTL00) (1/4)

Address: F0230H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICCTL00	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I^2C operation enable
0	Stop operation. Reset the IICA status register 0 (IICS0) Note 1. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCLA0 and SDAA0 lines are at high level.	
Condition for clearing (IICE0 = 0)	Condition for setting (IICE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0 Notes 2, 3	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLA0 and SDAA0 lines are set to high impedance. The following flags of IICA control register 00 (IICCTL00) and the IICA status register 0 (IICS0) are cleared to 0. • STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 = 0)	Condition for setting (LREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL0 Notes 2, 3	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When the WREL0 bit is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDAA0 line goes into the high impedance state (TRC0 = 0).	
Condition for clearing (WREL0 = 0)	Condition for setting (WREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

(**Notes** and **Caution** are listed on the next page.)

Figure 12-6. Format of IICA Control Register 00 (IICCTL00) (4/4)

SPT0 [Note]	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer).

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when the ACKE0 bit has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A stop condition cannot be generated normally during the acknowledge period. Therefore, set it during the wait period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as start condition trigger (STT0).
- The SPT0 bit can be set to 1 only when in master mode.
- When the WTIM0 bit has been cleared to 0, if the SPT0 bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock. The WTIM0 bit should be changed from 0 to 1 during the wait period following the output of eight clocks, and the SPT0 bit should be set to 1 during the wait period that follows the output of the ninth clock.
- Setting the SPT0 bit to 1 and then setting it again before it is cleared condition is prohibited.

Condition for clearing (SPT0 = 0)	Condition for setting (SPT0 = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • Cleared by LREL0 = 1 (exit from communications) • When IICE0 = 0 (operation stop) • Reset	• Set by instruction

Note The value read from the STT0 bit is always 0.

Caution When bit 3 (TRC0) of the IICA status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of IICA control register 00 (IICCTL00) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while the TRC0 bit is 1 (transmission status) by writing to the IICA shift register 0.

Remark Bit 0 (SPT0) becomes 0 when it is read after data setting.

The meanings of <1> to <7> in (1) Start condition ~ address ~ data in Figure 12-33 are explained below.

<1> The start condition trigger is set by the master device (STT0 = 1) and a start condition (i.e. SCLA0 =1 changes SDAA0 from 1 to 0) is generated once the bus data line goes low (SDAA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS0 = 1). The master device is ready to communicate once the bus clock line goes low (SCLA0 = 0) after the hold time has elapsed.

<2> The master device writes the address + R (reception) to the IICA shift register 0 (IICA0) and transmits the slave address.

<3> In the slave device if the address received matches the address (SVA0 value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)[Note].

<5> The timing at which the master device sets the wait status changes to the 8th clock (WTIM0 = 0).

<6> The slave device writes the data to transmit to the IICA0 register and releases the wait status that it set by the slave device.

<7> The master device releases the wait status (WREL0 = 1) and starts transferring data from the slave device to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 12-33 show descriptions the entire procedure for communicating data using the I^2C bus.

Figure 12-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 12-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 12-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

14.2 Configuration of DMA Controller

The DMA controller includes the following hardware.

Table 14-1. Configuration of DMA Controller

Item	Configuration
Address registers	• DMA SFR address registers 0, 1 (DSA0, DSA1) • DMA RAM address registers 0, 1 (DRA0, DRA1)
Count register	• DMA byte count registers 0, 1 (DBC0, DBC1)
Control registers	• DMA mode control registers 0, 1 (DMC0, DMC1) • DMA operation control register 0, 1 (DRC0, DRC1)

14.2.1 DMA SFR address register n (DSAn)

This is an 8-bit register that is used to set an SFR address that is the transfer source or destination of DMA channel n.

Set the lower 8 bits of the SFR addresses FFF00H to FFFFFH.

This register is not automatically incremented but fixed to a specific value.

In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DSAn register can be read or written in 8-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 00H.

Figure 14-1. Format of DMA SFR Address Register n (DSAn)

Address: FFFB0H (DSA0), FFFB1H (DSA1) After reset: 00H R/W

	7	6	5	4	3	2	1	0
DSAn								

Remark n: DMA channel number (n = 0, 1)

16.2 Configuration of Key Interrupt

The key interrupt includes the following hardware.

Table 16-2. Configuration of Key Interrupt

Item	Configuration
Control register	Key return control register (KRCTL) Key return mode control registers (KRM0, KRM1) Key return flag register (KRF) Port mode registers 0, 4, 6 (PM0, PM4, PM6)

16.3 Register Controlling Key Interrupt

The key interrupt function is controlled by the following registers:

- Key return control register (KRCTL)
- Key return mode control registers (KRM0, KRM1)
- Key return flag register (KRF)
- Port mode registers 0, 4, 6 (PM0, PM4, PM6)

16.3.1 Key return control register (KRCTL)

This register controls the usage of the key interrupt flags (KRF0 to KRF5) and sets the detection edge.

The KRCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16-2. Format of Key Return Control Register (KRCTL)

Address: FFF34H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRCTL	KRMD	0	0	0	0	0	0	KREG

KRMD	Usage of Key Interrupt Flags (KRF0 to KRF5)
0	Does not use key interrupt flags
1	Uses key interrupt flags

KRRG	Selection of Detection Edge (KR0 to KR9)
0	Falling edge
1	Rising edge

KRMD	KREG	Interrupt Function
0	0	Generates a key interrupt (INTKR) when detecting a falling edge. (Identify the channel by checking the port level).
0	1	Generates a key interrupt (INTKR) when detecting a rising edge. (Identify the channel by checking the port level).
1	0	Generates a key interrupt (INTKR) when detecting a falling edge. (Identify the channel by using the key interrupt flags (KRF0 to KRF5)).
1	1	Generates a key interrupt (INTKR) when detecting a rising edge. (Identify the channel by using the key interrupt flags (KRF0 to KRF5)).

24.4.3 Selecting communication mode

Communication modes of the RL78 microcontroller are as follows.

Table 24-6. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used
	Port	Speed [Note 2]	Frequency	Multiply Rate	
1-line UART (when flash memory programmer is used, or when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	–	–	TOOL0
Dedicated UART (when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	–	–	TOOLTxD, TOOLRxD

Notes 1. Selection items for standard settings on GUI of the flash memory programmer.

2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

24.4.4 Communication commands

The RL78 microcontroller executes serial programming through the commands listed in **Table 24-7.**

The signals sent from the dedicated flash memory programmer or external device to the RL78 microcontroller are called commands, and programming functions corresponding to the commands are executed. For details, refer to the **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

Table 24-7. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory. [Note]
Getting information	Silicon Signature	Gets the RL78 microcontroller information (such as the part number and flash memory configuration, firmware version).
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
	Security Get	Gets security information.
	Security Release	Releases the write prohibition setting.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

Note Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

Table 27-5. Operation List (10/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	CMP	A, #byte	2	1	–	A – byte	×	×	×
		!addr16, #byte	4	1	4	(addr16) – byte	×	×	×
		ES:!addr16, #byte	5	2	5	(ES:addr16) – byte	×	×	×
		saddr, #byte	3	1	–	(saddr) – byte	×	×	×
		A, r Note3	2	1	–	A – r	×	×	×
		r, A	2	1	–	r – A	×	×	×
		A, !addr16	3	1	4	A – (addr16)	×	×	×
		A, ES:!addr16	4	2	5	A – (ES:addr16)	×	×	×
		A, saddr	2	1	–	A – (saddr)	×	×	×
		A, [HL]	1	1	4	A – (HL)	×	×	×
		A, ES:[HL]	2	2	5	A – (ES:HL)	×	×	×
		A, [HL+byte]	2	1	4	A – (HL+byte)	×	×	×
		A, ES:[HL+byte]	3	2	5	A – ((ES:HL)+byte)	×	×	×
		A, [HL+B]	2	1	4	A – (HL+B)	×	×	×
		A, ES:[HL+B]	3	2	5	A – ((ES:HL)+B)	×	×	×
		A, [HL+C]	2	1	4	A – (HL+C)	×	×	×
		A, ES:[HL+C]	3	2	5	A – ((ES:HL)+C)	×	×	×
	CMP0	A	1	1	–	A – 00H	×	0	0
		X	1	1	–	X – 00H	×	0	0
		B	1	1	–	B – 00H	×	0	0
		C	1	1	–	C – 00H	×	0	0
		!addr16	3	1	4	(addr16) – 00H	×	0	0
		ES:!addr16	4	2	5	(ES:addr16) – 00H	×	0	0
		saddr	2	1	–	(saddr) – 00H	×	0	0
	CMPS	X, [HL+byte]	3	1	4	X – (HL+byte)	×	×	×
		X, ES:[HL+byte]	4	2	5	X – ((ES:HL)+byte)	×	×	×

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3			1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±0.35	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±2.0	LSB
Analog input voltage	VAIN	ANI16 to ANI22		0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.