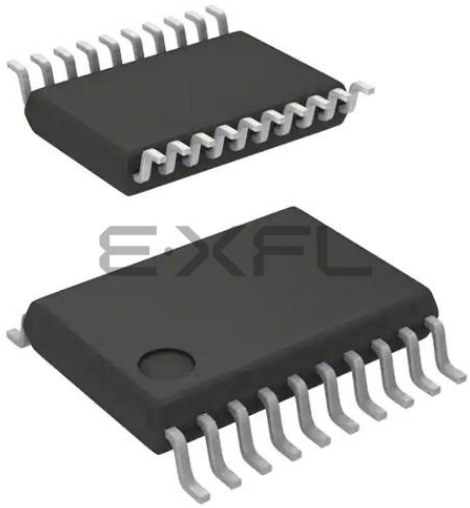

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Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10268dsp-x0

2.2.2 Description of Functions

Function Name	I/O	Functions
ANI0 to ANI3, ANI16 to ANI22	input	Analog input pins of A/D converter (see **Figure 10-44 Analog Input Pin Connection**)
AV_{REFP}	input	Inputs the A/D converter reference potential (+ side)
AV_{REFM}	input	Inputs the A/D converter reference potential (− side)
INTP0 to INTP5	input	External interrupt request input Specified available edge : rising edge, falling edge, or both rising and falling edges
KR0 to KR9	input	Key interrupt input
PCLBUZ0, PCLBUZ1	output	Clock/buzzer output
REGC	−	Connecting regulator output stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF)
$\overline{RESET}$	input	External reset input for low level active When the external reset pin is not used, connect this pin directly or via a resistor to V_{DD}.
RxD0 to RxD2	input	Serial data input for serial interfaces UART0, UART1, and UART2
TxD0 to TxD2	output	Serial data output for serial interfaces UART0, UART1, and UART2
SCK00, SCK01, SCK11, SCK20	I/O	Serial clock I/O for serial interfaces CSI00, CSI01, CSI11, and CSI20
SI00, SI01, SI11, SI20	input	Serial data input for serial interfaces CSI00, CSI01, CSI11, and CSI20
SO00, SO01, SO11, SO20	output	Serial data output for serial interfaces CSI00, CSI01, CSI11, and CSI20
SCLA0	I/O	Serial clock I/O for serial interface IICA
SDAA0	I/O	Serial data I/O for serial interface IICA
SCL00, SCL01, SCL11, SCL20	output	Clock output for simplified I^2C serial interfaces IIC00, IIC01, IIC11, IIC20
SDA00, SDA01, SDA11, SDA20	I/O	Serial data I/O for simplified I^2C serial interfaces IIC00, IIC01, IIC11, IIC20
TI00 to TI07	input	Inputting an external count clock/capture trigger to 16-bit timers 00 to 07
TO00 to TO07	output	Timer output pins of 16-bit timers 00 to 07
X1, X2	−	Connecting a resonator for main system clock
EXCLK	input	External clock input pin for main system clock
V_{DD}	−	Positive power supply
V_{SS}	−	Ground potential
TOOLRxD	input	This UART serial data input pin for an external device connection is used during flash memory programming
TOOLTxD	output	This UART serial data output pin for an external device connection is used during flash memory programming
TOOL0	I/O	Data I/O pin for a flash memory programmer/debugger

Caution The following shows the relationship between P40/TOOL0 and the operation mode when reset is released.

Table 2-1. Relationship between P40/TOOL0 and the Operation Mode When Reset Is Released

P40/TOOL0	Operation mode
V_{DD}	Normal operation mode
0 V	Flash memory programming mode

For details, see **24.4 Serial Programming Method**.

Remark Use bypass capacitors (about 0.1 μF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS} lines.

5.3.3 Clock operation status control register (CSC)

This register is used to control the operations of the high-speed system clock and high-speed on-chip oscillator clock, (except the low-speed on-chip oscillator clock).

The CSC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to C0H.

Figure 5-4. Format of Clock Operation Status Control Register (CSC)

Address: FFFA1H After reset: C0H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
CSC	MSTOP	1	0	0	0	0	0	HIOSTOP

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	Input port
1	X1 oscillator stopped	External clock from EXCLK pin is invalid	

HIOSTOP	High-speed on-chip oscillator clock operation control
0	High-speed on-chip oscillator operating
1	High-speed on-chip oscillator stopped

Cautions 1. After reset release, set the clock operation mode control register (CMC) before setting the CSC register.

2. Set the oscillation stabilization time select register (OSTS) before setting the MSTOP bit to 0 after releasing reset. Note that if the OSTS register is being used with its default settings, the OSTS register is not required to be set here.

3. To start X1 oscillation as set by the MSTOP bit, check the oscillation stabilization time of the X1 clock by using the oscillation stabilization time counter status register (OSTC).

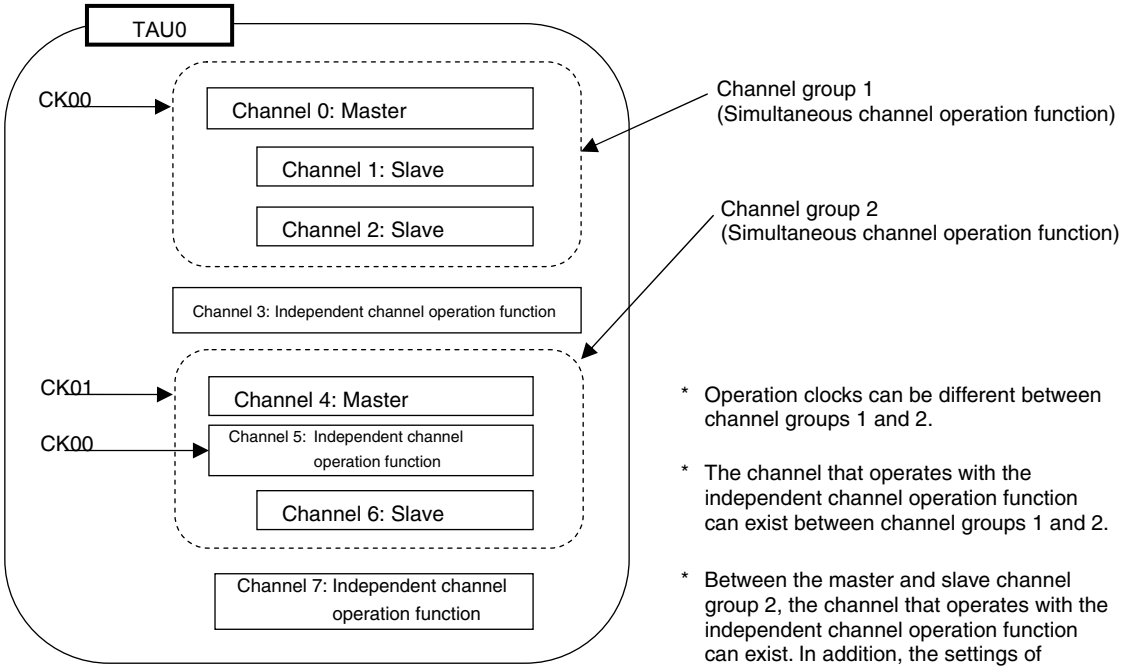
4. Do not stop the clock selected for the CPU peripheral hardware clock (f_{CLK}) with the CSC register.

<R> **5.** The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 5-2. Before stopping the clock oscillation, check the conditions before the clock oscillation is stopped.

Table 5-2. Stopping Clock Method

Clock	Condition Before Stopping Clock (Invalidating External Clock Input)	Setting of CSC Register Flags
X1 clock External main system clock	CPU and peripheral hardware clocks operate with a high-speed on-chip oscillator clock. (MCS = 0)	MSTOP = 1
High-speed on-chip oscillator clock	CPU and peripheral hardware clocks operate with a high-speed system clock.(MCS = 1)	HIOSTOP = 1

Example



* Operation clocks can be different between channel groups 1 and 2.
* The channel that operates with the independent channel operation function can exist between channel groups 1 and 2.
* Between the master and slave channel group 2, the channel that operates with the independent channel operation function can exist. In addition, the settings of operation clocks can be performed individually.

Figure 6-40. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (2/2)

(d) Timer output level register 0 (TOL0)

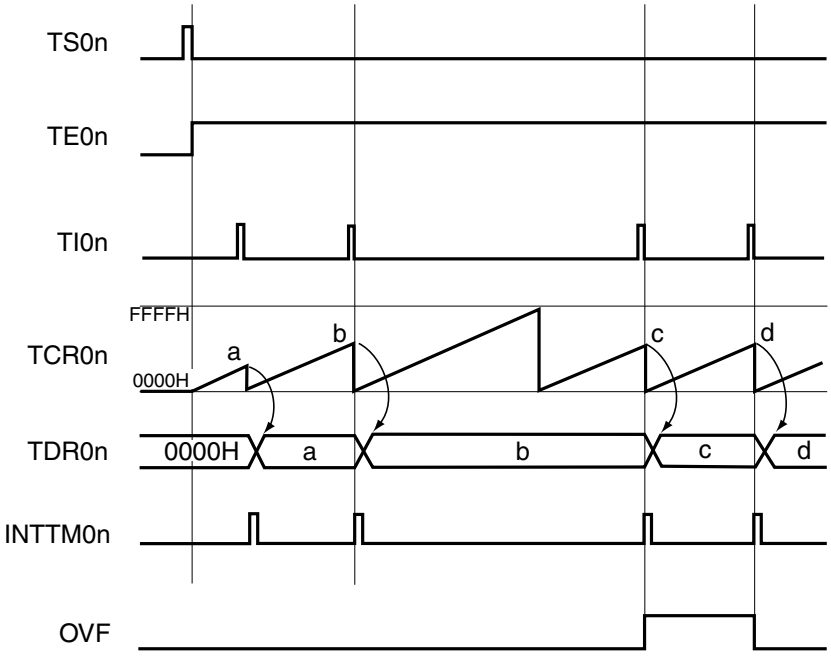
	Bit n	
TOL0	TOL0n 0	0: Cleared to 0 when master channel output mode (TOM0n = 0)

(e) Timer output mode register 0 (TOM0)

	Bit n	
TOM0	TOM0n 0	0: Sets master channel output mode.

Remark n: Channel number (n = 0 to 7)

Figure 6-51. Example of Basic Timing of Operation as Input Pulse Interval Measurement (MD0n0 = 0)



Remarks 1. n: Channel number (n = 0 to 7)

2. TS0n: Bit n of timer channel start register 0 (TS0)
TE0n: Bit n of timer channel enable status register 0 (TE0)
TI0n: TI0n pin input signal
TCR0n: Timer count register 0n (TCR0n)
TDR0n: Timer data register 0n (TDR0n)
OVF: Bit 0 of timer status register 0n (TSR0n)

Table 10-3. A/D Conversion Time Selection (1/4)

(1) When there is no A/D power supply stabilization wait time
Normal mode 1 or 2 (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock Note	Conversion Time	Conversion Time at 10-Bit Resolution					
									2.7 V ≤ V_{DD} ≤ 5.5 V					
FR2	FR1	FR0	LV1	LV0					f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	0	0	0	Normal 1	f_{CLK}/64	19 f_{AD} (number of sampling clock: 7 f_{AD})	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	76 μs	50.67 μs
0	0	1				f_{CLK}/32		608/f_{CLK}				76 μs	38 μs	25.33 μs
0	1	0				f_{CLK}/16		304/f_{CLK}			76 μs	38 μs	19 μs	12.67 μs
0	1	1				f_{CLK}/8		152/f_{CLK}		76 μs	38 μs	19 μs	9.5 μs	6.33 μs
1	0	0				f_{CLK}/6		114/f_{CLK}		57 μs	28.5 μs	14.25 μs	7.125 μs	4.75 μs
1	0	1				f_{CLK}/5		95/f_{CLK}	95 μs	47.5 μs	23.75 μs	11.875 μs	5.938 μs	3.96 μs
1	1	0				f_{CLK}/4		76/f_{CLK}	76 μs	38 μs	19 μs	9.5 μs	4.75 μs	3.17 μs
1	1	1				f_{CLK}/2		38/f_{CLK}	38 μs	19 μs	9.5 μs	4.75 μs	2.375 μs	Setting prohibited
0	0	0	0	1	Normal 2	f_{CLK}/64	17 f_{AD} (number of sampling clock: 5 f_{AD})	1088/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	68 μs	45.33 μs
0	0	1				f_{CLK}/32		544/f_{CLK}				68 μs	34 μs	22.67 μs
0	1	0				f_{CLK}/16		272/f_{CLK}			68 μs	34 μs	17 μs	11.33 μs
0	1	1				f_{CLK}/8		136/f_{CLK}		68 μs	34 μs	17 μs	8.5 μs	5.67 μs
1	0	0				f_{CLK}/6		102/f_{CLK}		51 μs	25.5 μs	12.75 μs	6.375 μs	4.25 μs
1	0	1				f_{CLK}/5		85/f_{CLK}	85 μs	42.5 μs	21.25 μs	10.625 μs	5.3125 μs	3.54 μs
1	1	0				f_{CLK}/4		68/f_{CLK}	68 μs	34 μs	17 μs	8.5 μs	4.25 μs	2.83 μs
1	1	1				f_{CLK}/2		34/f_{CLK}	34 μs	17 μs	8.5 μs	4.25 μs	2.125 μs	Setting prohibited
Other than the above						–	–	–	Setting prohibited					

Note These are the numbers of clock cycles when conversion is with 10-bit resolution. When eight-bit resolution is selected, the values are shorter by two cycles of the conversion clock (f_{AD}).

Cautions 1. The A/D conversion time must be within the range of conversion times (t_{CONV}) described in 28.6.1 A/D converter characteristics or 29.6.1 A/D converter characteristics.

2. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the current data, stop A/D conversion once (ADCS = 0, ADCE = 0) beforehand.

3. The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

10.3.3 A/D converter mode register 1 (ADM1)

This register is used to specify the A/D conversion trigger, conversion mode, and hardware trigger signal.

The ADM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-6. Format of A/D Converter Mode Register 1 (ADM1)

Address: FFF32H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADCSM	0	0	0	ADTRS1	ADTRS0

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger mode
1	0	Hardware trigger no- wait mode
1	1	Hardware trigger wait mode

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	Count completion of timer channel 01 or capture completion interrupt signal (INTTM01)
1	1	12-bit interval timer interrupt signal (INTIT)
Other than above		Setting prohibited

Cautions 1. Only rewrite the value of the ADM1 register while conversion is stopped (ADCS = 0, ADCE = 0).

2. To complete A/D conversion, specify at least the following values as the hardware trigger interval:
Hardware trigger no-wait mode: 2 f_{CLK} clock + conversion start time + A/D conversion time
Hardware trigger wait mode: 2 f_{CLK} clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time

3. In modes other than SNOOZE mode, input of the next INTIT will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTIT is input.

Remarks 1. ×: don't care

2. f_{CLK}: CPU/peripheral hardware clock frequency

Figure 11-6. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	TMKAEN	0	ADCEN	IICA0EN	SAU1EN[Note]	SAU0EN	0	TAU0EN

SAU1EN	Control of serial array unit 1 clock supply
0	Stops clock supply (fixed as "0" in 20- or 24-pin products). • SFR used by serial array unit 1 cannot be written. • Serial array unit 1 is in the reset status.
1	Enables clock supply. • SFR used by serial array unit 1 can be read/written.

SAU0EN	Control of serial array unit 0 clock supply
0	Stops clock supply. • SFR used by serial array unit 0 cannot be written. • Serial array unit 0 is in the reset status.
1	Enables clock supply. • SFR used by serial array unit 0 can be read/written.

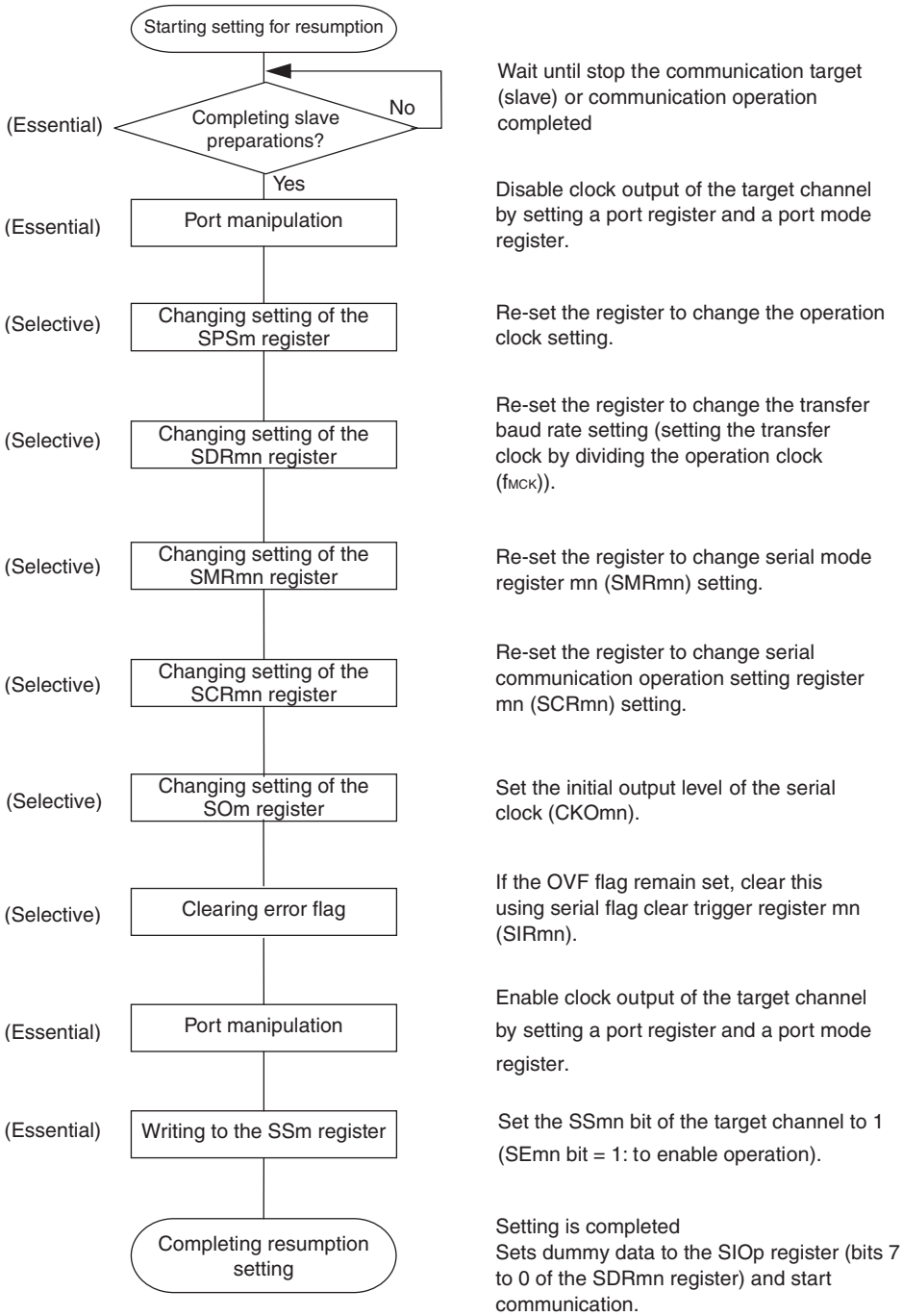
Note 30-pin products only.

Cautions 1. When setting serial array unit m, be sure to first set the following registers with the SAUmEN bit set to 1. If SAUmEN = 0, control registers of serial array unit m become default values and writing to them is ignored (except for the noise filter enable register 0 (NFEN0), port input mode registers 0, 1 (PIM0, PIM1), port output mode registers 0, 1, 4, 5 (POM0, POM1, POM4, POM5), port mode control registers 0, 1, 4 (PMC0, PMC1, PMC4), port mode registers 0, 1, 3 to 6 (PM0, PM1, PM3 to PM6), and port registers 0, 1, 3 to 6 (P0, P1, P3 to P6)).

- Serial clock select register m (SPSm)
- Serial mode register mn (SMRmn)
- Serial communication operation setting register mn (SCRmn)
- Serial data register mn (SDRmn)
- Serial flag clear trigger register mn (SIRmn)
- Serial status register mn (SSRmn)
- Serial channel start register m (SSm)
- Serial channel stop register m (STm)
- Serial channel enable status register m (SEm)
- Serial output enable register m (SOEm)
- Serial output level register m (SOLm)
- Serial output register m (SOm)
- Serial standby control register m (SSCm)

2. Be sure to clear the following bits to 0.
20, 24-pin products: bits 1, 3, 6
30-pin products: bits 1, 6

Figure 11-36. Procedure for Resuming Master Reception



Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

Figure 11-84. Example of Contents of Registers for UART Reception (UART0 to UART2) (2/2)

(e) Serial output register m (SOm) ... The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	1	CKOm1 ×	CKOm0 ×	0	0	0	0	SO03 Note ×	SO02 Note ×	SO01 ×	SOm0 ×

(f) Serial output enable register m (SOEm) ... The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOE03 Note ×	SOE02 Note ×	SOE01 ×	SOEm0 ×

(g) Serial channel start register m (SSm) ... Sets only the bits of the target channel is 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SS03 Note 0/1	SS02 Note ×	SSm1 0/1	SSm0 ×

Note Provided only in 30-pin product serial array unit 0.

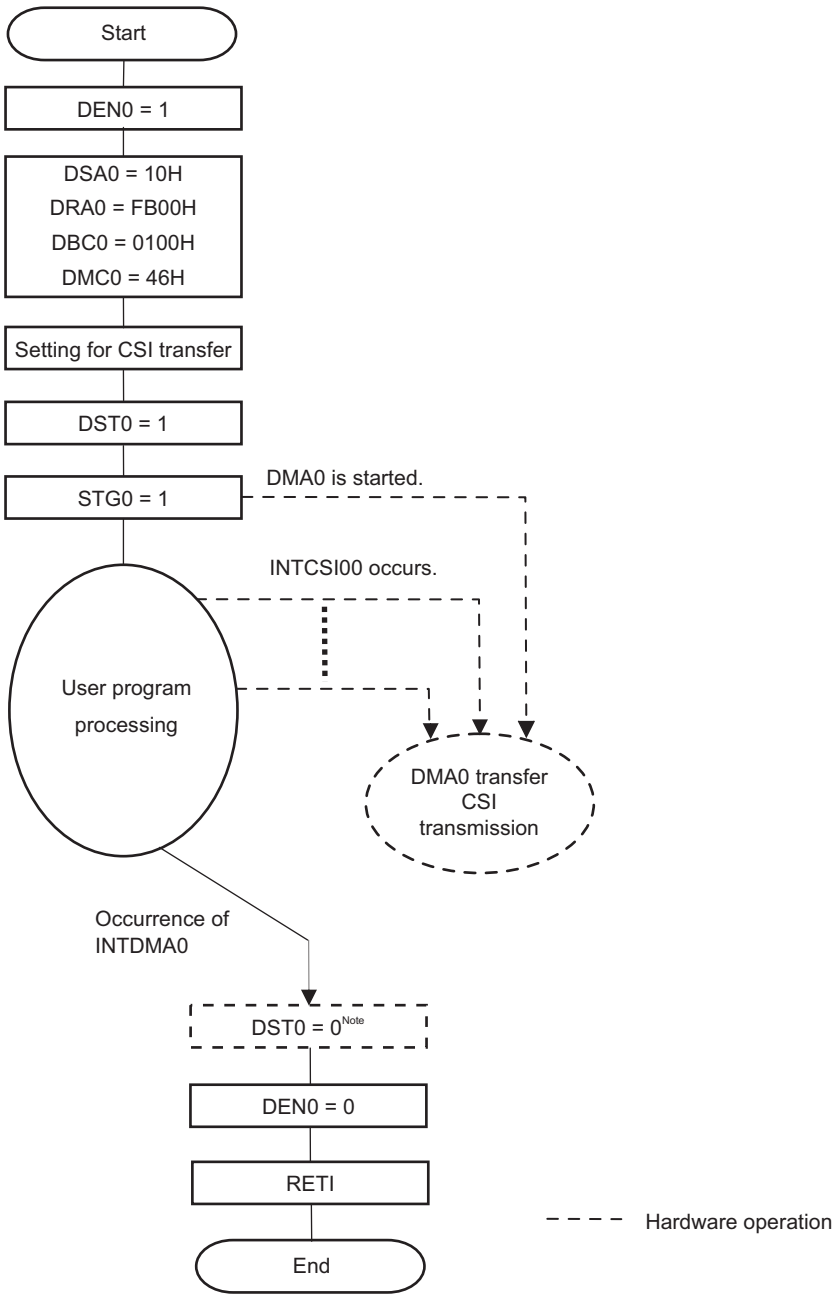
Remarks 1. m: Unit number (m = 0, 1)

2. ☐ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-7. Example of Setting for CSI Consecutive Transmission



Note The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **14.5.5 Forced termination by software**).

The first trigger for consecutive transmission is not started by the interrupt of CSI. In this example, it start by a software trigger.

CSI transmission of the second time and onward is automatically executed.

A DMA interrupt (INTDMA0) occurs when the last transmit data has been written to the data register.

Figure 15-6. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR10L, PR10H, PR11L) (20-, 24-pin product)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	DMAPR01[Note]	DMAPR00[Note]	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	DMAPR11	DMAPR10	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001	TMPR000	IICAPR00	TMPR003H	TMPR001H	SREPR00	SRPR00 CSIPR001[Note] IICPR001[Note]	STPR00 CSIPR000 IICPR000[Note]

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101	TMPR100	IICAPR10	TMPR103H	TMPR101H	SREPR10	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100

Address: FFFEAH After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	1	FLPR0	MDPR0	KRPR0	TMKAPR0	ADPR0	TMPR003	TMPR002

Address: FFFEEH After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	1	FLPR1	MDPR1	KRPR1	TMKAPR1	ADPR1	TMPR001	TMPR102

XXPR1X	XXPR0X	Priority Level Selection
0	0	Specifying level 0 (high priority)
0	1	Specifying level 1
1	0	Specifying level 2
1	1	Specifying level 3 (low priority)

Note Provided in the R5F102 products only.

Caution Be sure to set bits that are not available to the initial value.

15.3.4 External interrupt rising edge enable register (EGP0), external interrupt falling edge enable register (EGN0)

These registers specify the valid edge for INTP0 to INTP5.

The EGP0 and EGN0 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 15-8. Format of External Interrupt Rising Edge Enable Register (EGP0) and External Interrupt Falling Edge Enable Register (EGN0)

20-, 24-pin products

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	0	0	0	0	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	0	0	0	0	EGN3	EGN2	EGN1	EGN0

30-pin products

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 5)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution When the input port pins used for the external interrupt functions are switched to the output mode, the INTPn interrupt might be generated upon detection of a valid edge. When switching the input port pins to the output mode, set the port mode register (PMxx) to 0 after disabling the edge detection (by setting EGPn and EGNn to 0).

Remark n = 0 to 5

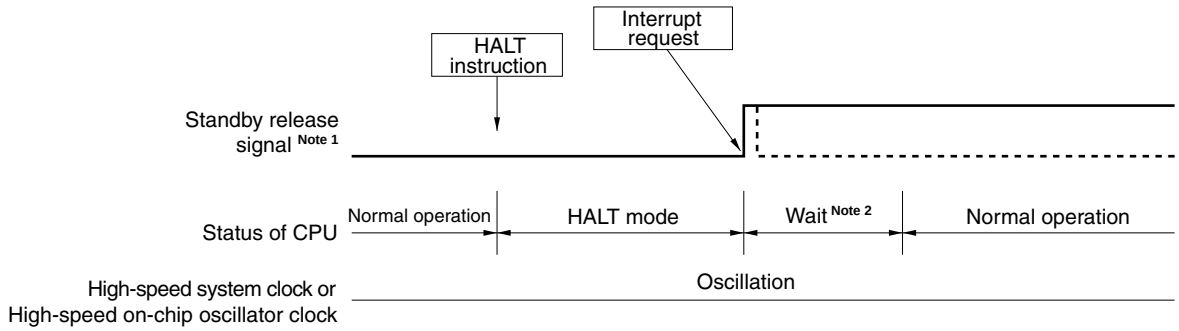
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 17-1. HALT Mode Release by Interrupt Request Generation



Notes 1. For details of the standby release signal, see **Figure 15-1 Basic Configuration of Interrupt Function**.

2. Wait time for HALT mode release

- When vectored interrupt servicing is carried out: 15 to 16 clocks
- When vectored interrupt servicing is not carried out: 9 to 10 clocks

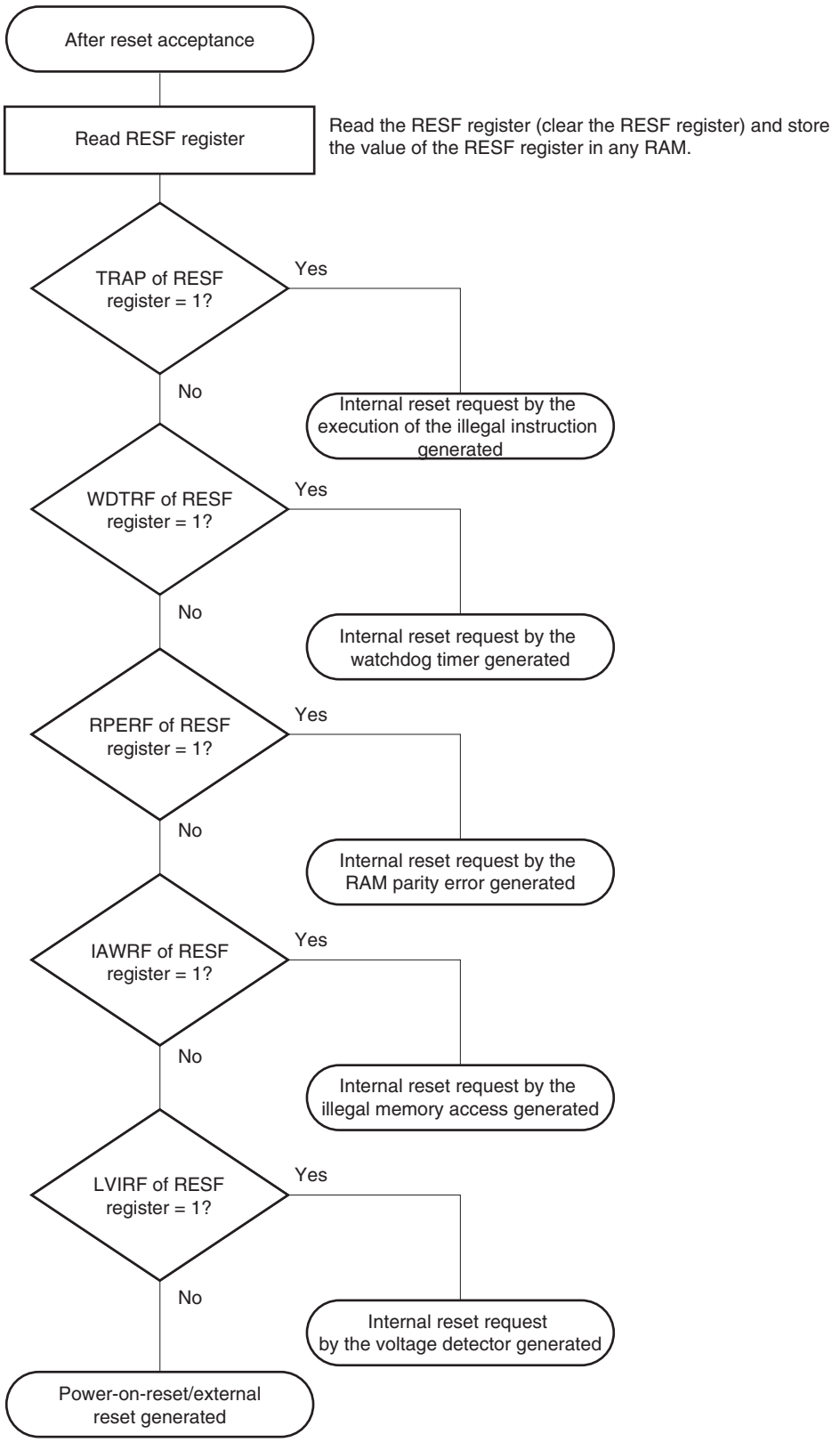
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

Table 17-2. Operating Statuses in STOP Mode

STOP Mode Setting / Item	When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
	When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock	Clock supply to the CPU is stopped		
Main system clock f_{IH} / f_X / f_{EX}	Stopped		
f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK = 1: Oscillates • WUTMMCK = 0 and WDTON = 0: Stops • WUTMMCK = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU	Operation stopped		
Code flash memory			
Data flash memory	Operation stopped		
RAM	Operation stopped		
Port (latch)	Status before STOP mode was set is retained		
Timer array unit	Operation disabled		
12-bit interval timer	Operable		
Watchdog timer	Set by bit 0 (WDSTBYON) of option byte (000C0H) • WDSTBYON = 0: Operation stopped • WDSTBYON = 1: Operation continues (cannot be stopped)		
Clock output/buzzer output	Operation disabled		
A/D converter	Wakeup operation is enabled (switching to the SNOOZE mode)		
Serial array unit (SAU)	Wakeup operation is enabled only for CSI00 and UART0 (switching to the SNOOZE mode) Operation is disabled for anything other than CSI00 and UART0		
Serial interface (IICA)	Wakeup by address match operable		
Multiplier and divider/multiply-accumulator	Operation disabled		
DMA controller			
Power-on-reset function	Operable		
Voltage detection function			
External interrupt			
Key interrupt function			
CRC operation function	Operation stopped		
RAM parity error detection function			
RAM guard function			
SFR guard function			
Illegal-memory access detection function			

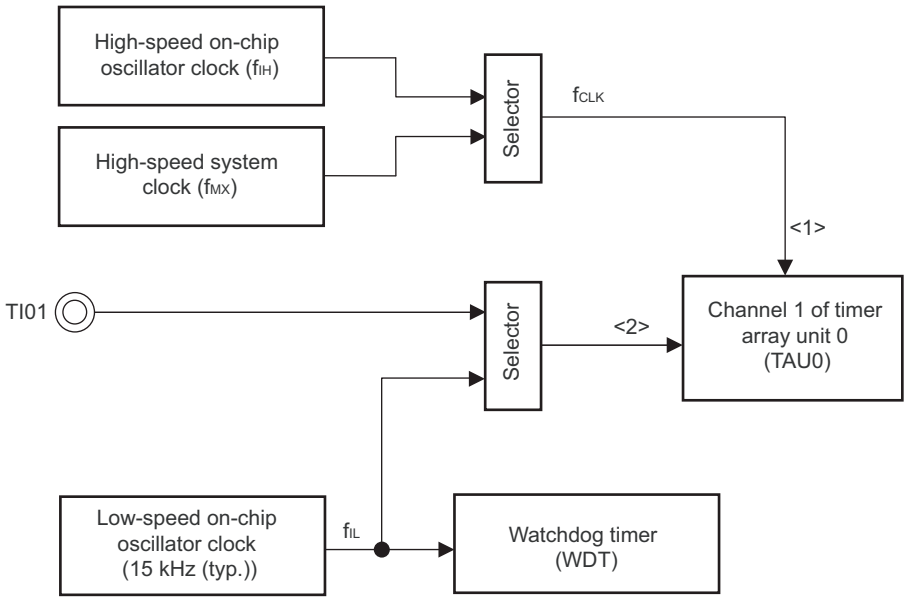
Remark Operation stopped: Operation is automatically stopped before switching to the STOP mode.
Operation disabled: Operation is stopped before switching to the STOP mode.
f_{IH}: High-speed on-chip oscillator clock
f_{IL}: Low-speed on-chip oscillator clock
f_X: X1 clock
f_{EX}: External main system clock

Figure 18-5. Procedure for Checking Reset Source



<R> The flow described above is an example of the procedure for checking.

Figure 21-10. Configuration of Frequency Detection Function



If input pulse interval measurement results in an abnormal value, it can be concluded that the clock frequency is abnormal.

For how to execute input pulse interval measurement, see **6.8.4 Operation as input pulse interval measurement**.

21.3.6.1 Timer input select register 0 (TIS0)

This register is used to select the timer input of channel 1 of the timer array unit 0 (TAU0) in 20- and 24-pin products.

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 21-11. Format of Timer Input Select Register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	0	0	0	TIS01	TIS00

TIS01	TIS00	Selection of timer input used with channel 1
×	0	Input signal of timer input pin (TI01)
0	1	Low-speed on-chip oscillator clock (fIL)
1	1	Setting prohibited

Remark ×: don't care

27.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

Table 27-2. Symbols in “Operation” Column

Symbol	Function
A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
ES	ES register
CS	CS register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
()	Memory contents indicated by address or register contents in parentheses
X_H, X_L X_S, X_H, X_L	16-bit registers: X_H = higher 8 bits, X_L = lower 8 bits 20-bit registers: X_S = (bits 19 to 16), X_H = (bits 15 to 8), X_L = (bits 7 to 0)
∧	Logical product (AND)
∨	Logical sum (OR)
∀	Exclusive logical sum (exclusive OR)
¯	Inverted data
addr5	16-bit immediate data (even addresses only in 0080H to 00BFH)
addr16	16-bit immediate data
addr20	20-bit immediate data
jdisp8	Signed 8-bit data (displacement value)
jdisp16	Signed 16-bit data (displacement value)

Table 27-5. Operation List (4/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	XCH	A, [HL+B]	2	2	–	A ←→ (HL+B)			
		A, ES:[HL+B]	3	3	–	A ←→ ((ES, HL)+B)			
		A, [HL+C]	2	2	–	A ←→ (HL+C)			
		A, ES:[HL+C]	3	3	–	A ←→ ((ES, HL)+C)			
	ONEB	A	1	1	–	A ← 01H			
		X	1	1	–	X ← 01H			
		B	1	1	–	B ← 01H			
		C	1	1	–	C ← 01H			
		!addr16	3	1	–	(addr16) ← 01H			
		ES:!addr16	4	2	–	(ES, addr16) ← 01H			
		saddr	2	1	–	(saddr) ← 01H			
	CLRB	A	1	1	–	A ← 00H			
		X	1	1	–	X ← 00H			
		B	1	1	–	B ← 00H			
		C	1	1	–	C ← 00H			
		!addr16	3	1	–	(addr16) ← 00H			
		ES:!addr16	4	2	–	(ES,addr16) ← 00H			
		saddr	2	1	–	(saddr) ← 00H			
	MOVS	[HL+byte], X	3	1	–	(HL+byte) ← X	×		×
		ES:[HL+byte], X	4	2	–	(ES, HL+byte) ← X	×		×
16-bit data transfer	MOVW	rp, #word	3	1	–	rp ← word			
		saddrp, #word	4	1	–	(saddrp) ← word			
		sfrp, #word	4	1	–	sfrp ← word			
		AX, rp Note 3	1	1	–	AX ← rp			
		rp, AX Note 3	1	1	–	rp ← AX			
		AX, !addr16	3	1	4	AX ← (addr16)			
		!addr16, AX	3	1	–	(addr16) ← AX			
		AX, ES:!addr16	4	2	5	AX ← (ES, addr16)			
		ES:!addr16, AX	4	2	–	(ES, addr16) ← AX			
		AX, saddrp	2	1	–	AX ← (saddrp)			
		saddrp, AX	2	1	–	(saddrp) ← AX			
		AX, sfrp	2	1	–	AX ← sfrp			
		sfrp, AX	2	1	–	sfrp ← AX			

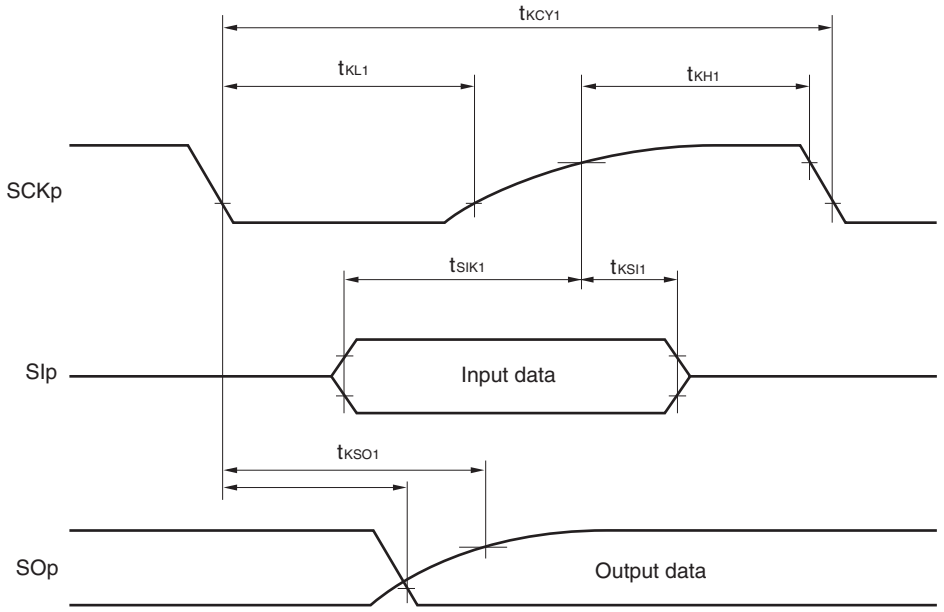
Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

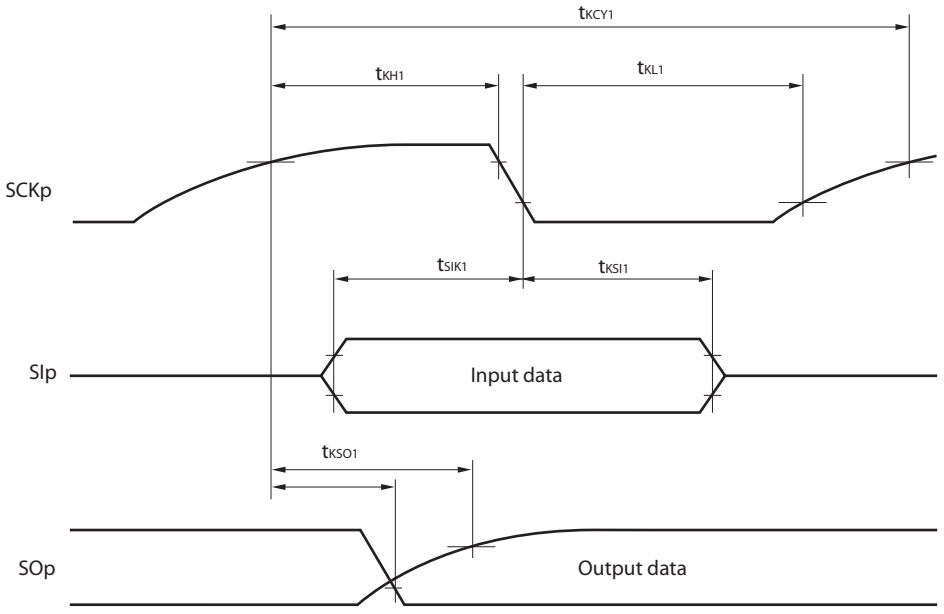
3. Except rp = AX

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)