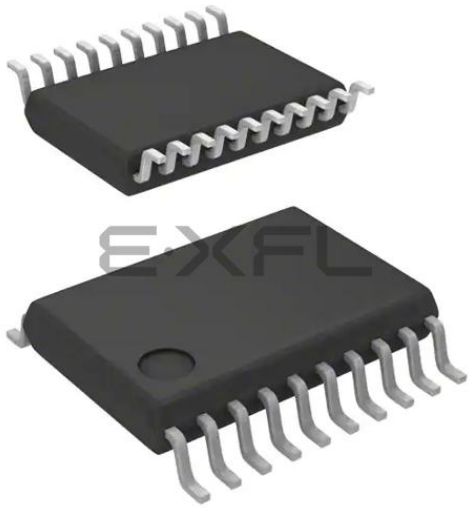

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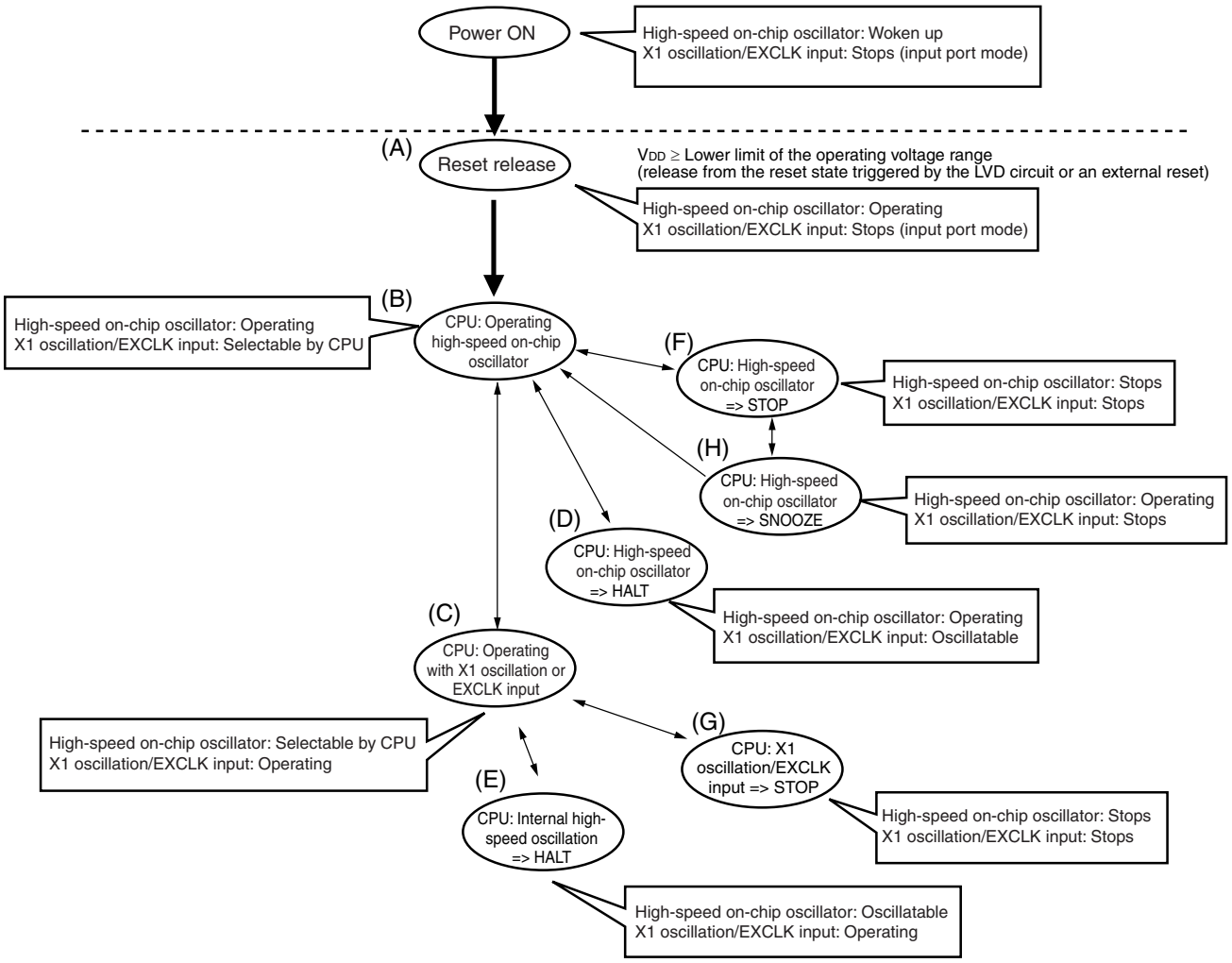
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1026adsp-x0

5.6.3 CPU clock status transition diagram

Figure 5-14 shows the CPU clock status transition diagram of this product.

Figure 5-14. CPU Clock Status Transition Diagram



6.1 Functions of Timer Array Unit

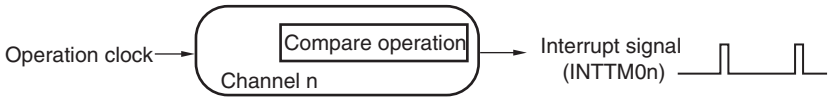
Timer array unit has the following functions.

6.1.1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

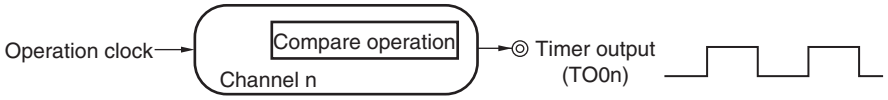
(1) Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTM0n) at fixed intervals.



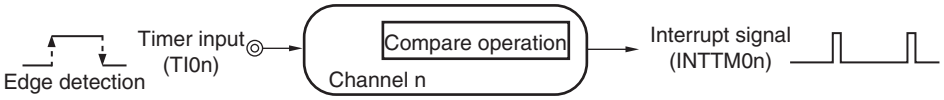
(2) Square wave output

A toggle operation is performed each time INTTM0n interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TO0n).



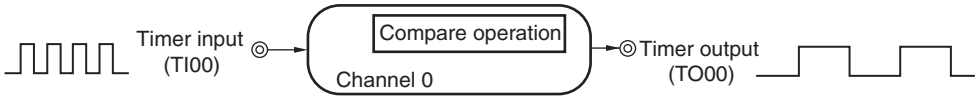
(3) External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TI0n) has reached a specific value.



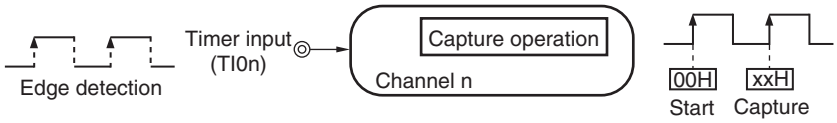
(4) Divider [Note]

A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).



(5) Input pulse interval measurement

Counting is started by the valid edge of a pulse signal input to a timer input pin (TI0n). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.



Note Only channel 0 of the 30-pin products.

Figure 6-8. Format of Timer Clock Select register 0 (TPS0)

Address: F01B6H, F01B7H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0	0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000

PRS 0k3	PRS 0k2	PRS 0k1	PRS 0k0	Selection of operation clock (CK0k)[Note](k = 0, 1)						
					f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	0	0	f_{CLK}	2 MHz	4 MHz	8 MHz	16 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	8 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	4 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1 MHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	500 kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	250 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	125 kHz	156 kHz	188 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	62.5 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	31.3 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	15.6 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	7.81 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	997 Hz	1.95 kHz	3.91 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	1.95 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	977 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	122 Hz	244 Hz	488 Hz	610 Hz	732 Hz

PRS 021	PRS 020	Selection of operation clock (CK02)[Note]						
			f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	8 MHz	10 MHz	12 MHz
0	1	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	4 MHz	5 MHz	6 MHz
1	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1 MHz	1.25 MHz	1.5 MHz
1	1	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	250 kHz	313 kHz	375 kHz

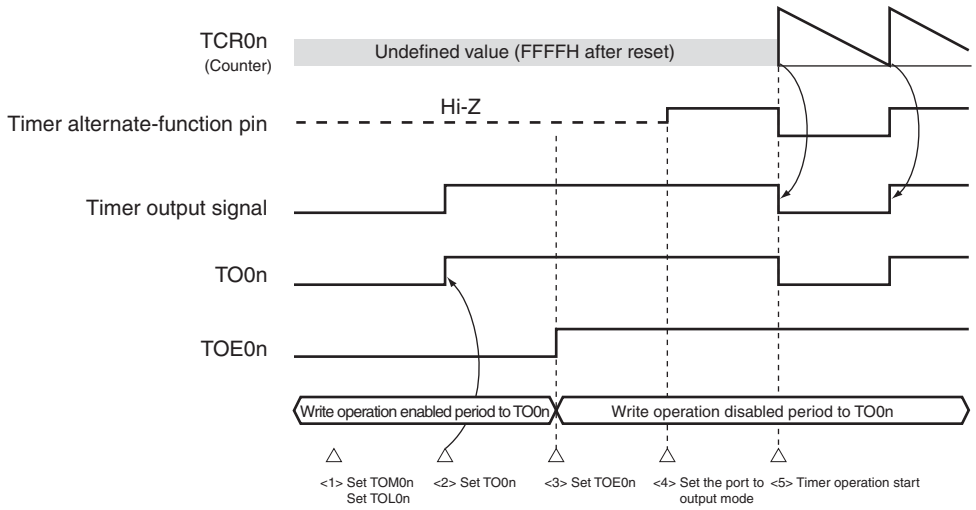
PRS 031	PRS 030	Selection of operation clock (CK03)[Note]						
			f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	62.5 kHz	78.1 kHz	93.8 kHz
0	1	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	15.6 kHz	19.5 kHz	23.4 kHz
1	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	3.91 kHz	4.88 kHz	5.86 kHz
1	1	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	977 Hz	1.22 kHz	1.46 kHz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop timer array unit (TT0 = 00FFH).

6.6.2 TO0n Pin Output Setting

The following figure shows the procedure and status transition of the TO0n output pin from initial setting to timer operation start.

Figure 6-28. Status Transition from Timer Output Setting to Operation Start



<1> The operation mode of timer output is set.

- TOM0n bit (0: Master channel output mode, 1: Slave channel output mode)
- TOL0n bit (0: Positive logic output, 1: Negative logic output)

<2> The timer output signal is set to the initial status by setting timer output register 0 (TO0).
<3> The timer output operation is enabled by writing 1 to the TOE0n bit (writing to the TO0 register is disabled).
<4> The port is set to digital I/O by port mode control register (PMCxx) (see **6.3.14 Registers controlling port functions of pins to be used for timer I/O**).
<5> The port I/O setting is set to output (see **6.3.14 Registers controlling port functions of pins to be used for timer I/O**).
<6> The timer operation is enabled (TS0n = 1).

Remark n: Channel number (n = 0 to 7)

Figure 6-44. Example of Set Contents of Registers in External Event Counter Mode (2/2)

(d) Timer output level register 0 (TOL0)

	Bit n	
TOL0	TOL0n 0	0: Cleared to 0 when master channel output mode (TOM0n = 0).

(e) Timer output mode register 0 (TOM0)

	Bit n	
TOM0	TOM0n 0	0: Sets master channel output mode.

Remark n: Channel number (n = 0 to 7)

7.4 12-bit Interval Timer Operation

7.4.1 12-bit interval timer operation timing

The count value specified for the ITCMP11 to ITCMP0 bits is used as an interval to operate an 12-bit interval timer that repeatedly generates interrupt requests (INTIT).

When the RINTE bit is set to 1, the 12-bit counter starts counting.

When the 12-bit counter value matches the value specified for the ITCMP11 to ITCMP0 bits, the 12-bit counter value is cleared to 0, counting continues, and an interrupt request signal (INTIT) is generated at the same time.

The basic operation of the 12-bit interval timer is shown in Figure 7-5.

Figure 7-5. 12-bit Interval Timer Operation Timing
(ITCMP11 to ITCMP0 = 0FFH, count clock: f_{IL} = 15 kHz)

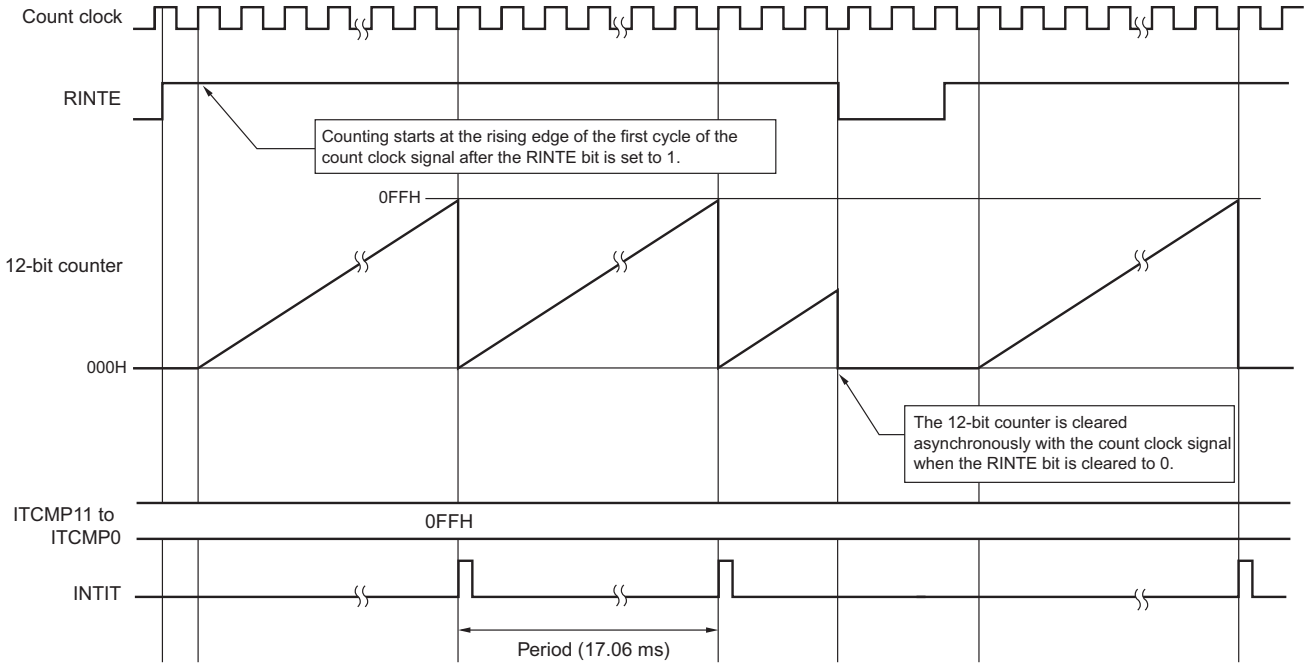
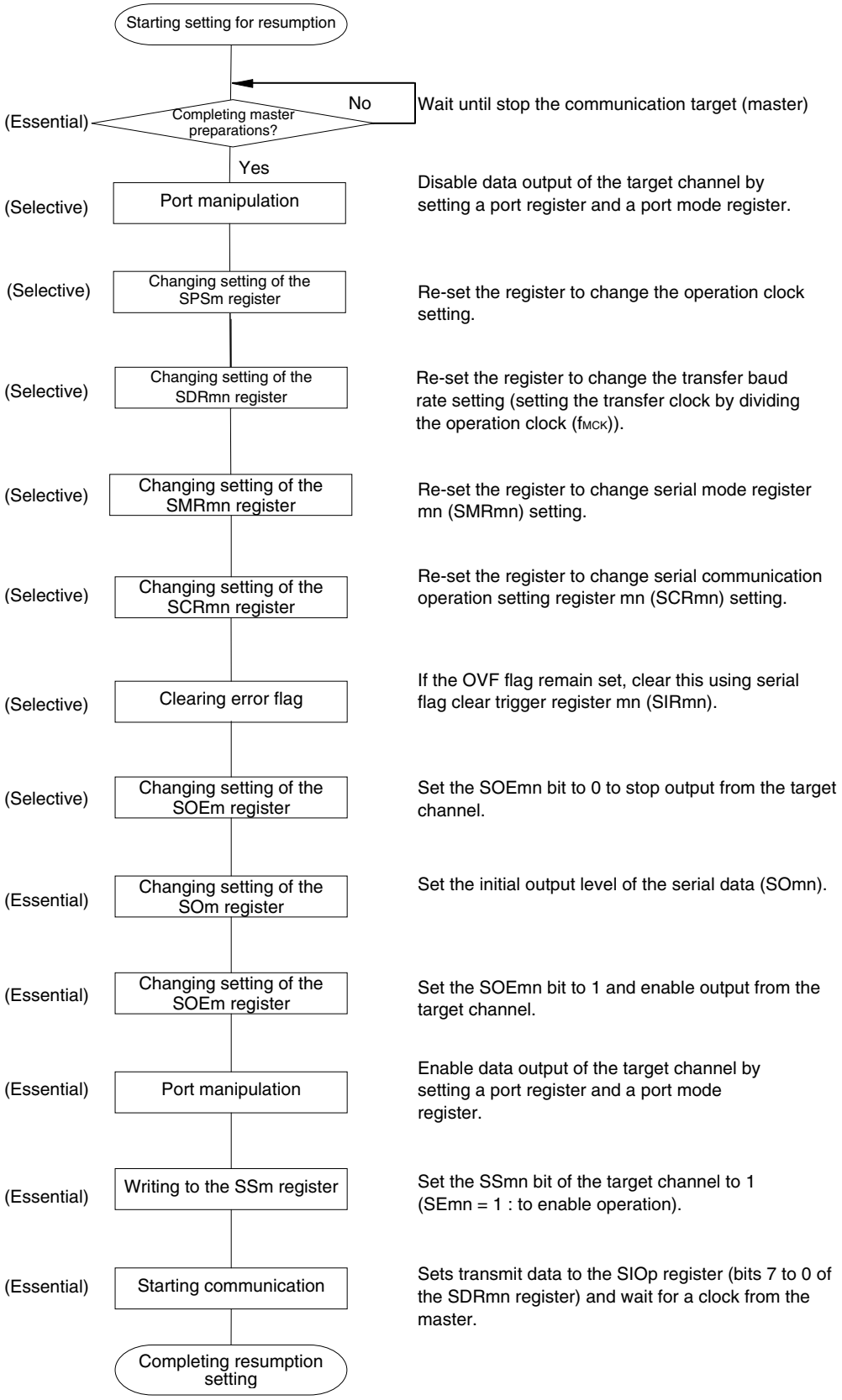
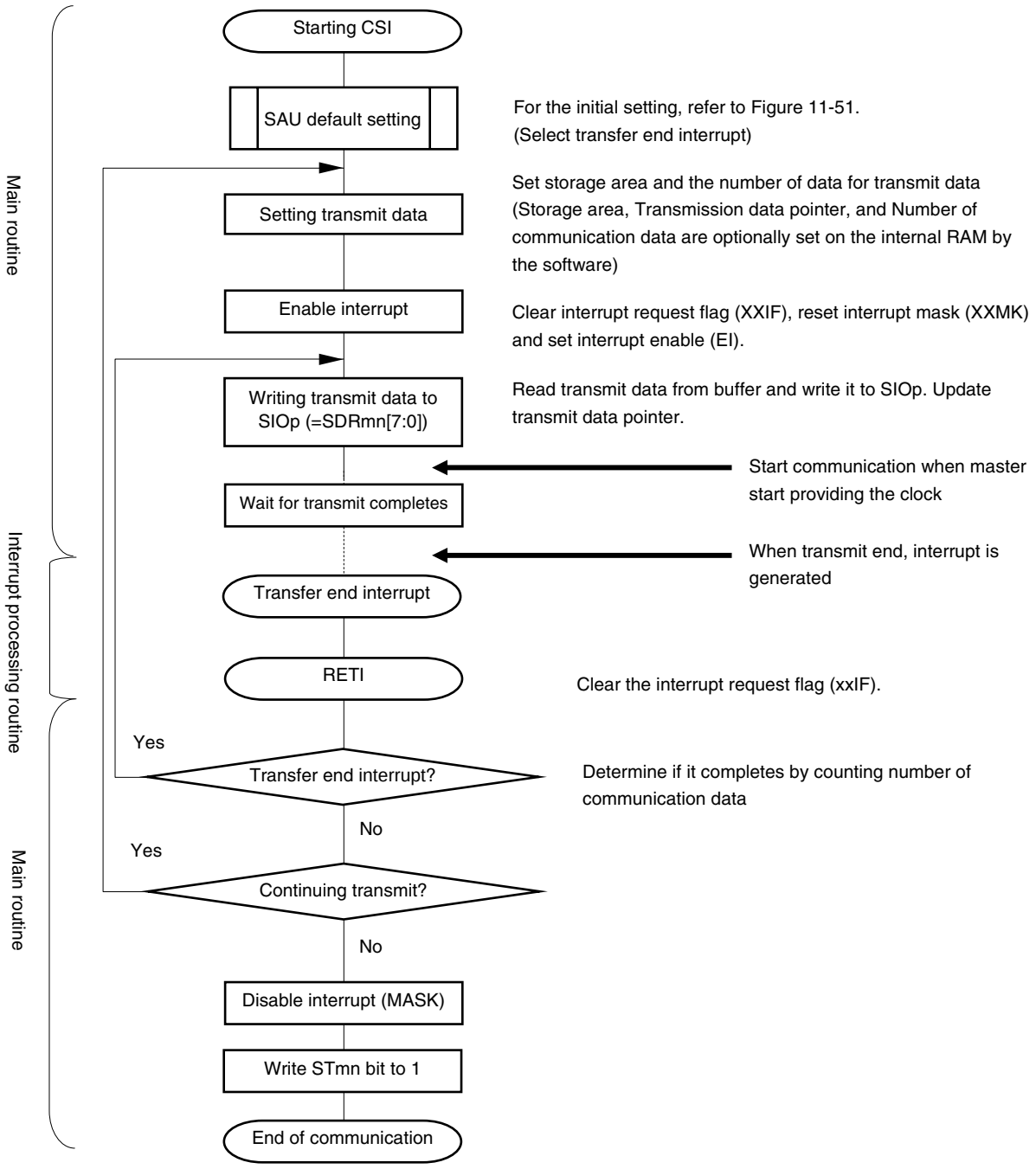


Figure 11-52. Procedure for Resuming Slave Transmission



Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

Figure 11-54. Flowchart of Slave Transmission (in Single-Transmission Mode)



(3) Permissible baud rate range for reception

The permissible baud rate range for reception during UART (UART0 to UART2) communication can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

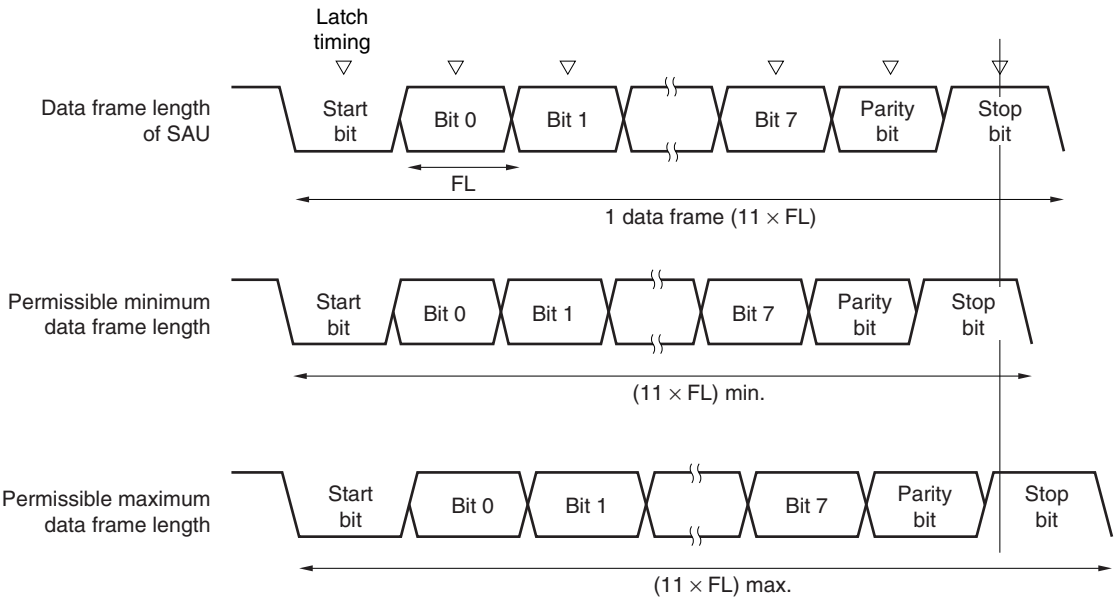
$$\text{(Maximum receivable baud rate)} = \frac{2 \times k \times Nfr}{2 \times k \times Nfr - k + 2} \times Brate$$

$$\text{(Minimum receivable baud rate)} = \frac{2 \times k \times (Nfr - 1)}{2 \times k \times Nfr - k - 2} \times Brate$$

Brate: Calculated baud rate value at the reception side (See **11.6.4 (1) Baud rate calculation expression**.)
k: SDRmn[15:9] + 1
Nfr: 1 data frame length [bits]
= (Start bit) + (Data length) + (Parity bit) + (Stop bit)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

Figure 11-95. Permissible Baud Rate Range for Reception (1 Data Frame Length = 11 Bits)



As shown in Figure 11-95 the timing of latching receive data is determined by the division ratio set by bits 15 to 9 of serial data register mn (SDRmn) after the start bit is detected. If the last data (stop bit) is received before this latch timing, the data can be correctly received.

Figure 15-7. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (30-pin product) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	SREPR00 TMPR001H	SRPR00	STPR00 CSIPR000 IICPR000Note	DMAPR01Note	DMAPR00Note	SREPR02Note	SRPR02Note	STPR02Note CSIPR020Note IICPR020Note

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	SREPR10 TMPR101H	SRPR10	STPR10 CSPR100 IICPR100Note	DMAPR11Note	DMAPR10Note	SREPR12Note	SRPR12Note	STPR12Note CSIPR120Note IICPR120Note

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	IICAPR00	SREPR01Note TMPR003H	SRPR01Note CSIPR011Note IICPR011Note	STPR01Note

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	IICAPR10	SREPR11Note TMPR103H	SRPR11Note CSIPR111Note IICPR111Note	STPR11Note

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	3	<2>	1	<0>
PR01H	TMPR004	1	1	1	1	TMKAPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	6	5	4	3	<2>	1	<0>
PR11H	TMPR104	1	1	1	1	TMKAPR1	1	ADPR1

Note Provided in the R5F102 products only.

16.4.2 When using the key interrupt flag (KRMD = 1)

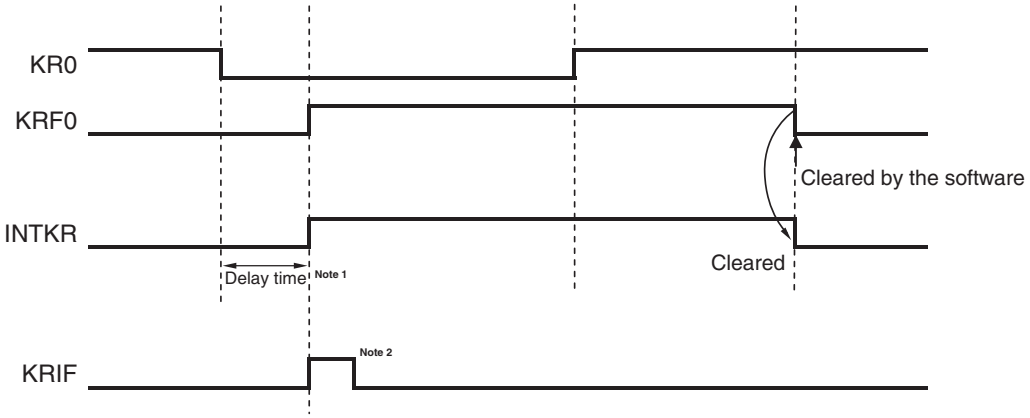
A key interrupt (INTKR) is generated when the valid edge specified by the setting of the KREG bit is input to a key interrupt pin (KR0 to KR5). The channels to which the valid edge was input can be identified by reading the key return flag register (KRF) after the key interrupt (INTKR) is generated.

If the KRMD bit is set to 1, the INTKR signal is cleared by clearing the corresponding bit in the KRF register.

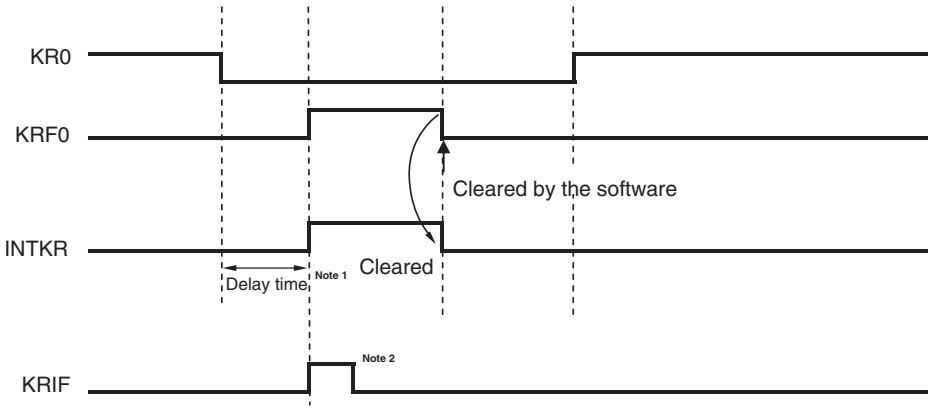
As shown in Figure 16-8, only one interrupt is generated each time a falling edge is input to one channel (when KREG = 0), regardless of whether the KRFn bit is cleared before or after a rising edge is input.

Figure 16-8. Basic Operation of the INTKR Signal When the Key Interrupt Flag Is Used (When KRMD = 1 and KREG = 0)

(a) KRF0 is cleared after a rising edge is input to the KR0 pin



(b) KRF0 is cleared before a rising edge is input to the KR0 pin



Notes 1. The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **28.4 AC Characteristics** or **29.4 AC Characteristics**).

2. Cleared by acknowledgment of vectored interrupt request or bit cleared by software.

20.3.1 Voltage detection register (LVIM)

This register is used to specify whether to enable or disable rewriting the voltage detection level register (LVIS), as well as to check the LVD output mask status.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 20-2. Format of Voltage Detection Register (LVIM)

Address: FFFA9H After reset: Note 1 R/W Note 2

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVISEN Note 3	0	0	0	0	0	LVIOMSK	LVIF

LVISEN Note 3	Specification of whether to enable or disable rewriting the voltage detection level register (LVIS)
0	Disabling of rewriting the LVIS register (LVIOMSK = 0 (Mask of LVD output is invalid))
1	Enabling of rewriting the LVIS register (LVIOMSK = 1 (Mask of LVD output is valid))

LVIOMSK	Mask status flag of LVD output
0	Mask of LVD output is invalid
1	Mask of LVD output is valid Note 4

LVIF	Voltage detection flag
0	Supply voltage (V_{DD}) ≥ detection voltage (V_{LVD}), or when LVD is off
1	Supply voltage (V_{DD}) < detection voltage (V_{LVD})

Notes 1. The reset value changes depending on the reset source.
If the LVIS register is reset by LVD, it is not reset but holds the current value. The value of this LVISEN is reset to “0” if a reset other than by LVD is effected.

2. Bits 0 and 1 are read-only.

3. LVISEN and LVIOMSK can only be set in the interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0). Do not change the initial value in other modes.

4. LVIOMSK bit is only automatically set to “1” when the interrupt & reset mode is selected (option byte LVIMDS1, LVIMDS0 = 1, 0) and reset or interrupt by LVD is masked.
- Period during LVISEN = 1
- Waiting period from the time when LVD interrupt is generated until LVD detection voltage becomes stable
- Waiting period from the time when the value of LVILV bit changes until LVD detection voltage becomes stable

20.4.2 When used as interrupt mode

Specify the operation mode (the interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)) and the detection voltage (V_{LVD}) by using the option byte 000C1H.

The operation is started in the following initial setting state when the interrupt mode is set.

- Bit 7 (LVISEN) of the voltage detection register (LVIM) is set to 0 (disable rewriting of voltage detection level register (LVIS))
- The initial value of the voltage detection level select register (LVIS) is set to 01H.
  Bit 7 (LVIMD) is 0 (interrupt mode).
  Bit 0 (LVILV) is 1 (low-voltage detection level: V_{LVD}).

- Operation in LVD interrupt mode

<R> In the interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1), the state of an internal reset by LVD is retained immediately after a reset until the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}). The internal reset is released when the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}).
After the LVD internal reset is released, an interrupt request signal (INTLVI) by the LVD is generated when the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}).
When the voltage falls, this LSI should be placed in the STOP mode, or placed in the reset state by controlling the externally input reset signal, before the voltage falls below the operating voltage range defined in **28.4 or 29.4 AC Characteristics**. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Figure 20-6 shows the timing of the interrupt request signal generated in the LVD interrupt mode.

24.3 Connection of Pins on Board

To write the flash memory on-board by using the flash memory programmer, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

Remark For the flash memory programming mode, see **24.4.2 Flash memory programming mode**.

24.3.1 P40/TOOL0 pin

In the flash memory programming mode, pull up externally with a 1 kΩ resister, and connect it to the dedicated flash memory programmer.

When using it as a port pin, use it as described below.

When used as an input pin: Do not input a low level for t_{HD} period after the external reset release. However, when this pin is used via pull-down resistors, use the 500 kΩ or more resistors.

When used as an output pin: When this pin is used via pull-down resistors, use the 500 kΩ or more resistors.

Remarks 1. t_{HD}: How long to keep the TOOL0 pin at the low level from when the external reset ends for setting of the flash memory programming mode (see **28.10** or **29.10 Timing of Entry to Flash Memory Programming Modes**)

2. The SAU and IICA pins are not used for communication between the RL78 microcontroller and dedicated flash memory programmer, because single-line UART (TOOL0 pin) is used.

24.3.2 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer and external device are connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set. Do not input any signal other than the reset signal of the dedicated flash memory programmer and external device.

Figure 24-5. Signal Conflict ($\overline{\text{RESET}}$ Pin)

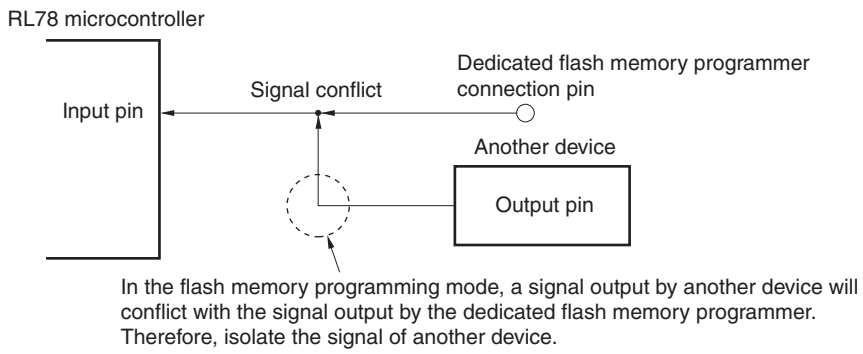
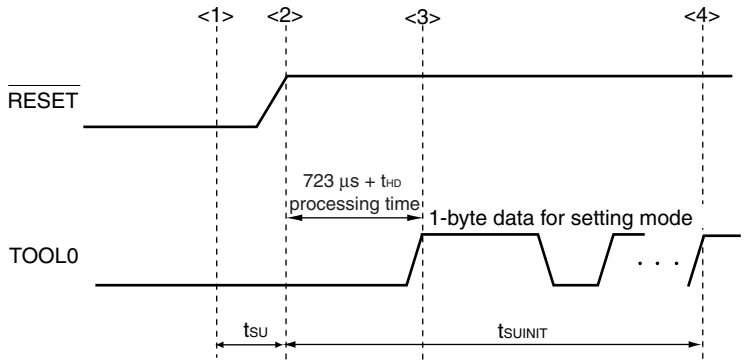


Figure 24-7. Setting of Flash Memory Programming Mode



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

For details, see **28.10** or **29.10 Timing of Entry to Flash Memory Programming Modes**.

There are two flash memory programming modes: wide voltage mode and full speed mode. The supply voltage value applied to the microcontroller during write operations and the setting information of the user option byte for setting of the flash memory programming mode determine which mode is selected.

When a dedicated flash memory programmer is used for serial programming, setting the voltage on GUI selects the mode automatically.

Table 24-5. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified

Power Supply Voltage (V_{DD})	User Option Byte Setting for Switching to Flash Memory Programming Mode		Flash Programming Mode
	Flash Operation Mode	Operating Frequency	
2.7 V ≤ V_{DD} ≤ 5.5 V	Blank state		Full speed mode
	HS (high speed main) mode	1 MHz to 24 MHz	Full speed mode
	LS (low speed main) mode	1 MHz to 8 MHz	Wide voltage mode
2.4 V ≤ V_{DD} < 2.7 V	Blank state		Full speed mode
	HS (high speed main) mode	1 MHz to 16 MHz	Full speed mode
	LS (low speed main) mode	1 MHz to 8 MHz	Wide voltage mode
1.8 V ≤ V_{DD} < 2.4 V	Blank state		Wide voltage mode
	LS (low speed main) mode	1 MHz to 8 MHz	Wide voltage mode

Remarks 1. Using both the wide voltage mode and full speed mode imposes no restrictions on writing, erasing, or verification.
2. For details about communication commands, see **24.4.4 Communication commands**.

24.4.3 Selecting communication mode

Communication modes of the RL78 microcontroller are as follows.

Table 24-6. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used
	Port	Speed [Note 2]	Frequency	Multiply Rate	
1-line UART (when flash memory programmer is used, or when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	–	–	TOOL0
Dedicated UART (when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	–	–	TOOLTxD, TOOLRxD

Notes 1. Selection items for standard settings on GUI of the flash memory programmer.

2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

24.4.4 Communication commands

The RL78 microcontroller executes serial programming through the commands listed in **Table 24-7.**

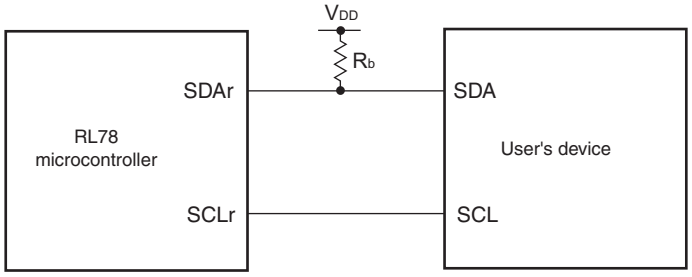
The signals sent from the dedicated flash memory programmer or external device to the RL78 microcontroller are called commands, and programming functions corresponding to the commands are executed. For details, refer to the **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

Table 24-7. Flash Memory Control Commands

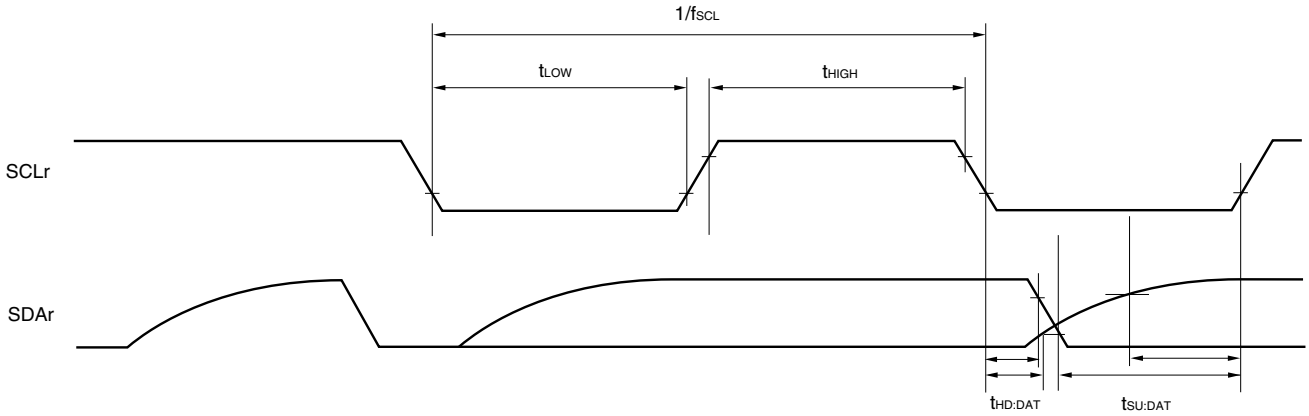
Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory. [Note]
Getting information	Silicon Signature	Gets the RL78 microcontroller information (such as the part number and flash memory configuration, firmware version).
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
	Security Get	Gets security information.
	Security Release	Releases the write prohibition setting.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

Note Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b [Ω]:Communication line (SDAr) pull-up resistance
C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

4. Simplified I²C mode is supported only by the R5F102 products.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (4/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P23	I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V
Input leakage current, high	I_{LIH1}	Other than P121, P122	V_I = V_{DD}			1	μA
	I_{LIH2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{DD} Input port or external clock input			1	μA
			V_I = V_{DD} When resonator connected			10	μA
Input leakage current, low	I_{LIL1}	Other than P121, P122	V_I = V_{SS}			–1	μA
	I_{LIL2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{SS} Input port or external clock input			–1	μA
			V_I = V_{SS} When resonator connected			–10	μA
On-chip pull-up resistance	R_U	20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	V_I = V_{SS}, input port	10	20	100	kΩ

Note 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) 20-, 24-pin products

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (High-speed main) mode[Note 6]	f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		440	2230	μA
					V_{DD} = 3.0 V		440	2230	
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 5.0 V		400	1650	μA
					V_{DD} = 3.0 V		400	1650	
				f_{MX} = 20 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		190	1010	μA
					Resonator connection		260	1090	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		190	1010	μA
					Resonator connection		260	1090	
	I_{DD3}[Note 5]	STOP mode	T_A = –40°C				0.19	0.50	μA
			T_A = +25°C				0.24	0.50	
			T_A = +50°C				0.32	0.80	
			T_A = +70°C				0.48	1.20	
			T_A = +85°C				0.74	2.20	
			T_A = +105°C				1.50	10.20	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz

V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Except temperature condition of the TYP. value is T_A = 25°C, other than STOP mode

(4/17)

Edition	Description	Chapter
2.00	Modification of Caution in 11.3.14 Serial standby control register 0 (SSC0)	CHAPTER 11 SERIAL ARRAY UNIT
	Modification of Figure 11-20	
	Addition of Figure 11-21	
	Modification of description in 11.3.15 Noise filter enable register 0 (NFEN0)	
	Modification of Caution in Figure 11-22	
	Modification of description in 11.3.16 Registers controlling port functions of serial input/output pins	
	Modification of description of 11.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI11, CSI20) Communication and Note	
	Modification of description in 11.5.1 Master transmission and addition of Remark	
	Modification of Figures 11-28 to 11-32	
	Modification of description in 11.5.2 Master reception and addition of Remark	
	Modification of Figures 11-35 to 11-37, 11-39, and 11-40	
	Modification of description in 11.5.3 Master transmission/reception and addition of Remark	
	Modification of Figures 11-43, 11-45, 11-47, and 11-48	
	Modification of description in 11.5.4 Slave transmission, Notes 1 and 2, and Remark 2	
	Modification of Figures 11-49 and 11-51 to 11-56	
	Modification of description in 11.5.5 Slave reception and Notes 1 and 2	
	Modification of Figures 11-57 to 11-59, 11-61, and 11-62	
	Modification of description in 11.5.6 Slave transmission/reception and Notes 1 and 2	
	Modification of Figures 11-65 and 11-67 to 11-70	
	Modification of description in 11.5.7 SNOOZE mode function	
	Modification of Figures 11-71 to 11-74	
	Modification of description in 11.6 Operation of UART (UART0 to UART2) Communication and addition of Note 1	
	Modification of description in 11.6.1 UART transmission and addition of Notes 1 and 2	
	Modification of Figures 11-77 to 11-83	
	Modification of description in 11.6.2 UART reception and addition of Notes 1 and 2	
	Modification of Figure 11-86, 11-88, and 11-89	
	Modification of description in 11.6.3 SNOOZE mode function and addition of Cautions 2 to 4	
	Modification of Table 11-3	
	Modification of description in 11. 6. 3 (1) and Figure 11-90	
	Modification of description in 11. 6. 3 (2) and Figure 11-91	
	Modification of Figure 11-92	
	Modification of description in 11. 6. 3 (3) and Figure 11-93	
	Modification of Figure 11-94	
	Modification of description in 11.7 Operation of Simplified I2C (IIC00, IIC01, IIC11, IIC20) Communication	
	Modification of description in 11.7.1 Address field transmission and Notes 1 and 2	
	Modification of description in 11.7.2 Data transmission and Notes 1 and 2	
	Modification of description in 11.7.3 Data reception and Notes 1 and 2	
	Modification of Figure 11-107	
	Modification of Figure 11-109	
	Modification of Figure 11-110	
	Modification of Figure 12-1	CHAPTER 12 SERIAL INTERFACE IICA
	Modification of Figure 12-5	
	Modification of Figure 12-6 (3/4) and (4/4)	
	Modification of Figure 12-9 (2/2)	
	Modification of description in 12.3.6 IICA low-level width setting register 0 (IICWL0)	
	Modification of description in 12.3.7 IICA high-level width setting register 0 (IICWH0)	
	Modification of description in 12.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers	