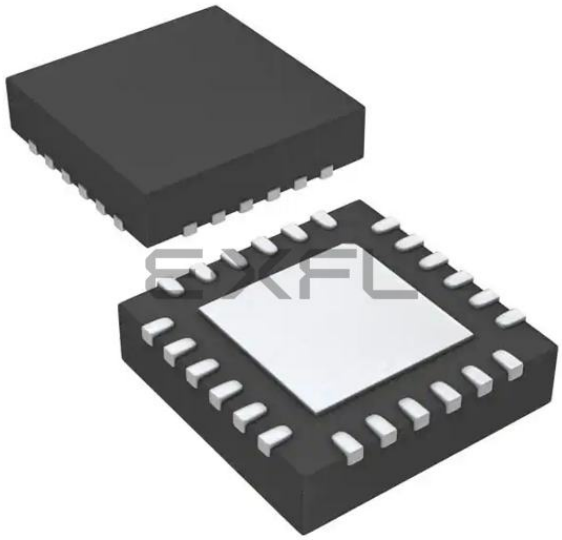

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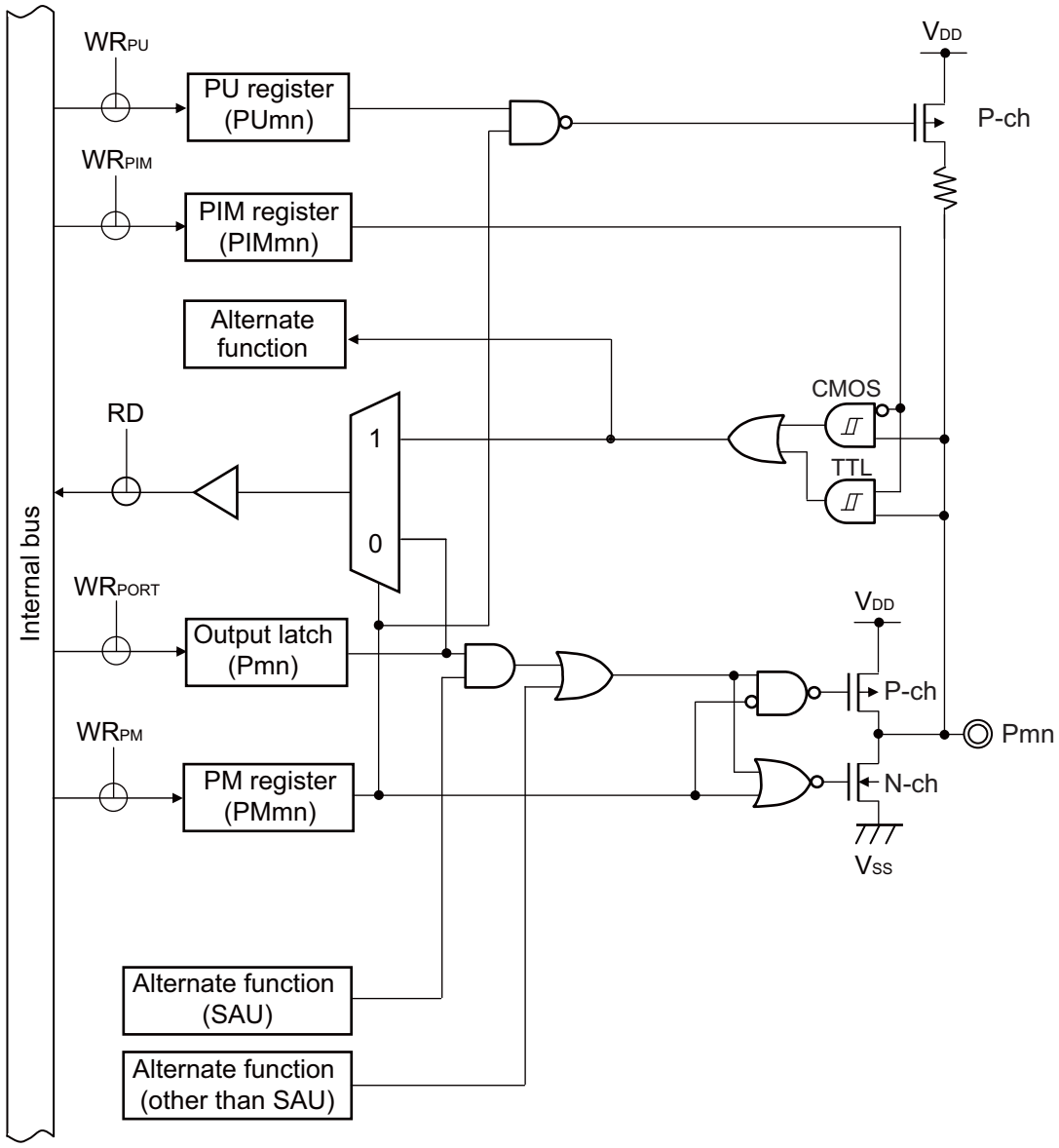
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10278dna-u0

Figure 2-10. Pin Block Diagram for Pin Type 8-1-1



Remarks 1. For alternate functions, see **2.1 Port Functions**.

2. SAU: Serial array unit

<R> **Caution** Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

5.4.2 High-speed on-chip oscillator

The high-speed on-chip oscillator is incorporated in the RL78/G12. The frequency can be selected from among 24, 16, 12, 8, 6, 4, 3, 2, or 1 MHz by using the option byte (000C2H). Oscillation can be controlled by bit 0 (HIOSTOP) of the clock operation status control register (CSC). The high-speed on-chip oscillator automatically starts oscillating after reset release.

5.4.3 Low-speed on-chip oscillator

The low-speed on-chip oscillator is incorporated in the RL78/G12.

The low-speed on-chip oscillator clock is used only as the watchdog timer, and 12-bit interval timer clock. The low-speed on-chip oscillator clock cannot be used as the CPU clock.

This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the operation speed mode control register (OSMC), or both are set to 1.

Unless the watchdog timer is stopped and WUTMMCK0 is a value other than zero, oscillation of the low-speed on-chip oscillator continues. Note that only when the watchdog timer is operating and the WUTMMCK0 bit is 0, oscillation of the low-speed on-chip oscillator will stop while the WDSTBYON bit is 0 and operation is in the HALT, STOP, or SNOOZE mode. While the watchdog timer operates, the low-speed on-chip oscillator clock does not stop even if the program freezes.

5.5 Clock Generator Operation

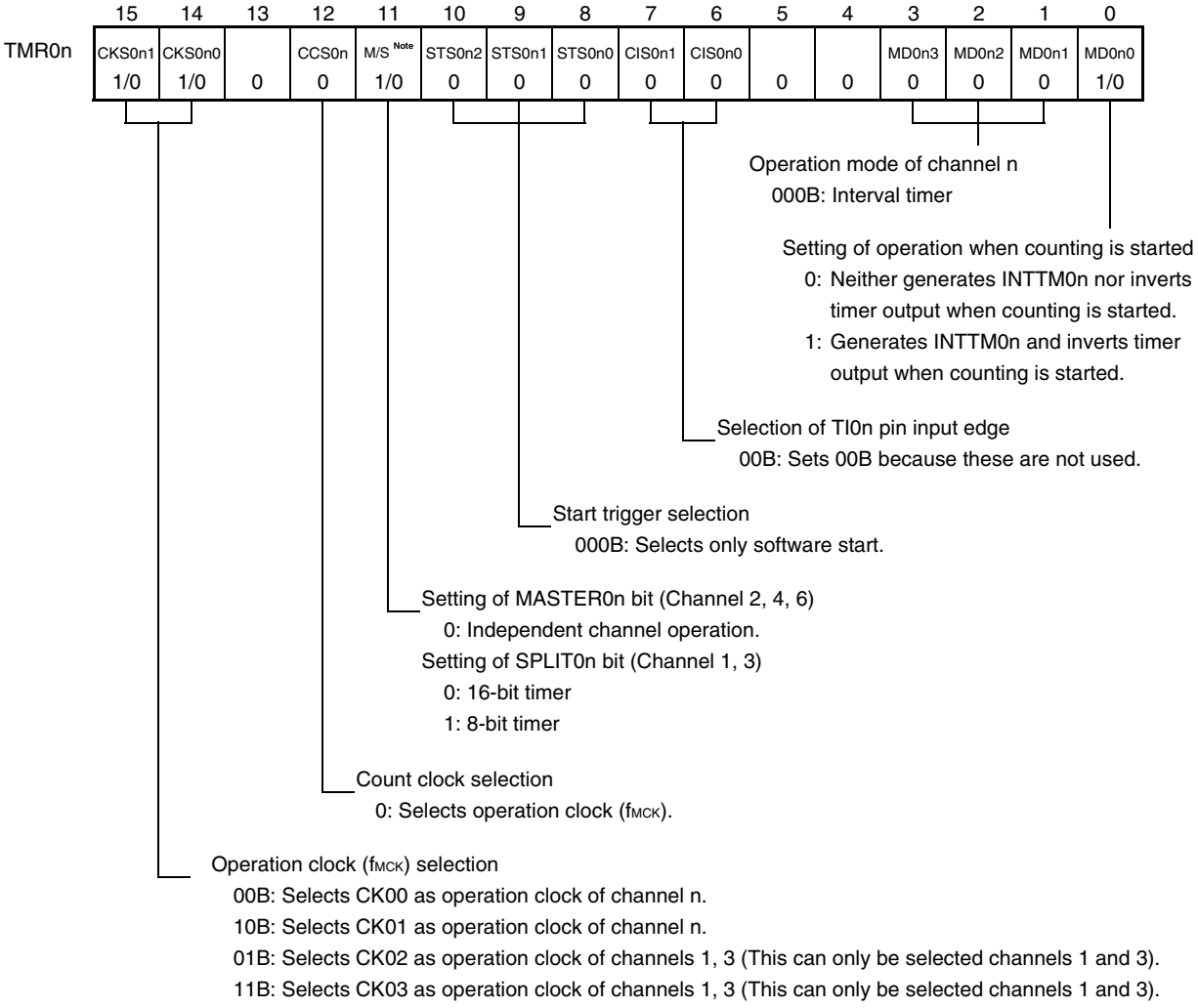
The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 5-1**).

- Main system clock f_{MAIN}
  - High-speed system clock f_{MX}
    X1 clock f_X
    External main system clock f_{EX}
  - High-speed on-chip oscillator clock f_{IH}
- Low-speed on-chip oscillator clock f_{IL}
- CPU/peripheral hardware clock f_{CLK}

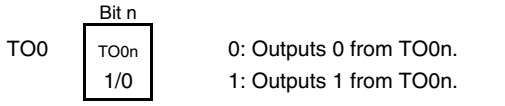
The CPU starts operation when the high-speed on-chip oscillator starts outputting after a reset release in the RL78/G12. When the power supply voltage is turned on, the clock generator operation is shown in Figure 5-13.

Figure 6-40. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (1/2)

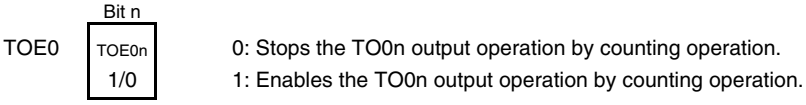
(a) Timer mode register 0n (TMR0n)



(b) Timer output register 0 (TO0)



(c) Timer output enable register 0 (TOE0)



Note TMR02, TMR04, TMR06: MASTER0n bit
TMR01, TMR03: SPLIT0n bit
TMR00, TMR05, TMR07: 0 fixed

Remark n: Channel number (n = 0 to 7)

11.2.1 Shift register

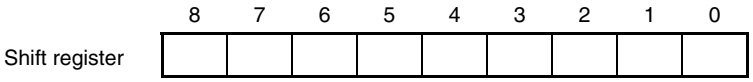
This is an 8-bit register that converts parallel data into serial data or vice versa.

In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used[Note 1].

During reception, it converts data input to the serial pin into parallel data. When data is transmitted, the value set to this register is output as serial data from the serial output pin.

The shift register cannot be directly manipulated by program.

To read or write to the shift register, use the lower 8/9 bits of serial data register mn (SDRmn).



11.2.2 Lower 8/9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits)[Note 1] or bits 7 to 0 (lower 8 bits) function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

When data is received, parallel data converted by the shift register is stored in the lower 8/9 bits. When data is to be transmitted, set transmit data to be transferred to the shift register to the lower 8/9 bits.

The length of data stored in the lower 8/9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLS0m1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDR00 and SDR01 registers)[Note 1]

The SDRmn register can be read or written in 16-bit units.

The lower 8/9 bits of the SDRmn register can be read or written in 8-bit units as the following SFR, depending on the communication mode[Note 2].

- During CSIp communication: SIOp (CSIp data register)
- During UARTq reception: RXDq (UARTq receive data register)
- During UARTq transmission: TXDq (UARTq transmit data register)
- During IICr communication: SIOr (IICr data register)

Reset signal generation clears the SDRmn register to 0000H.

Notes 1. Only UART0 can be specified for the 9-bit data length.

<R> **2.** When operation is stopped (SEmn = 0), do not rewrite SDRmn[7:0] by an 8-bit memory manipulation instruction (SDRmn[15:9] are all cleared to 0).

Remarks 1. After data is received, "0" is applied to some bits of bits 0 to 8 to make up the specified data length.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 11, 20), q: UART number (q = 0 to 2), r: IIC number (r = 00, 01, 11, 20)

11.5.3 Master transmission/reception

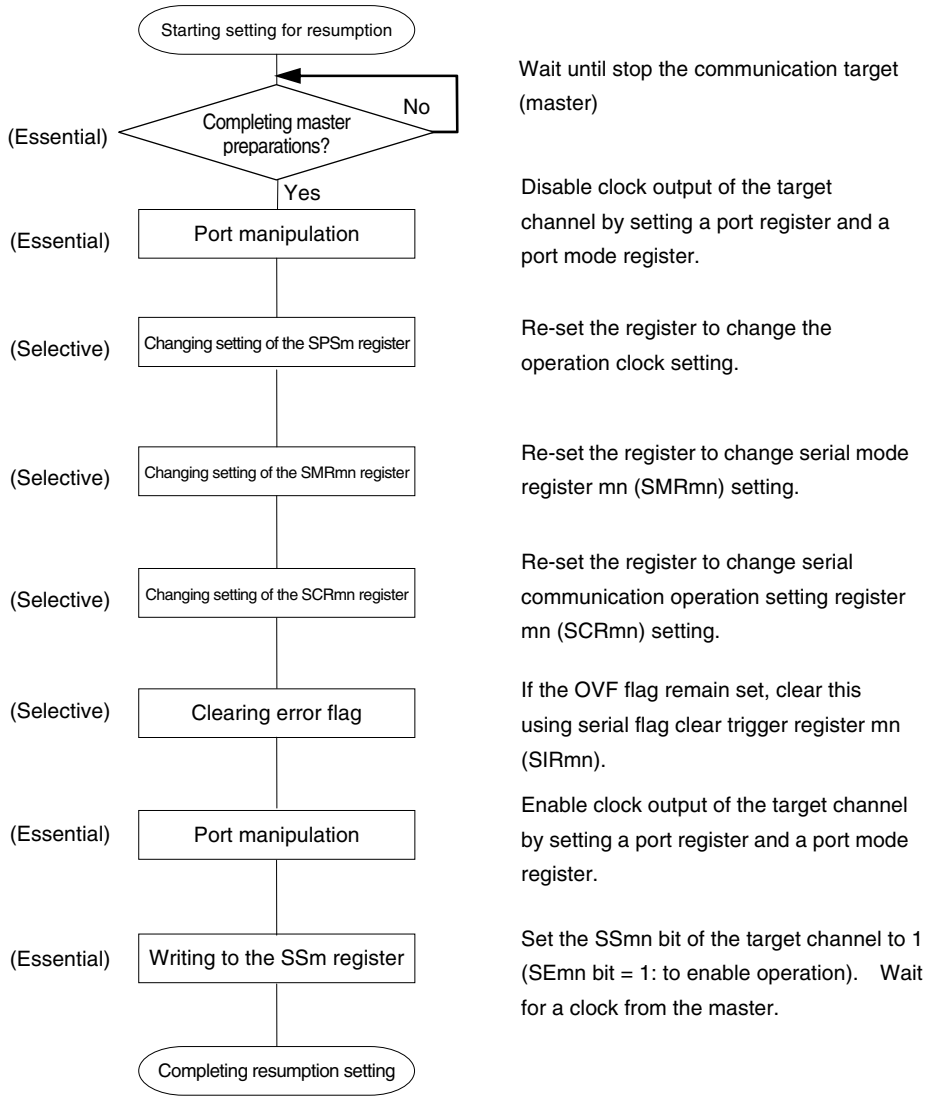
Master transmission/reception is that the RL78 microcontroller outputs a transfer clock and transmits/receives data to/from other device.

3-Wire Serial I/O	CSI00	CSI01	CSI11	CSI20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 3 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SI00, SO00	SCK01, SI01, SO01	SCK11, SI11, SO11	SCK20, SI20, SO20
Interrupt	INTCSI00	INTCSI01	INTCSI11	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.			
Error detection flag	Overrun error detection flag (OVFmn) only			
Transfer data length	7 or 8 bits			
Transfer rate[Note]	Max. $f_{CLK}/2$ [Hz] (CSI00 only), $f_{CLK}/4$ [Hz] Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [Hz] f_{CLK}: System clock frequency			
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts at the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.			
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-inversion • CKPmn = 1: Inverted			
Data direction	MSB or LSB first			

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 28 ELECTRICAL SPECIFICATIONS (A, D: T_A = -40 to +85°C)** or **CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: T_A = -40 to +105°C)**).

Remarks m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13

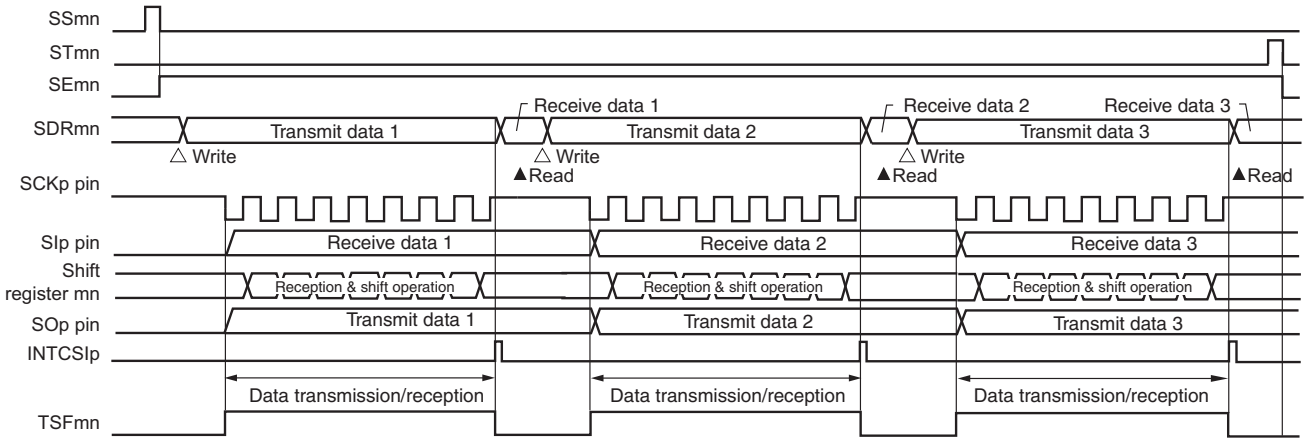
Figure 11-60. Procedure for Resuming Slave Reception



Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

(3) Processing flow (in single-transmission/reception mode)

Figure 11-67. Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 11, 20), mn = 00, 01, 03, 10

11.5.7 SNOOZE mode function

The SNOOZE mode makes the CSI perform reception operations upon SCK00 pin input detection while in the STOP mode. Normally the CSI stops communication in the STOP mode. However, using the SNOOZE mode enables the CSI to perform reception operations without CPU operation upon detection of the SCK00 pin input. Only CSI00 can be set to the SNOOZE mode.

When using the CSI in SNOOZE mode, make the following setting before switching to the STOP mode (see **Figure 11-72 Flowchart of SNOOZE Mode Operation (once startup)** and **Figure 11-74 Flowchart of SNOOZE Mode Operation (continuous startup)**).

<R> • When using the SNOOZE mode function, set the SWC0 bit of serial standby control register 0 (SSC0) to 1 just before switching to the STOP mode. After the initial setting has been completed, set the SS00 bit of serial channel start register 0 (SS0) to 1.

• The CPU shifts to the SNOOZE mode on detecting the valid edge of the SCKp signal following a transition to the STOP mode. A CSIp starts reception on detecting input of the serial clock on the SCKp pin.

After a transition to the STOP mode, the CSI starts reception operations upon detection of an edge of the SCK00 pin.

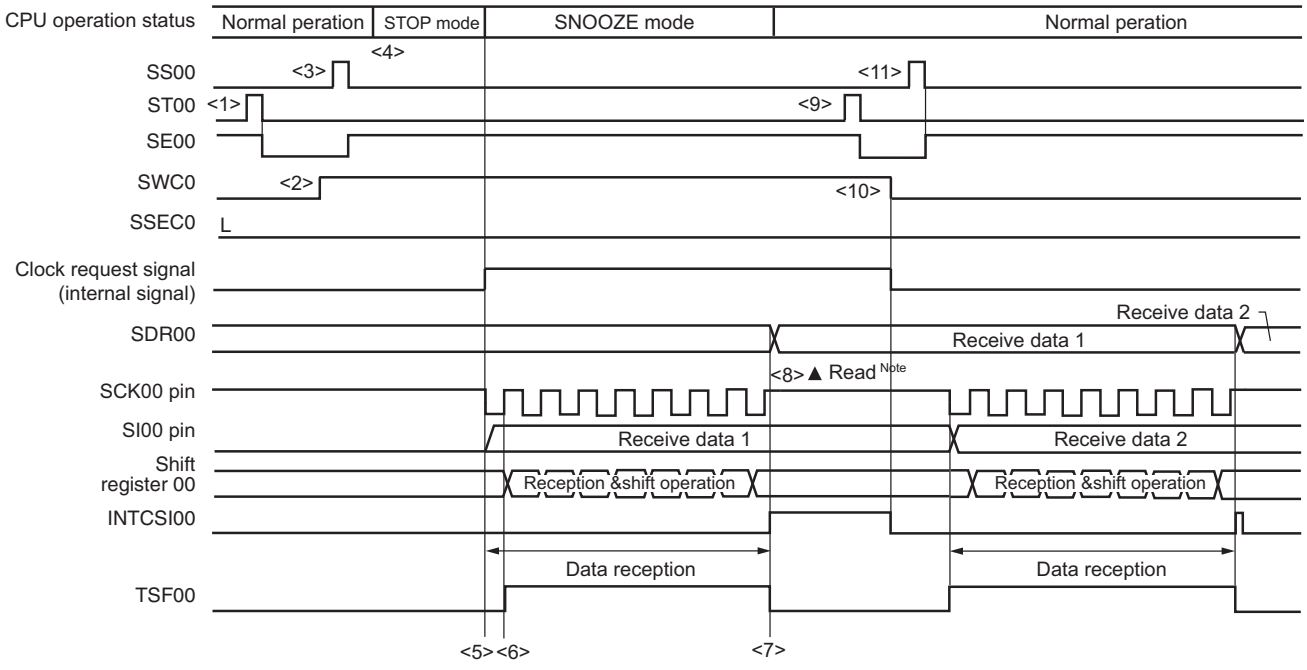
Cautions 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for f_{CLK}.

2. The maximum transfer rate when using CSI00 in the SNOOZE mode is 1 Mbps.

(1) SNOOZE mode operation (once startup)

Figure 11-71. Timing Chart of SNOOZE Mode Operation (once startup) (Type 1: DAP00 = 0, CKP00 = 0)

<R>



Note Only read received data while SWC0 = 1 and before the next valid edge of the SCK00 pin input is detected.

Cautions 1. Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the ST00 bit to 1 (clear the SE00 bit, and stop the operation).
And after completion the receive operation, also clearing SWC0 bit to 0 (SNOOZE mode release).

2. When SWC0 = 1, the BFF01 and OVF01 flags will not change.

Figure 11-76. Example of Contents of Registers for UART Transmission (UART0 to UART2) (2/2)

(e) Serial output register m (SOm) ... Sets only the bits of the target channel.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	1	CKOm1 ×	CKOm0 ×	0	0	0	0	SO03 Note 1 ×	SO02 Note 1 0/1 Note 2	SO01 ×	SOm0 0/1 Note 2

0: Serial data output value is "0"
1: Serial data output value is "1"

(f) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	SOE03 Note 1 ×	SOE02 Note 1 0/1	SOE01 ×	SOEm0 0/1

(g) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SS03 Note 1 ×	SS02 Note 1 0/1	SSm1 ×	SSm0 0/1

Notes 1. Provided only in 30-pin product serial array unit 0.

2. Before transmission is started, be sure to set to 1 when the SOL00 bit of the target channel is set to 0, and set to 0 when the SOL00 bit of the target channel is set to 1. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

2. ☐ : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

12.5.13 Wakeup function

The I^2C bus slave function is a function that generates an interrupt request signal (INTIICA0) when a local address and extension code have been received.

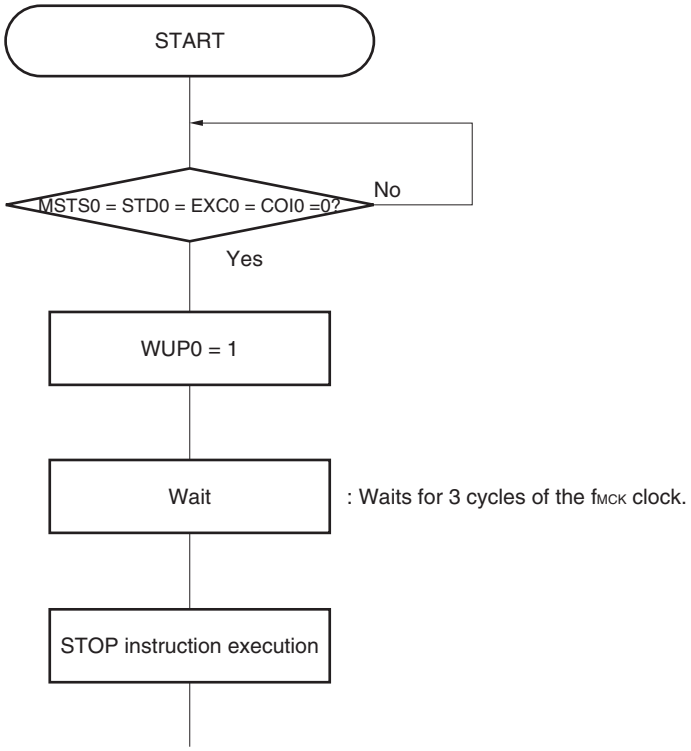
This function makes processing more efficient by preventing unnecessary INTIICA0 signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

To use the wakeup function in the STOP mode, set the WUP0 bit to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICA0) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUP0 bit after this interrupt has been generated.

Figure 12-22 shows the flow for setting WUP0 = 1 and Figure 12-23 shows the flow for setting WUP0 = 0 upon an address match.

Figure 12-22. Flow When Setting WUP0 = 1



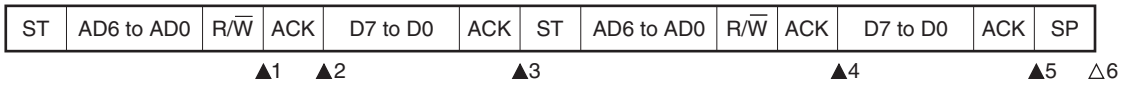
(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, matches SVA0)

▲1: IICS0 = 0010×010B
▲2: IICS0 = 0010×000B
▲3: IICS0 = 0001×110B
▲4: IICS0 = 0001×000B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches SVA0)



▲1: IICS0 = 0010×010B
▲2: IICS0 = 0010×110B
▲3: IICS0 = 0010××00B
▲4: IICS0 = 0001×110B
▲5: IICS0 = 0001××00B
△6: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

13.2.3 Multiplication/division data register C (MDCL, MDCH)

The MDCH and MDCL registers are used to store the accumulated result while in the multiply-accumulator mode or the remainder of the operation result while in the division mode. These registers are not used while in the multiplication mode.

The MDCH and MDCL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 13-4. Format of Multiplication/Division Data Register C (MDCH, MDCL)

Address: F00E0H, F00E1H, F00E2H, F00E3H After reset: 0000H, 0000H R/W

Symbol F00E3H F00E2H

MDCH	MDCH 15	MDCH 14	MDCH 13	MDCH 12	MDCH 11	MDCH 10	MDCH 9	MDCH 8	MDCH 7	MDCH 6	MDCH 5	MDCH 4	MDCH 3	MDCH 2	MDCH 1	MDCH 0

Symbol F00E1H F00E0H

MDCL	MDCL 15	MDCL 14	MDCL 13	MDCL 12	MDCL 11	MDCL 10	MDCL 9	MDCL 8	MDCL 7	MDCL 6	MDCL 5	MDCL 4	MDCL 3	MDCL 2	MDCL 1	MDCL 0

Cautions 1. The MDCH and MDCL registers values read during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H) will not be guaranteed.

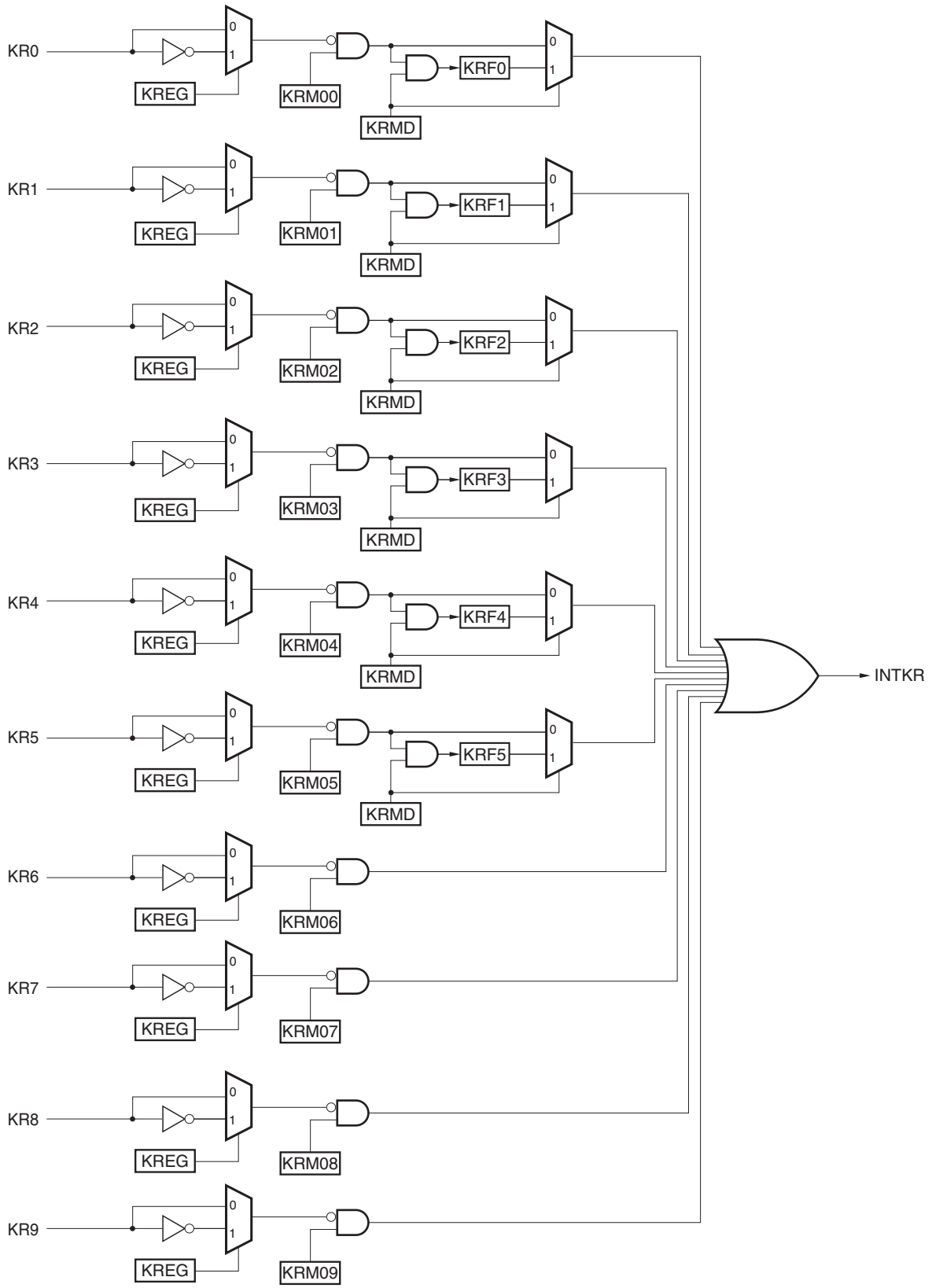
2. During multiply-accumulator processing, do not use software to rewrite the values of the MDCH and MDCL registers. If this is done, the operation result will be undefined.

3. The data is in the two's complement format in the multiply-accumulator mode (signed).

Table 13-4. Functions of MDCH and MDCL Registers During Operation Execution

Operation Mode	Setting	Operation Result
Multiplication mode (unsigned or signed)	–	–
Multiply-accumulator mode (unsigned)	MDCH: Initial accumulated value (unsigned) (higher 16 bits) MDCL: Initial accumulated value (unsigned) (lower 16 bits)	MDCH: accumulated value (unsigned) (higher 16 bits) MDCL: accumulated value (unsigned) (lower 16 bits)
Multiply-accumulator mode (signed)	MDCH: Initial accumulated value (signed) (higher 16 bits) MDCL: Initial accumulated value (signed) (lower 16 bits)	MDCH: accumulated value (signed) (higher 16 bits) MDCL: accumulated value (signed) (lower 16 bits)
Division mode (unsigned)	–	MDCH: Remainder (unsigned) (higher 16 bits) MDCL: Remainder (unsigned) (lower 16 bits)

Figure 16-1. Block Diagram of Key Interrupt



Remark KR0 to KR5: 20-pin products
KR0 to KR9: 24-pin products

Figure 20-4. LVD Operation Mode and Detection Voltage Settings for User Option Byte (000C1H) (2/2)

Address: 000C1H

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	PORTSELB	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt mode)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.88 V	1.84 V	0	0	1	1	1	0	1
1.98 V	1.94 V		0	1	1	0		
2.09 V	2.04 V		0	1	0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V		1	0	1	0		
2.71 V	2.65 V		1	0	0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V		1	1	1	0		
3.02 V	2.96 V		1	1	0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
—		Setting of values other than above is prohibited.						

- LVD off (use of external reset input via $\overline{\text{RESET}}$ pin)

Detection voltage		Option byte Setting Value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
–	–	1	×	×	×	×	×	1
—		Setting of values other than above is prohibited.						

Cautions 1. Set bit 4 to 1.

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 28.4 or 29.4 AC Characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H).

Remarks 1. ×: don't care

2. For details on the LVD circuit, see **CHAPTER 20 VOLTAGE DETECTOR**.

3. The detection voltage is a TYP. value. For details, see **28.6.4** or **29.6.4 LVD circuit characteristics**.

Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. After an interrupt is generated, perform the processing according to **Figure 20-8 Processing Procedure After an Interrupt Is Generated**.

3. After a reset is released, perform the processing according to **Figure 20-9 Initial Setting of Interrupt and Reset Mode**.

Remark V_{POR}: POR power supply rise detection voltage

V_{PDR}: POR power supply fall detection voltage

24.3.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to either to V_{DD} or V_{SS} via a resistor.

24.3.4 REGC pins

Connect the REGC pin to GND via a capacitor having excellent characteristics (0.47 to 1 μF) in the same manner as during normal operation (30-pin products only). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

24.3.5 X1 and X2 pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the high-speed on-chip oscillation clock (f_{IH}) is used.

24.3.6 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, when writing to the flash memory by using the flash memory programmer and using the on-board supply voltage, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer.

CHAPTER 27 INSTRUCTION SET

This chapter lists the instructions in the RL78 microcontroller instruction set. For details of each operation and operation code, refer to the separate document **RL78 Microcontrollers User's Manual: software (R01US0015E)**.

(2) During communication at same potential (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	83.3		250		ns
SCK00 high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2-7$		$t_{KCY1}/2-50$		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2-10$		$t_{KCY1}/2-50$		ns
SI00 setup time (to SCK00↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	23		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	33		110		ns
SI00 hold time (from SCK00↑) Note2	t_{KSI1}		10		10		ns
Delay time from SCK00↓ to SO00 output Note 3	t_{KSO1}	C = 20 pF Note 4		10		10	ns

Notes 1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes "to SCK00↓" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes "from SCK00↓" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

3. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes "from SCK00↑" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

4. C is the load capacitance of the SCK00 and SO00 output lines.

Caution Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

Remarks 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

(4/4)

Page	Description	Classification
CHAPTER 28 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85 °C)		
p.733	Modification of description, and addition of target products	(c)
p.769	Modification of note 2 in 28.5.2 Serial interface IICA	(c)
p.777	Modification of title and note, and addition of caution in 28.7 RAM Data Retention Characteristics	(b)
p.777	Modification of conditions in 28.8 Flash Memory Programming Characteristics	(b)
CHAPTER 29 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105 °C)		
p.779	Modification of description, and addition of target products and remark	(c)
p.811	Modification of note 2 in 29.5.2 Serial interface IICA	(c)
p.819	Modification of title and note in 29.7 RAM Data Retention Characteristics	(b)
p.819	Modification of conditions in 29.8 Flash Memory Programming Characteristics	(b)
CHAPTER 30 PACKAGE DRAWINGS		
p.821 to 823	Addition of package name	(d)

Remark “Classification” in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note,
(d): Addition/change of package, part number, or management division, (e): Addition/change of related documents