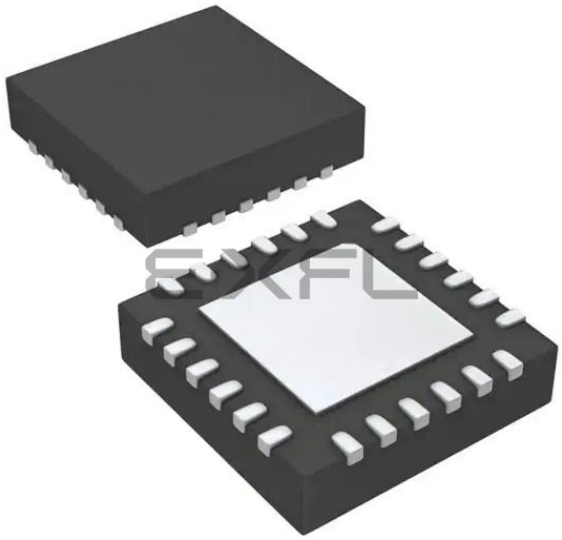


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10279dna-u0

○ ROM, RAM capacities

Code flash	Data flash	RAM	20 pins	24 pins	30 pins
16 KB	2 KB	2 KB	—	—	R5F102AA
	—		—	—	R5F103AA
	2 KB	1.5 KB	R5F1026A Note 1	R5F1027A Note 1	—
	—		R5F1036A Note 1	R5F1037A Note 1	—
12 KB	2KB	1 KB	R5F10269 Note 1	R5F10279 Note 1	R5F102A9
	—		R5F10369 Note 1	R5F10379 Note 1	R5F103A9
8 KB	2 KB	768 B	R5F10268 Note 1	R5F10278 Note 1	R5F102A8
	—		R5F10368 Note 1	R5F10378 Note 1	R5F103A8
4 KB	2KB	512 B	R5F10267	R5F10277	R5F102A7
	—		R5F10367	R5F10377	R5F103A7
2 KB	2 KB	256 B	R5F10266 Note 2	—	—
	—		R5F10366 Note 2	—	—

Notes 1. This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**.)

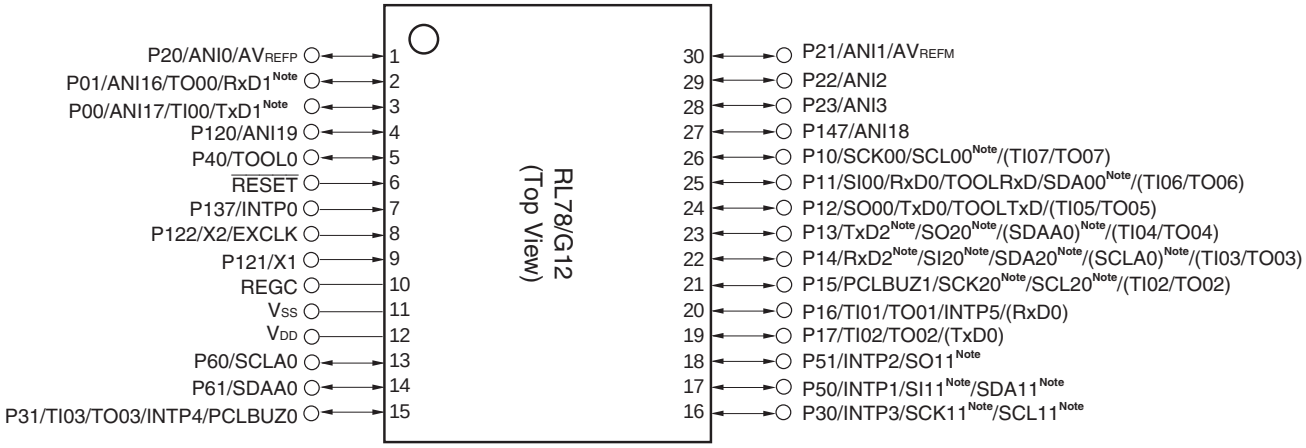
2. The self-programming function cannot be used for R5F10266 and R5F10366.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

1.4.3 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

<R>



Note Provided only in the R5F102 products.

Caution Connect the REGC pin to VSS via capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.5 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).**

1.5 Pin Identification

ANI0 to ANI3, ANI16 to ANI22:	Analog input
AV_{REFM}:	Analog Reference Voltage Minus
AV_{REFP}:	Analog reference voltage plus
EXCLK:	External Clock Input (Main System Clock)
INTP0 to INTP5	Interrupt Request From Peripheral
KR0 to KR9:	Key Return
P00 to P03:	Port 0
P10 to P17:	Port 1
P20 to P23:	Port 2
P30 to P31:	Port 3
P40 to P42:	Port 4
P50, P51:	Port 5
P60, P61:	Port 6
P120 to P122, P125:	Port 12
P137:	Port 13
P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/ Buzzer Output
REGC:	Regulator Capacitance
$\overline{\text{RESET}}$:	Reset
RxD0 to RxD2:	Receive Data
SCK00, SCK01, SCK11, SCK20:	Serial Clock Input/Output
SCL00, SCL01, SCL11, SCL20, SCLA0:	Serial Clock Input/Output
SDA00, SDA01, SDA11, SDA20, SDAA0:	Serial Data Input/Output
SI00, SI01, SI11, SI20:	Serial Data Input
SO00, SO01, SO11, SO20:	Serial Data Output
TI00 to TI07:	Timer Input
TO00 to TO07:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0 to TxD2:	Transmit Data
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)

CHAPTER 2 PIN FUNCTIONS

2.1 Port Functions

V_{DD} is the I/O buffer power supply for pins.

Set in each port I/O, buffer, pull-up resistor is also valid for alternate functions.

2.1.1 20-pin products

(1/2)

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P10	8-3-2	I/O	Analog input port	ANI16/PCLBUZ0/ SCK00/ SCL00 Note 3	Port 1. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port (in 1-bit units). Input of P10 and P11 can be set to TTL input buffer. Output of P10 to P12 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to analog input Note 1.
P11				ANI17/SI00/RxD0/ SDA00 Note 3/ TOOLRxD	
P12	7-3-2			ANI18/SO00/TxD0/ TOOLTxD	
P13	7-3-1			ANI19/TI00/TO00/ INTP2	
P14				ANI20/TI01/TO01/ INTP3	
P20	4-3-1	I/O	Analog input port	ANI0/AV_{REFP}	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input Note 2.
P21				ANI1/AV_{REFM}	
P22				ANI2	
P23				ANI3	
P40	7-1-1	I/O	Input port	KR0/TOOL0	Port 4. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port (in 1-bit units). Output of P41 can be set to N-ch open-drain output (V_{DD} tolerance). P41 and P42 can be set to analog input Note 1.
P41	7-3-2		Analog input port	ANI22/SO01 Note 3/ SDA01 Note 3/TI02/ TO02/INTP1	
P42	7-3-1			ANI21/SCK01 Note 3/ SCL01 Note 3/TI03/ TO03	
P60	12-1-1	I/O	Input port	KR4/SCLA0/(TxD0)	Port 6 2-bit I/O port. Input/output can be specified in 1-bit units. N-ch open-drain output (6-V tolerance).
P61				KR5/SDAA0/(RxD0)	

Notes 1. Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit unit).

2. Digital or analog for each pin can be selected with the A/D port configuration register (ADPC).

3. Provided only in the R5F102 products.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). For details, see **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

Figure 2-4. Pin Block Diagram for Pin Type 3-1-1

<R>

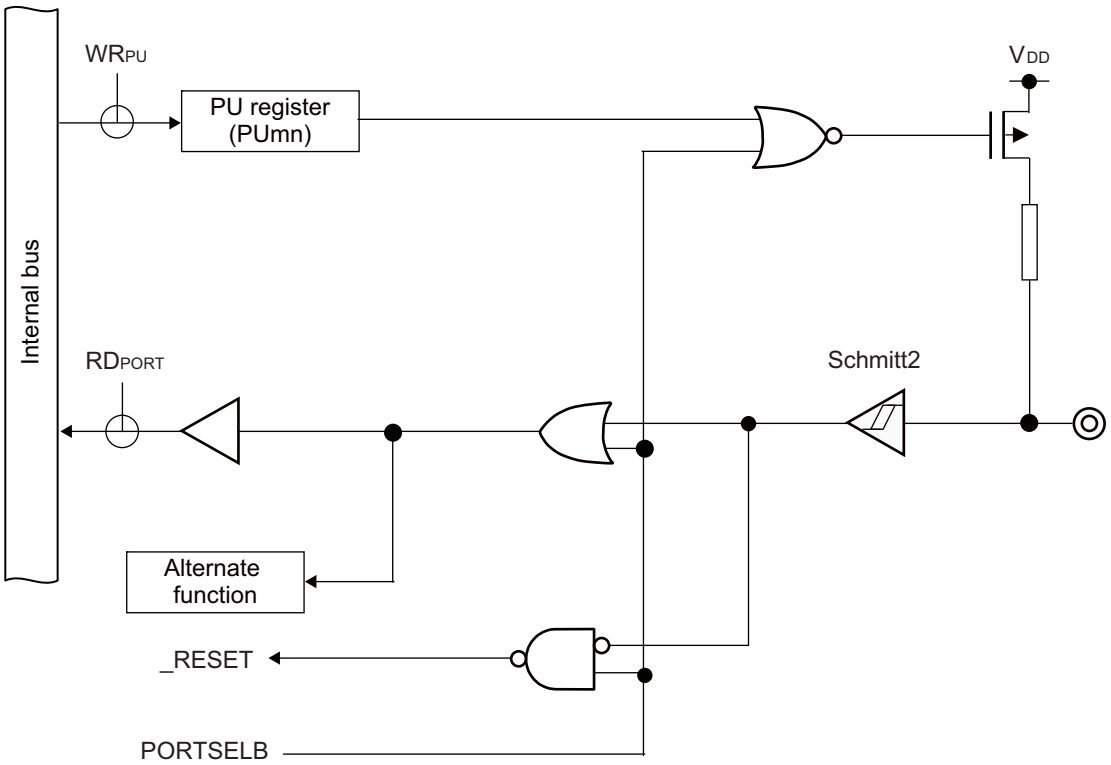
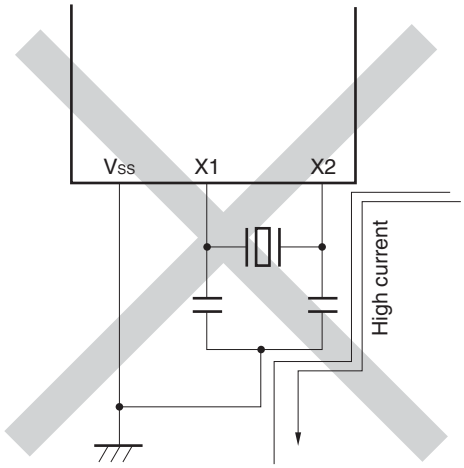
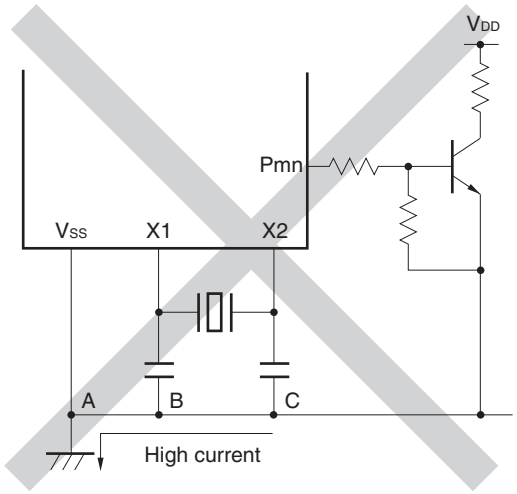


Figure 5-12. Examples of Incorrect Resonator Connection (2/2)

(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched

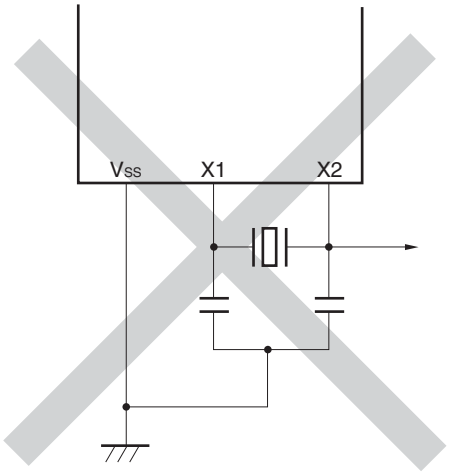


Figure 6-9. Format of Timer Mode Register 0n (TMR0n) (2/4)

Address: : F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR0n (n =2, 4, 6)	CKS 0n1	CKS 0n0	0	CCS 0n	MASTER0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR0n (n = 1, 3)	CKS 0n1	CKS 0n0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR0n (n = 0, 5, 7)	CKS 0n1	CKS 0n0	0	CCS 0n	0[Note]	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0

(Bit 11 of TMR0n (n = 2, 4, 6))

MASTER0n	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the 2, 4, 6 channel can be set as a master channel (MASTER0n = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTER0n bit to 0 for a channel that is used with the independent channel operation function.	

(Bit 11 of TMR0n (n = 1, 3))

SPLIT0n	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

STS0n2	STS0n1	STS0n0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI0n pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI0n pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Note Bit 11 is a read-only bit and fixed to 0. Writing to this bit is ignored.

Remark n: Channel number (n = 0 to 7)

Figure 6-60. Example of Set Contents of Registers to Delay Counter (2/2)

(d) Timer output level register 0 (TOL0)

	Bit n	
TOL0	TOL0n	0: Cleared to 0 when master channel output mode (TOM0n = 0).
	0	

(e) Timer output mode register 0 (TOM0)

	Bit n	
TOM0	TOM0n	0: Sets master channel output mode.
	0	

Remark n: Channel number (n = 0 to 7)

10.6.7 Hardware trigger no-wait mode (scan mode, sequential conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.

<3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.

<4> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion of the four channels ends, the A/D conversion of the channel following the specified channel automatically starts.

<5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.

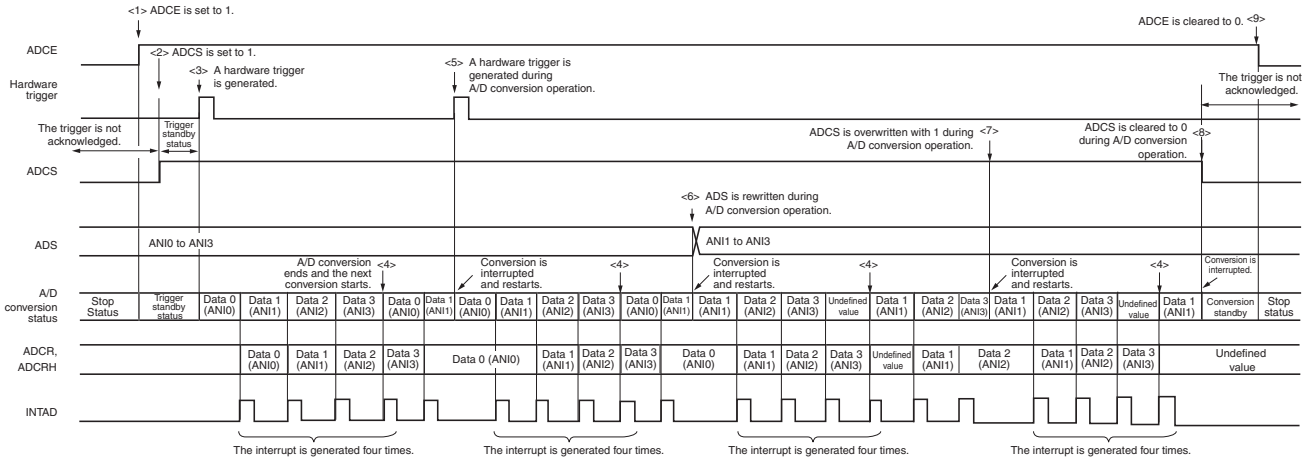
<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not power down in this status.

<9> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.

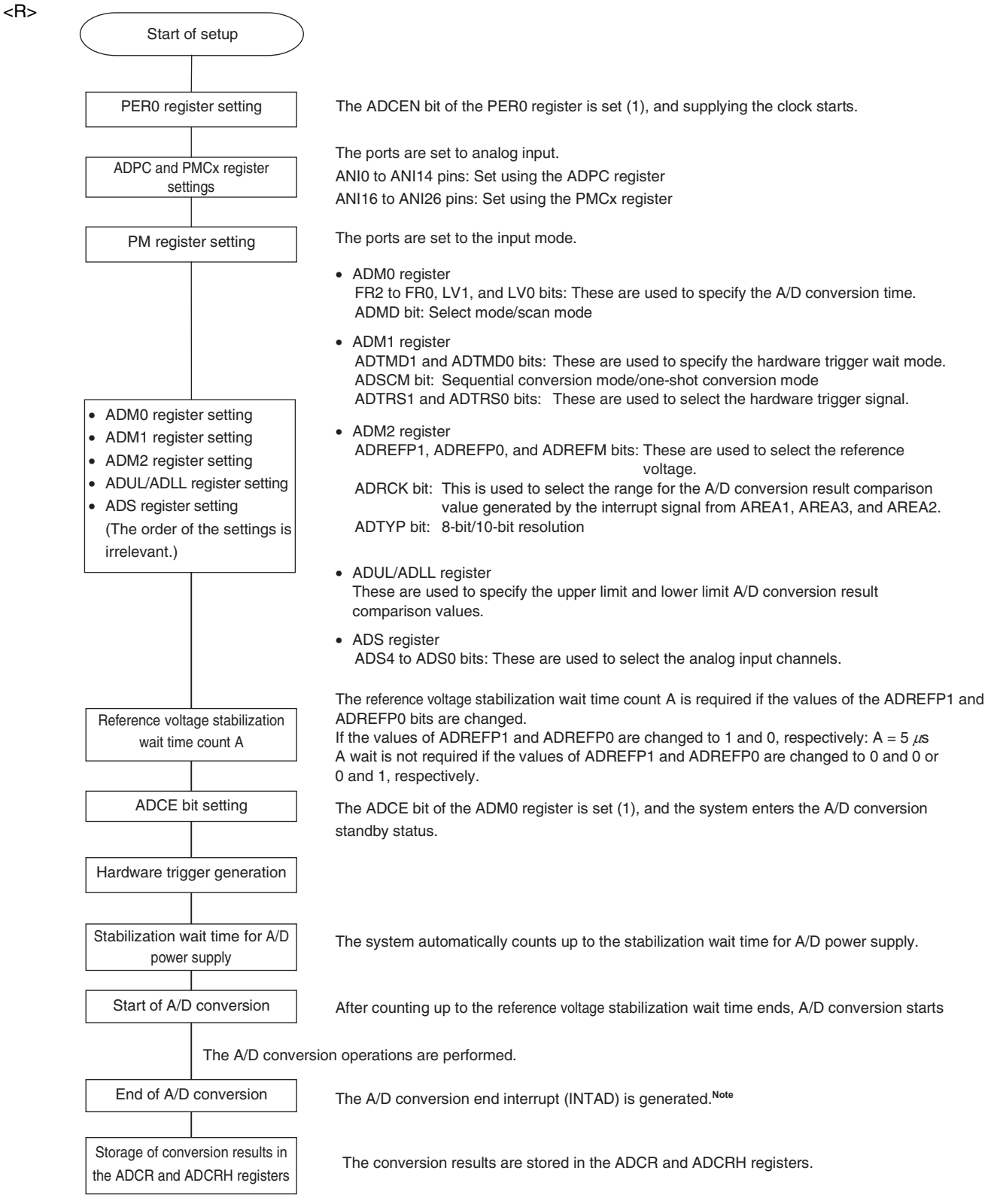
Figure 10-23. Example of Hardware Trigger No-Wait Mode (Scan Mode, Sequential Conversion Mode) Operation Timing



10.7.3 Setting up hardware trigger wait mode

Figure 10-31. Setting up Hardware Trigger Wait Mode

<R>



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR and ADCRH registers.

(10) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 10-46. Internal Equivalent Circuit of ANIn Pin

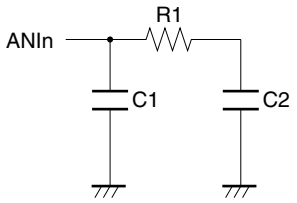


Table 10-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REFP}, V_{DD}	ANIn Pins	R1 [kΩ]	C1 [pF	C2 [pF]
3.6 V ≤ V_{DD} ≤ 5.5 V	ANI0 to ANI3	14	8	2.5
	ANI16 to ANI22	18		7.0
2.7 V ≤ V_{DD} < 3.6 V	ANI0 to ANI3	39		2.5
	ANI16 to ANI22	53		7.0
1.8 V ≤ V_{DD} < 2.7 V	ANI0 to ANI3	231		2.5
	ANI16 to ANI22	321		7.0

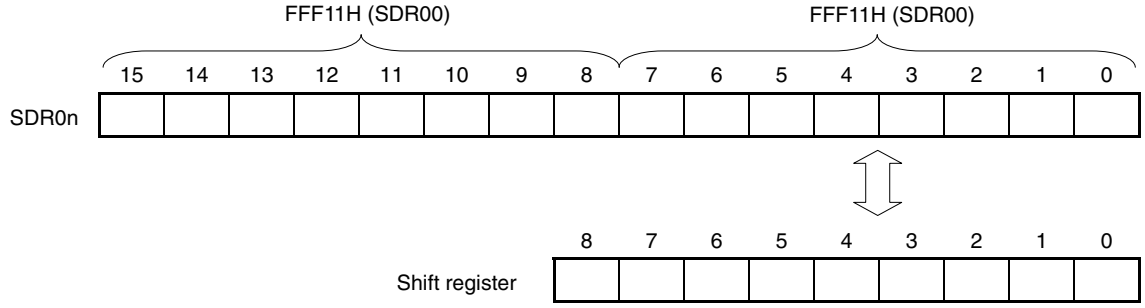
Remark The resistance and capacitance values shown in Table 10-6 are not guaranteed values.

(11) Starting the A/D converter

Start the A/D converter after the AV_{REFP} and V_{DD} voltages stabilize.

Figure 11-4. Format of Serial Data Register mn (SDRmn) (mn = 00, 01)

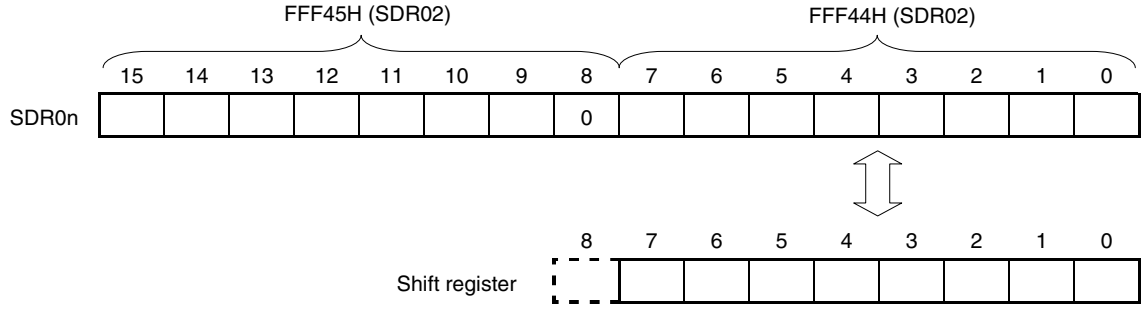
Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W



Remark For the function of the higher 7 bits of the SDRmn register, see **11.3 Registers Controlling Serial Array Unit**.

Figure 11-5. Format of Serial Data Register mn (SDRmn) (mn = 02, 03, 10, 11)

Address: FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03) After reset: 0000H R/W
FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11)



Caution Be sure to clear bit 8 to "0".

Remark For the function of the higher 7 bits of the SDRmn register, see **11.3 Registers Controlling Serial Array Unit**.

11.5.8 Calculating transfer clock frequency

The transfer clock frequency for 3-wire serial I/O (CSI00, CSI01, CSI11, CSI20) communication can be calculated by the following expressions.

(1) Master

(Transfer clock frequency) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [Hz]

(2) Slave

(Transfer clock frequency) = {Frequency of serial clock (SCK) supplied by master}[Note] [Hz]

Note The permissible maximum transfer clock frequency is f_{MCK}/6.

Remark The value of SDRmn[15:9] is the value of bits 15 to 9 of serial data register mn (SDRmn) (0000000B to 1111111B) and therefore is 0 to 127.

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

The meanings of <7> to <15> in (3) Data ~ data ~ stop condition in Figure 12-32 are explained below.

<7> After data transfer is completed, because of ACKE0 = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).

<9> The master device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WREL0 = 1). The master device then starts transferring data to the slave device.

<11> When data transfer is complete, the slave device (ACKE0 =1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<12> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).

<13> The slave device reads the received data and releases the wait status (WREL0 = 1).

<14> By the master device setting a stop condition trigger (SPT0 = 1), the bus data line is cleared (SDAA0 = 0) and the bus clock line is set (SCLA0 = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDAA0 = 1), the stop condition is then generated (i.e. SCLA0 =1 changes SDAA0 from 0 to 1).

<15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICA0: stop condition).

Remark <1> to <15> in Figure 12-32 show the entire procedure for communicating data using the I^2C bus.
Figure 12-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 12-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 12-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

CHAPTER 20 VOLTAGE DETECTOR

20.1 Functions of Voltage Detector

The operation mode and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector is set by using the option byte (000C1H).

The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}), and generates an internal reset or interrupt request signal.
- The detection level for the power supply detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by using the option byte as one of 12 levels (For details, see **CHAPTER 23 OPTION BYTE**).
- Operable in STOP mode.
- <R> After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in **28.4** or **29.4 AC Characteristics.** This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H).

(a) Interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0)

The two detection voltages (V_{LVDH}, V_{LVDL}) are selected by the option byte 000C1H. The high-voltage detection level (V_{LVDH}) is used for releasing resets and generating interrupts. The low-voltage detection level (V_{LVDL}) is used for generating resets.

(b) Reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for generating/releasing resets.

(c) Interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for releasing resets/generating interrupts.

The reset and interrupt request signals are generated in each mode as follows.

<R>

Interrupt & reset mode (LVIMDS1, LVIMDS0 = 1, 0)	Reset mode (LVIMDS1, LVIMDS0 = 1, 1)	Interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)
Generates an interrupt request signal by detecting $V_{DD} < V_{LVDH}$ when the operating voltage falls, and an internal reset by detecting $V_{DD} < V_{LVDL}$. Releases an internal reset by detecting $V_{DD} \geq V_{LVDH}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$. Generates an internal reset signal by detecting $V_{DD} < V_{LVD}$.	Retains the state of an internal reset by the LVD immediately after a reset until $V_{DD} \geq V_{LVD}$. Releases the LVD internal reset by detecting $V_{DD} \geq V_{LVD}$. Generates an interrupt request signal (INTLVI) by detecting $V_{DD} < V_{LVD}$ or $V_{DD} \geq V_{LVD}$ after the LVD internal reset is released.

While the voltage detector is operating, whether the supply voltage is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).

Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **CHAPTER 18 RESET FUNCTION**.

23.1.2 On-chip debug option byte (000C3H)

- Control of on-chip debug operation
  - On-chip debug operation is disabled or enabled.
- Handling of data of flash memory in case of failure in on-chip debug security ID authentication
  - Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

The dedicated flash memory programmer generates the following signals for the RL78 microcontroller. See the manual of PG-FP5, FL-PR5, or E1 on-chip debugging emulator for details.

Table 24-2. Pin Connection

Dedicated Flash Memory Programmer				RL78 Microcontroller
Signal Name		I/O	Pin Function	Pin Name
PG-FP5, FL-PR5	E1 on-chip debugging emulator			
V_{DD}		I/O	V_{DD} voltage generation/power monitoring	V_{DD}
GND		–	Ground	V_{SS}, REGC Note
FLMD1	EMV_{DD}	–	Driving power for TOOL0 pin	V_{DD}
/RESET	–	Output	Reset signal	$\overline{RESET}$
–	$\overline{RESET}$	Output		
–	TOOL0	I/O	Transmit/receive signal	TOOL0
SI/RxD	–	I/O	Transmit/receive signal	

Note Connect REGC pin to ground via a capacitor (0.47 to 1 μF) (30-pin products only).

Caution Pins to be connected differ with the product. For details, see Table 24-1.

24.2 Serial Programming Using External Device (that Incorporates UART)

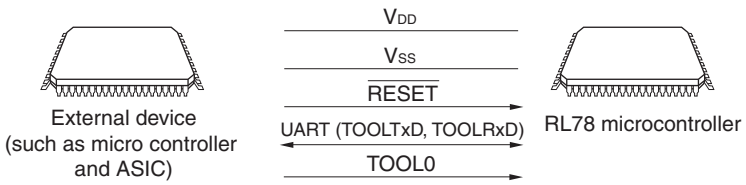
On-board data writing to the internal flash memory is possible by using the RL78 microcontroller and an external device (a microcontroller or ASIC) connected to a UART.

On the development of flash memory programmer by user, refer to the **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

24.2.1 Programming environment

The environment required for writing a program to the flash memory of the RL78 microcontroller is illustrated below.

Figure 24-3. Environment for Writing Program to Flash Memory



Processing to write data to or delete data from the RL78 microcontroller by using an external device is performed on-board. Off-board writing is not possible.

24.8.3 Procedure for accessing data flash memory

The data flash memory is stopped after a reset ends. To access the data flash, make initial settings according to the following procedure.

<1> Set bit 0 (DFLEN) of the data flash control register (DFLCTL) to 1.
<2> Wait for the setup to finish for software timer, etc.
The time setup takes differs for each flash operation mode for the main clock.
<Setup time for each flash operation mode>
- HS (High speed main): 5 μs
- LS (Low speed main): 720 ns

<3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.
2. Transition to the STOP mode is not possible during the setup time. To enter the STOP mode during the setup time, clear DFLEN to 0 and then execute the STOP instruction.
3. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, the high-speed on-chip oscillator clock should be operated (HIOSTOP = 0). The data flash library should be executed after 30 μs have elapsed.

After initial setting, the data flash can be read through CPU instructions and can be read or rewritten to by using the data flash library.

Follow one of the procedures below when the DMA controller operates during access to the data flash memory.

(A) Hold DMA transfer pending or forcibly terminate it
Before reading the data flash memory, hold the DMA transfer pending in all the channels which are in use. The data flash memory should be read 3 clocks (f_{CLK}) or more after the DWAITn bit is set to 1. After reading the data flash memory, set the DWAITn bit to 0 and then cancel the pending status.
Or, before reading the data flash memory, forcibly terminate the DMA transfer in accordance with the process described in **15.5.5 Forced termination by software**. Resume the DMA transfer after reading the data flash memory.

(B) Access the data flash memory by using the library
Access the data flash memory by using the latest data flash library.

(C) Insert the NOP instruction
Insert the NOP instruction immediately before the data flash read instruction.
<Example>

```
MOVW  HL, !addr16  ; Read RAM
NOP                ; Insert the NOP instruction before reading the data flash memory
MOV  A,[DE]        ; Read the data flash memory
```

If high-level language like C language is used, the compiler may generate two instructions per code. At that time, the NOP instruction is not inserted immediately before the data flash read instruction. Read the data flash memory by following procedure (A) or (B).

Remark f_{CLK}: CPU/peripheral hardware clock frequency

28.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode

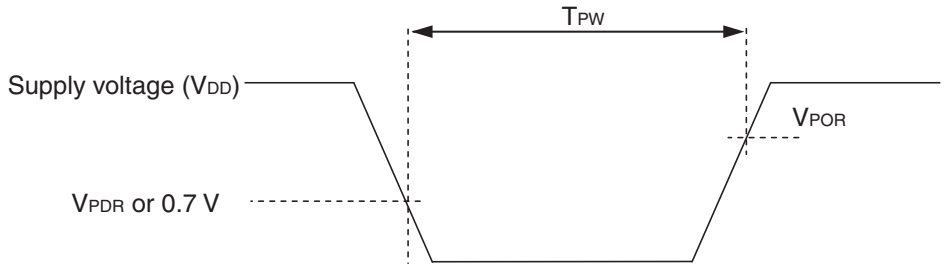
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

28.6.3 POR circuit characteristics

(T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width Note	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



28.9 Dedicated Flash Memory Programmer Communication (UART)

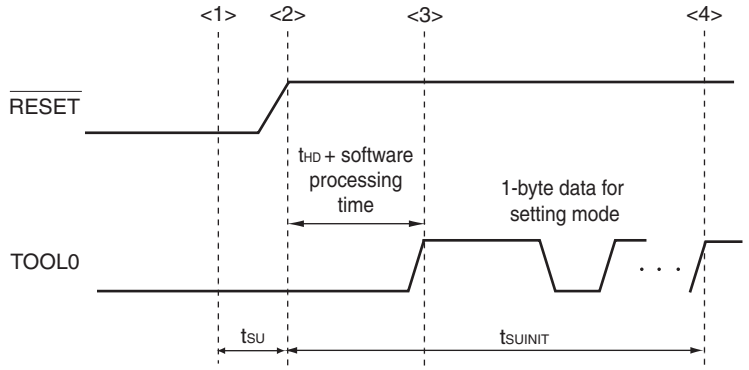
(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

28.10 Timing of Entry to Flash Memory Programming Modes

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external reset release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external reset release	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)