Section	Page	Description
5.4.2 Data Array	152	Description amended The address array is mapped to H'F1000000 to H'F1FFFFFF. To access an element of the data array, the 32-bit address field (for read/write access) and 32-bit data field (for write access) must be specified. The address field specifies the information that selects the entry to be accessed; the data field specifies the longword data to be written to the data array. In the address field, specify the entry's address in bits 11-4, L in bits 3-2 to indicate the longword's position within a line (which consists of 16 bytes), W in bits 13-12 to select the way, and H'F1 in bits 31-24 to indicate access to the data array. The L bits (3-2) specification is in the following form: 00 is longword 0, 01 is longword 1, 10 is longword 2, and 11 is longword 3. Settings for the W bits (13-12) are as follows: 00 is way 0, 01 is way 1, 10 is way 2, and 11 is way 3. Since access is not allowed crossing longword boundaries, always set 00 in bits 1-0 of the address field. The following two operations on the data array are possible. Note that these operations will not change the information in the address array. (1) Data Array Read Reads the data at the position selected by the L bits (3-2) of the address field from the entry that corresponds to the entry address and way that were specified in the address field. (2) Data Array Write Writes the longword data set in the data field into the entry that corresponds to the entry address and way that were specified in the address field. The longword data will be written to the entry at the position selected by the L bits (3-2) of the address field.

The correspondence between DSP data transfer operands and registers is shown in table 2.29. CPU core registers are used as a pointer address that indicates a memory address.

Table 2.29 Correspondence between DSP Data Transfer Operands and Registers

Register		Ax	Ix	Dx	Ay	Iy	Dy	Da	As	Is	Ds
CPU register	R0										
	R1										
	R2 (As2)								Yes		
	R3 (As3)								Yes		
	R4 (Ax0, As0)	Yes							Yes		
	R5 (Ax1, As1)	Yes							Yes		
	R6 (Ay0)				Yes						
	R7 (Ay1)				Yes						
	R8 (Ix, Is)		Yes							Yes	
	R9 (Iy)					Yes					
DSP register	A0							Yes			Yes
	A1							Yes			Yes
	M0										Yes
	M1										Yes
	X0			Yes							Yes
	X1			Yes							Yes
	Y0						Yes				Yes
	Y1						Yes				Yes
	A0G										Yes
	A1G										Yes

Table 2.32 DSP Operation Instructions

Instruction		Instruction Code	Operation	Execution States	DC
	PMULS Se,Sf,Dg	111110*********	Se * Sf → Dg (signed)	1	—
		0100eeff0000gg00			
	PADD Sx,Sy,Du	111110*********	Sx + Sy → Du	1	*
	PMULS Se,Sf,Dg	0111eeffxxyygguu	Se * Sf → Dg (signed)		
	PSUB Sx,Sy,Du	111110*********	Sx – Sy → Du	1	*
	PMULS Se,Sf,Dg	0110eeffxxyygguu	Se * Sf → Dg (signed)		
	PADD Sx,Sy,Dz	111110*********	Sx + Sy → Dz	1	*
		10110001xxyyzzzz			
DCT	PADD Sx,Sy,Dz	111110*********	If DC = 1, Sx + Sy → Dz	1	*
		10110010xxyyzzzz	If DC = 0, nop		
DCF	PADD Sx,Sy,Dz	111110*********	If DC = 0, Sx + Sy → Dz	1	*
		10110011xxyyzzzz	If DC = 1, nop		
	PSUB Sx,Sy,Dz	111110*********	Sx – Sy → Dz	1	*
		10100001xxyyzzzz			
DCT	PSUB Sx,Sy,Dz	111110*********	If DC = 1, Sx – Sy → Dz	1	—
		10100010xxyyzzzz	If DC = 0, nop		
DCF	PSUB Sx,Sy,Dz	111110*********	If DC = 0, Sx – Sy → Dz	1	—
		10100011xxyyzzzz	If DC = 1, nop		
	PSHA Sx,Sy,Dz	111110*********	If Sy > = 0, Sx << Sy → Dz (arithmetic shift)	1	*
		1010001xxyyzzzz	If Sy<0, Sx>>Sy → Dz		
DCT	PSHA Sx,Sy,Dz	111110*********	If DC = 1 & Sy > = 0, Sx << Sy → Dz (arithmetic shift)	1	—
		10010010xxyyzzzz	If DC = 1 & Sy < 0, Sx >> Sy → Dz		
			If DC = 0, nop		

Note: * See table 2.33.

Interrupt Source		INTEVT Code (INTEVT2 Code)	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
SCIF	ERI2	H'200–3C0[*1] (H'900)	0–15 (0)	IPRE (7–4)	High	High
	RXI2	H'200–3C0[*1] (H'920)			↕	
	BRI2	H'200–3C0[*1] (H'940)				
	TXI2	H'200–3C0[*1] (H'960)			Low	
ADC	ADI	H'200–3C0[*1] (H'980)	0–15 (0)	IPRE (3–0)	—	
TMU0	TUNI0	H'400 (H'400)	0–15 (0)	IPRA (15–12)	—	
TMU1	TUNI1	H'420 (H'420)	0–15 (0)	IPRA (11–8)	—	
TMU2	TUNI2	H'440 (H'440)	0–15 (0)	IPRA (7–4)	High	
	TICPI2	H'460 (H'460)			Low	
RTC	ATI	H'480 (H'480)	0–15 (0)	IPRA (3–0)	High	
	PRI	H'4A0 (H'4A0)			↕	
	CUI	H'4C0 (H'4C0)			Low	
SCI	ERI	H'4E0 (H'4E0)	0–15 (0)	IPRB (7–4)	High	
	RXI	H'500 (H'500)			↕	
	TXI	H'520 (H'520)				
	TEI	H'540 (H'540)			Low	
WDT	ITI	H'560 (H'560)	0–15 (0)	IPRB (15–12)	—	
REF	RCMI	H'580 (H'580)	0–15 (0)	IPRB (11–8)	High	
	ROVI	H'5A0 (H'5A0)			Low	Low

Notes: 1. The code corresponding to an interrupt level shown in table 7.6 is set.

2. When $\overline{\text{IRLS3}}$–$\overline{\text{IRLS0}}$ are enabled, IRL is the higher level of $\overline{\text{IRL3}}$–$\overline{\text{IRL0}}$ and $\overline{\text{IRLS3}}$–$\overline{\text{IRLS0}}$.

Bit 7—Standby (STBY): Specifies transition to standby mode.

Bit 7: STBY	Description	
0	Executing SLEEP instruction puts chip into sleep mode	(Initial value)
1	Executing SLEEP instruction puts chip into standby mode	

Bits 6, 5, and 3—Reserved: These bits are always read as 0. The write value should always be 0.

Bit 4—Standby Crystal (STBXTL): Specifies halting or operating of the clock pulse generator in standby mode.

Bit 4: STBXTL	Description
0	Clock pulse generator is halted in standby mode
1	Clock pulse generator is operates in standby mode

Bit 2—Module Standby 2 (MSTP2): Specifies halting of the clock supply to the timer unit TMU (an on-chip peripheral module). When the MSTP2 bit is set to 1, the supply of the clock to the TMU is halted.

Bit 2: MSTP2	Description	
0	TMU runs	(Initial value)
1	Clock supply to TMU is halted	

Bit 1—Module Standby 1 (MSTP1): Specifies halting of the clock supply to the realtime clock RTC (an on-chip peripheral module). When the MSTP1 bit is set to 1, the supply of the clock to the RTC is halted. When the clock halts, all RTC registers become inaccessible, but the counter keeps running.

Bit 1: MSTP1	Description	
0	RTC runs	(Initial value)
1	Clock supply to RTC is halted	

Before switching the RTC to module standby, access at least one among the registers RTC, SCI, and TMU.

Bit 0—Module Standby 0 (MSTP0): Specifies halting of the clock supply to the serial communication interface SCI (an on-chip peripheral module). When the MSTP0 bit is set to 1, the supply of the clock to the SCI is halted.

Cautions:

1. The input to divider 1 becomes the output of PLL circuit 1 when PLL circuit 1 is on.
2. The input of divider 2 becomes the output of PLL circuit 1.
3. The frequency of the internal clock (Iϕ) becomes:
   - The product of the frequency of the CKIO pin, the frequency multiplication ratio of PLL circuit 1, and the division ratio of divider 1 when PLL circuit 1 is on.
   - Do not set the internal clock frequency lower than the CKIO pin frequency.

Bit 15—Area 6 Wait Control (A6W3): Specifies the number of inserted wait states for area 6 combined with bits A6W2–A6W0 in WCR2. Also specifies the number of transfer states in burst transfer. Clear this bit to 0 when area 6 is not set to PCMCIA.

				First Cycle		Burst Cycle	
A6W3	A6W2	A6W1	A6W0	Inserted Wait States	$\overline{\text{WAIT}}$ Pin	Number of States per One-data Transfer	$\overline{\text{WAIT}}$ Pin
0	0	0	0	0	Ignored	2	Enabled
0	0	0	1	1	Enabled	2	Enabled
0	0	1	0	2	Enabled	3	Enabled
0	0	1	1	3	Enabled	4	Enabled
0	1	0	0	4	Enabled	5	Enabled
0	1	0	1	6	Enabled	7	Enabled
0	1	1	0	8	Enabled	9	Enabled
0	1	1	1	10 (Initial value)	Enabled	11	Enabled
1	0	0	0	12	Enabled	13	Enabled
1	0	0	1	14	Enabled	15	Enabled
1	0	1	0	18	Enabled	19	Enabled
1	0	1	1	22	Enabled	23	Enabled
1	1	0	0	26	Enabled	27	Enabled
1	1	0	1	30	Enabled	31	Enabled
1	1	1	0	34	Enabled	35	Enabled
1	1	1	1	38	Enabled	39	Enabled

Bit 14—Area 5 Wait Control (A5W3): Specifies the number of inserted wait states for area 5 combined with bits A5W2–A5W0 in WCR2. Also specifies the number of transfer states in burst transfer. Clear this bit to 0 when area 5 is not set to PCMCIA.

The relationship between the set value and the number of waits is the same as for A6W3.

Bits 13 and 12—Reserved: These bits are always read as 0. The write value should always be 0.

11.3.2 Description of Areas

Area 0: Area 0 physical address bits A28–A26 are 000. Address bits A31–A29 are ignored and the address range is H'00000000 + H'20000000 × n – H'03FFFFFF + H'20000000 × n (n = 0–6 and n = 1–6 are the shadow spaces).

Ordinary memories such as SRAM, ROM, and burst ROM can be connected to this space. Byte, word, or longword can be selected as the bus width using external pins MD3 and MD4. When the area 0 space is accessed, the $\overline{CS0}$ signal is asserted. The $\overline{RD}$ signal that can be used as $\overline{OE}$ and the $\overline{WE0}$–$\overline{WE3}$ signals for write control are also asserted. The number of bus cycles is selected between 0 and 10 wait cycles using the A0W2–A0W0 bits in WCR2. When the burst function is used, the bus cycle pitch of the burst cycle is determined within a range of 2–10 according to the number of waits.

Area 1: Area 1 physical address bits A28–A26 are 001. Address bits A31–A29 are ignored and the address range is H'04000000 + H'20000000 × n – H'07FFFFFF + H'20000000 × n (n = 0–6 and n = 1–6 are the shadow spaces).

Area 1 is the area specifically for internal peripheral modules. External memories cannot be connected.

Control registers of the peripheral modules shown below are mapped to this area 1. Their addresses are physical addresses, to which logical addresses can be mapped when the MMU is enabled:

DMAC, PORT, IrDA, SCIF, ADC, DAC, INTC (except INTEVT, IPRA, IPRB)

These registers must be set not to be cached.

Area 2: Area 2 physical address bits A28–A26 are 010. Address bits A31–A29 are ignored and the address range is H'08000000 + H'20000000 × n – H'0BFFFFFF + H'20000000 × n (n = 0–6 and n = 1–6 are the shadow spaces).

Ordinary memories such as SRAM and ROM, as well as synchronous DRAM, can be connected to this space. Byte, word, or longword can be selected as the bus width using bits A2SZ1 and A2SZ0 in BCR2 for ordinary memory.

When the area 2 space is accessed, the $\overline{CS2}$ signal is asserted. When ordinary memories are connected, the $\overline{RD}$ signal that can be used as $\overline{OE}$ and the $\overline{WE0}$–$\overline{WE3}$ signals for write control are also asserted and the number of bus cycles is selected between 0 and 3 wait cycles using bits A2W1 and A2W0 bits in WCR2.

When synchronous DRAM is connected, the $\overline{RAS3U}$ and $\overline{RAS3L}$ signals, $\overline{CASU}$ and $\overline{CASL}$ signals, RD/$\overline{WR}$ signal, and byte control signals DQMHH, DQMHL, DQMLH, and DQMLL are

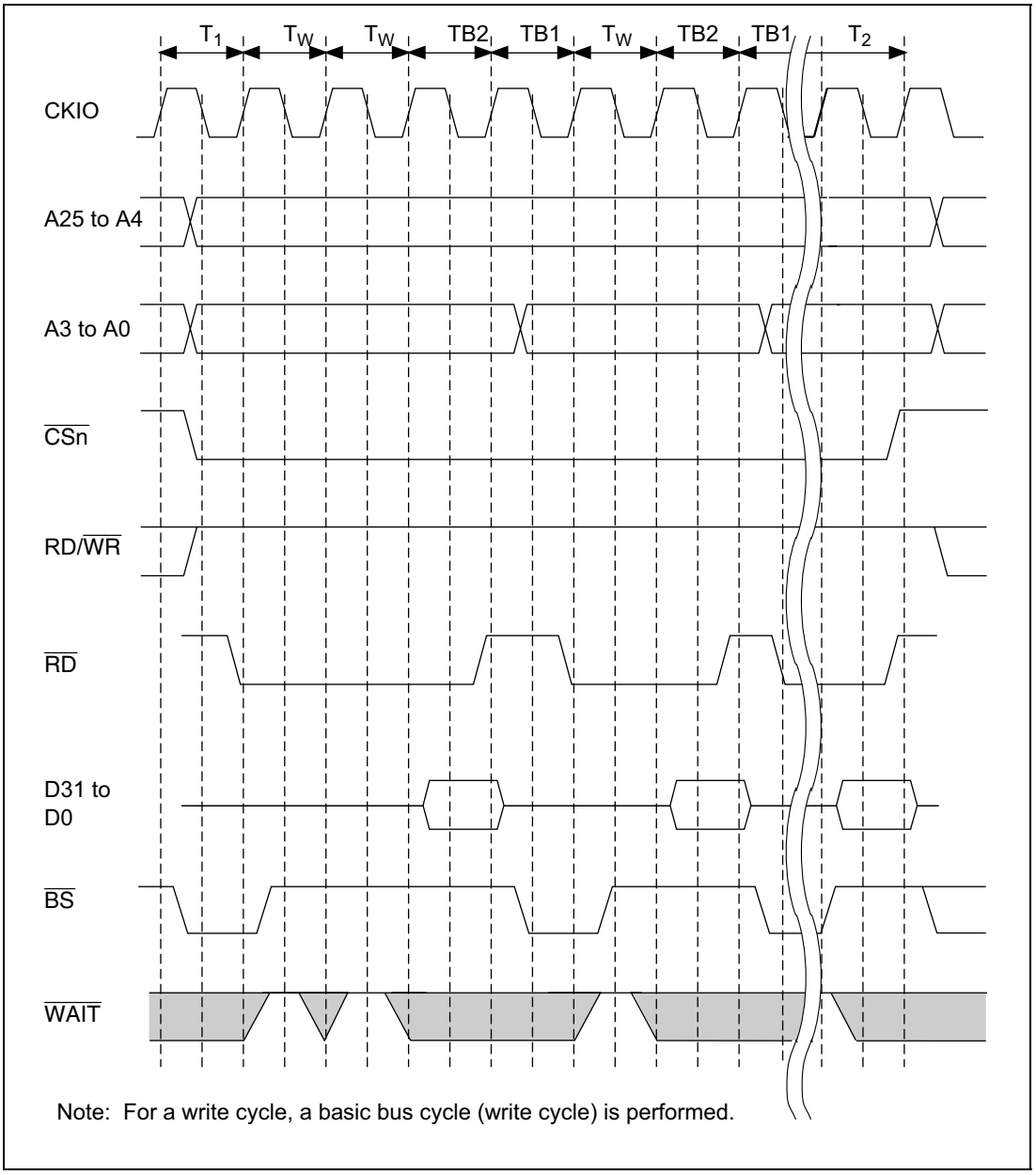


Figure 11.29 Burst ROM Wait Access Timing

11.3.10 $\overline{\text{MCS[0]}}$ to $\overline{\text{MCS[7]}}$ Pin Control

The SH7729R is provided with pins $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ as dedicated $\overline{\text{CS}}$ pins for the ROM connected to area 0 or 2. Assertion of $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ is controlled by settings in MCSCR0–MCSCR7. This enables 32-, 64-, 128-, or 256-Mbit memory to be connected to area 0 or area 2. However, only CS2/0 = 0 (area 0) should be used for MCSCR0. Table 11.15 shows MCSCR0–MCSCR7 settings and $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ assertion conditions.

As the $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$ pins are multiplexed as the PTC0–PTC7 pins, when using these pins as $\overline{\text{MCS[0]}}$–$\overline{\text{MCS[7]}}$, the corresponding bits in the PCCR register should be set to “other function.”

When CS2/0 = 0 in the MCSCR0 and when the PTC0 pin is switched to $\overline{\text{MCS[0]}}$ (when PCOMD1–PCOMD0 are set to “other function”), the $\overline{\text{CS0}}$ pin is also switched to $\overline{\text{MCS[0]}}$.

As port register writes operate on the peripheral clock, they take time compared with instruction execution by the CPU operating on the high-speed internal clock. Therefore, if an instruction that accesses $\overline{\text{MCS[1]}}$ to $\overline{\text{MCS[7]}}$ is located several instructions after an instruction that switches port C to $\overline{\text{MCS}}$, the switch from PTC[n] to $\overline{\text{MCSn}}$ and from $\overline{\text{CS0}}$ to $\overline{\text{MCS[0]}}$ may not be performed correctly.

To prevent this problem, the following switching procedure should be used.

- When the program runs with cache on

(1) To switch port C to $\overline{\text{MCS}}$, set the corresponding bits in the PCCR register to 00 ("other function").

(2) Read the PCCR register and check whether the set value is read. Repeat until the set value is read.

(3) Perform a dummy read from non-cacheable CS0 space (e.g. address H'A0000000). This will result in an access to the CS0 space, and immediately afterward, CS0 will be switched to $\overline{\text{MCS[0]}}$, and port C[n] will be switched to $\overline{\text{MCS[n]}}$.

(4) Access can now be made to the $\overline{\text{MCS[1]}}$ to $\overline{\text{MCS[7]}}$ spaces.

- When the program runs in $\overline{\text{MCS[0]}}$ space with cache off

(1) Set the PCCR register as in (1) above.

(2) Place at least three NOP instructions after the instruction in (1). As a result, when the PCCR register is rewritten, an access to the CS0 space will be generated, and immediately afterward, CS0 will be switched to $\overline{\text{MCS[0]}}$, and port C[n] will be switched to $\overline{\text{MCS[n]}}$.

(3) Access can now be made to the $\overline{\text{MCS[1]}}$ to $\overline{\text{MCS[7]}}$ spaces.

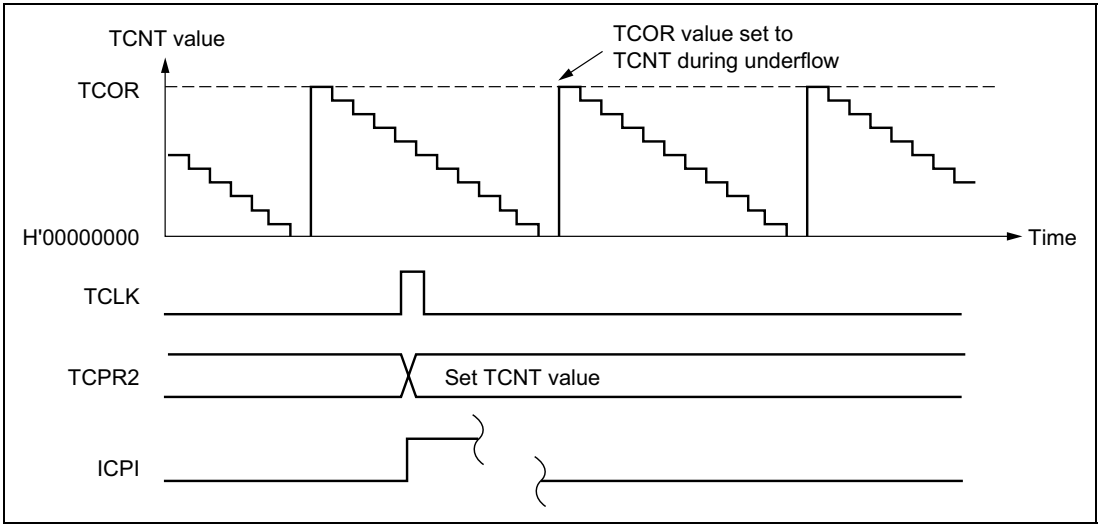


Figure 13.7 Operation Timing when Using Input Capture Function (Using TCLK Rising Edge)

13.4 Interrupts

There are two sources of TMU interrupts: underflow interrupts (TUNI) and interrupts when using the input capture function (TICPI2).

13.4.1 Status Flag Setting Timing

UNF is set to 1 when the TCNT underflows. Figure 13.8 shows the timing.

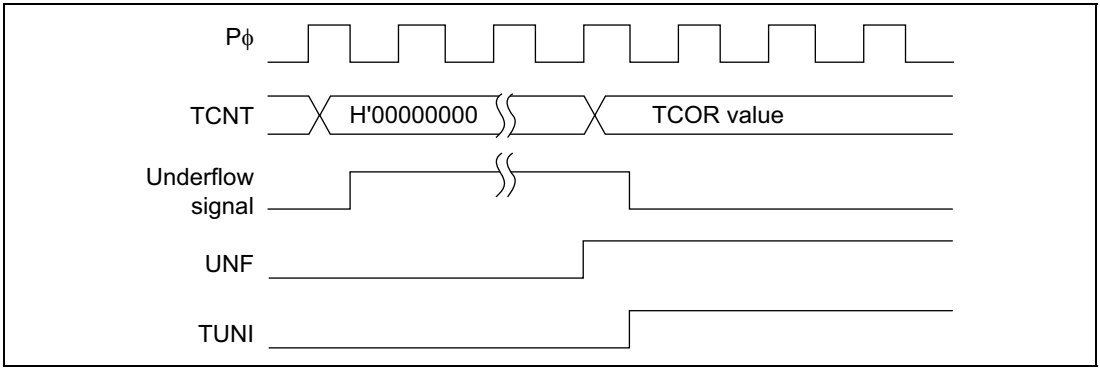


Figure 13.8 UNF Setting Timing

14.1.4 RTC Register Configuration

Table 14.2 shows the RTC register configuration.

Table 14.2 RTC Registers

Name	Abbreviation	R/W	Initial Value	Address	Access Size
64-Hz counter	R64CNT	R	Undefined	H'FFFFFEC0	8
Second counter	RSECCNT	R/W	Undefined	H'FFFFFEC2	8
Minute counter	RMINCNT	R/W	Undefined	H'FFFFFEC4	8
Hour counter	RHRCNT	R/W	Undefined	H'FFFFFEC6	8
Day of week counter	RWKCNT	R/W	Undefined	H'FFFFFEC8	8
Date counter	RDAYCNT	R/W	Undefined	H'FFFFFECA	8
Month counter	RMONCNT	R/W	Undefined	H'FFFFFECC	8
Year counter	RYRCNT	R/W	Undefined	H'FFFFFECE	8
Second alarm register	RSECAR	R/W	Undefined*	H'FFFFFED0	8
Minute alarm register	RMINAR	R/W	Undefined*	H'FFFFFED2	8
Hour alarm register	RHRAR	R/W	Undefined*	H'FFFFFED4	8
Day of week alarm register	RWKAR	R/W	Undefined*	H'FFFFFED6	8
Date alarm register	RDAYAR	R/W	Undefined*	H'FFFFFED8	8
Month alarm register	RMONAR	R/W	Undefined*	H'FFFFFEDA	8
RTC control register 1	RCR1	R/W	H'00	H'FFFFFEDC	8
RTC control register 2	RCR2	R/W	H'09	H'FFFFFEDE	8

Note: * Only the ENB bits of each register are initialized.

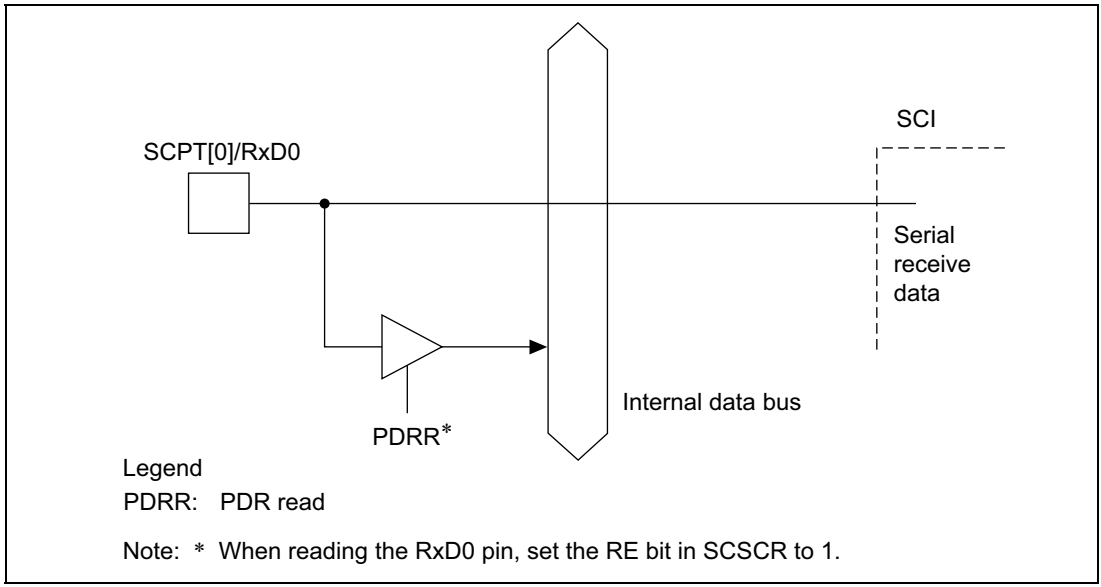


Figure 15.4 SCPT[0]/RxD0 Pin

15.1.3 Pin Configuration

The SCI has the serial pins summarized in table 15.1.

Table 15.1 SCI Pins

Pin Name	Abbreviation	I/O	Function
Serial clock pin	SCK0	I/O	Clock I/O
Receive data pin	RxD0	Input	Receive data input
Transmit data pin	TxD0	Output	Transmit data output

Note: These pins are made to function as serial pins by performing SCI operation settings with the TE, RE, CKEI, and CKEO bits in SCSCR and the C/$\overline{A}$ bit in SCSMR. Break state transmission and detection can be performed by means of the SCI's SCSPTR register.

17.2.10 FIFO Data Count Register (SCFDR)

SCFDR is a 16-bit register which indicates the quantity of data stored in the transmit FIFO data register (SCFTDR) and the receive FIFO data register (SCFRDR). It indicates the quantity of transmit data in SCFTDR with the upper 8 bits, and the quantity of receive data in SCFRDR with the lower 8 bits. SCFDR can always be read by the CPU.

Upper 8 Bits:	15	14	13	12	11	10	9	8
	—	—	—	T4	T3	T2	T1	T0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

The upper 8 bits of SCFDR indicate the quantity of non-transmitted data stored in SCFTDR. H'00 means no transmit data, and H'10 means that SCFTDR is full of transmit data.

Lower 8 Bits:	7	6	5	4	3	2	1	0
	—	—	—	R4	R3	R2	R1	R0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

The lower 8 bits of SCFDR indicate the quantity of receive data stored in SCFRDR. H'00 means no receive data, and H'10 means that SCFRDR full of receive data.

20.7 Port F

Port F is an 8-bit input port with the pin configuration shown in figure 20.6. Each pin has an input pull-up MOS, which is controlled by the port F control register (PFCR) in the PFC.

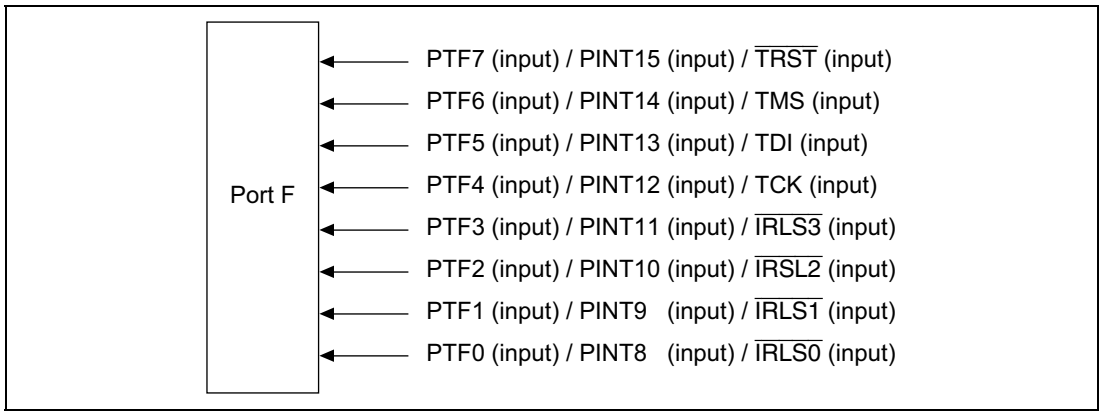


Figure 20.6 Port F

20.7.1 Register Description

Table 20.11 summarizes the port F register.

Table 20.11 Port F Register

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port F data register	PFDR	R	H'**	H'0400012A (H'A400012A)*1	8

Notes: This register is located in area 1 of physical space. Therefore, when the cache is on, either access this register from the P2 area of logical space or else make an appropriate setting using the MMU so that this register is not cached.

* Means no value.

1. When address translation by the MMU does not apply, the address in parentheses should be used.

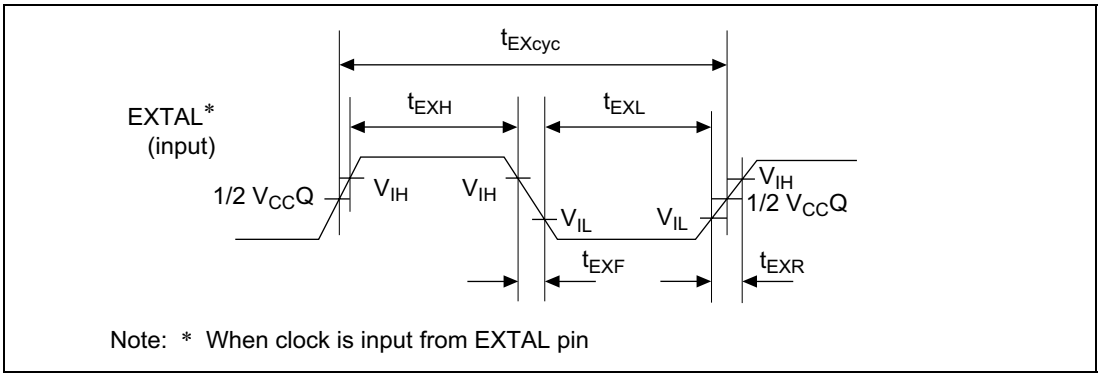


Figure 24.1 EXTAL Clock Input Timing

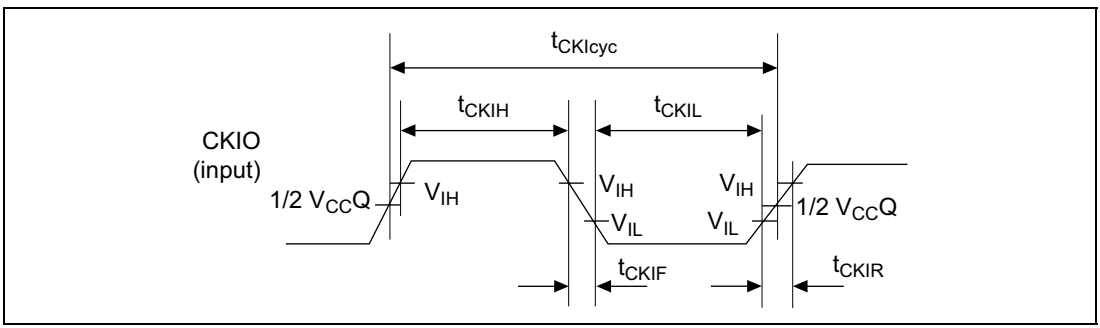


Figure 24.2 CKIO Clock Input Timing

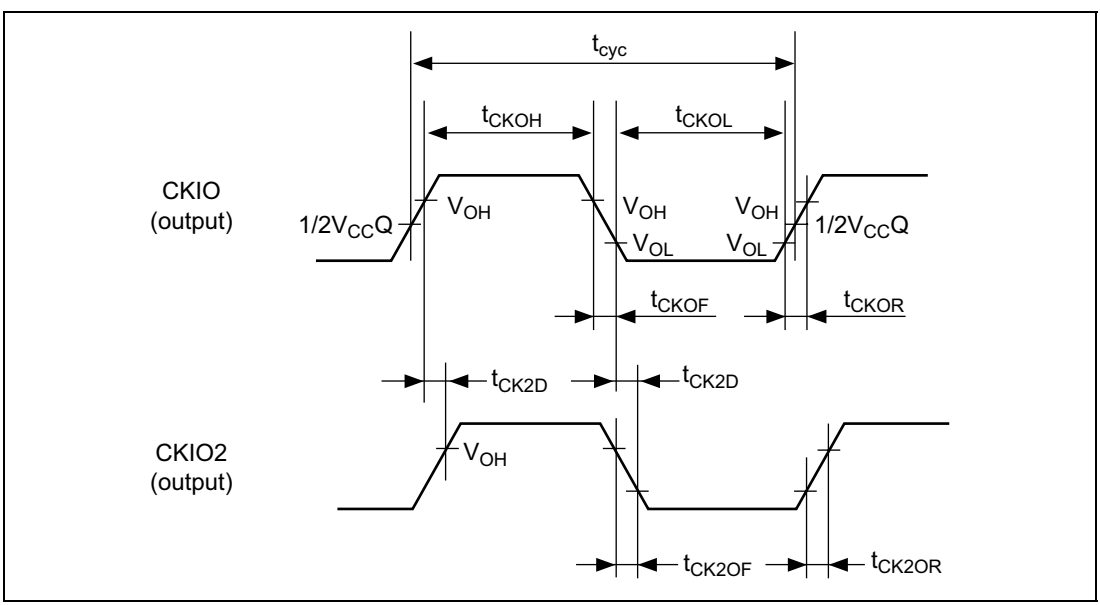


Figure 24.3 CKIO Clock Output Timing

24.3.6 Synchronous DRAM Timing

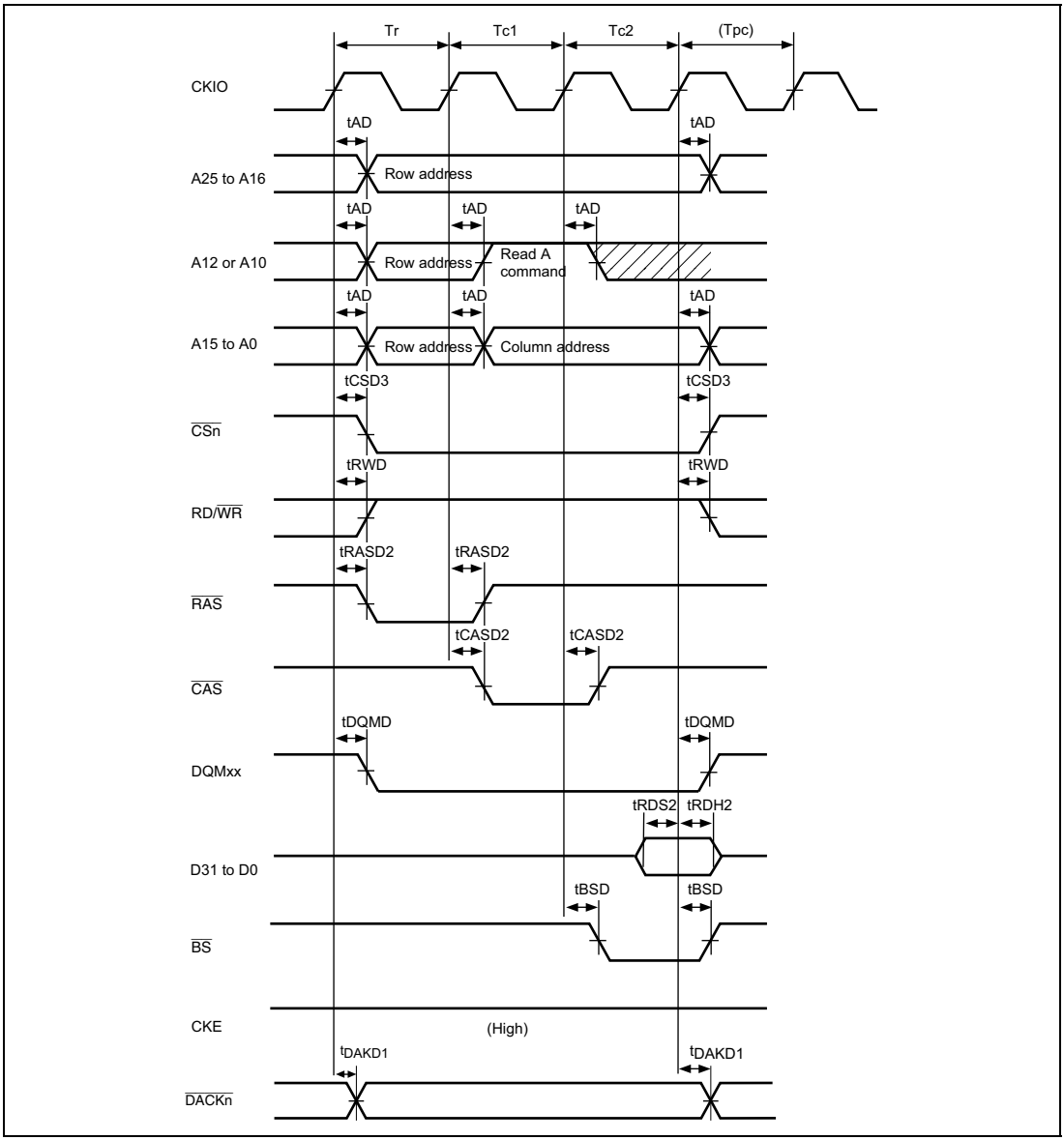


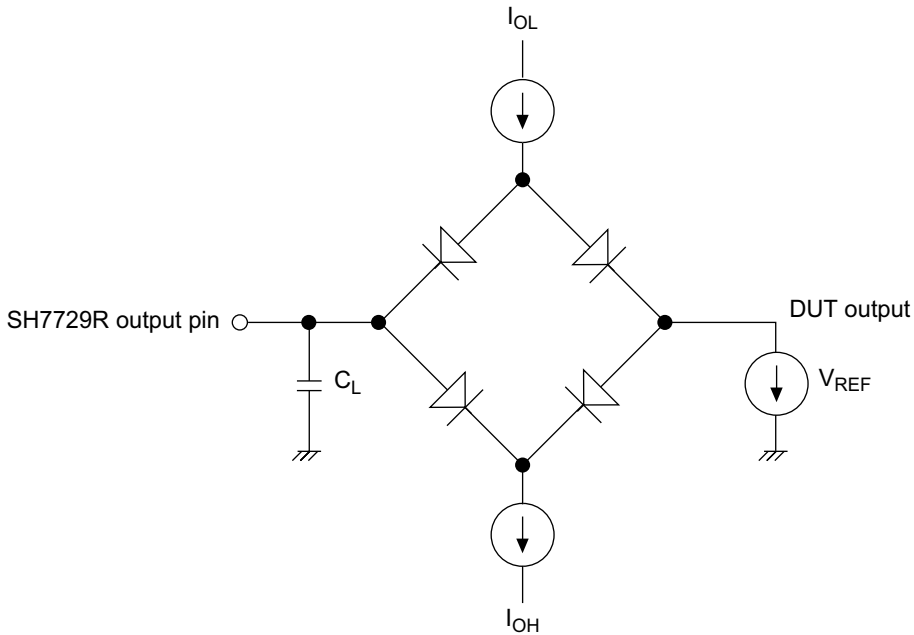
Figure 24.22 Synchronous DRAM Read Bus Cycle (RCD = 0, CAS Latency = 1, TPC = 0)

24.3.10 AC Characteristic Test Conditions

I/O signal reference level: VccQ/2 (VccQ = 3.3 ± 0.3 V, Vcc = 1.55 V to 2.15 V)

Input pulse level: Vss to 3.0 V (where $\overline{\text{RESETP}}$, $\overline{\text{RESETM}}$, ASEMD0, IRL3 to IRL0, IRLS3 to IRLS0, ADTRG, PINT15 to PINT0, $\overline{\text{TRST}}$, RxD1, CA, NMI, $\overline{\text{IRQ5}}$–$\overline{\text{IRQ0}}$, CKIO, and MD5–MD0 are within Vss to Vcc)

Input rise and fall times: 1 ns



Notes: 1. C_L is the total value that includes the capacitance of measurement instruments, etc., and is set as follows for each pin.
30pF: CKIO, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{CS0}}$, $\overline{\text{CS2}}$–$\overline{\text{CS6}}$, $\overline{\text{CE2A}}$, $\overline{\text{CE2B}}$, $\overline{\text{BACK}}$
50pF: All other pins
2. I_{OL} and I_{OH} are the values shown in table 24.3.

Figure 24.59 Output Load Circuit