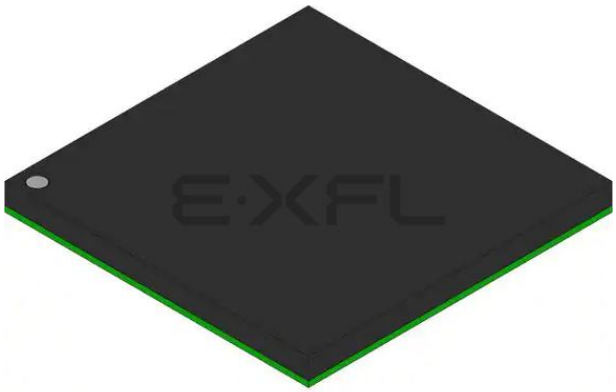

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mx21scvk

- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Reference Documentation

The following documents are required for a complete description of the i.MX21S and are necessary to design properly with the device. Especially for those not familiar with the ARM926EJ-S processor the following documents are helpful when used in conjunction with this manual.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM7TDMI Data Sheet (ARM Ltd., order number ARM DDI 0029)

ARM920T Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

MC9328MX21S Product Brief (order number MC9328MX21SPB)

The Freescale manuals are available on the Freescale Semiconductor Web site at http://www.freescale.com. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

1.3 Ordering Information

Table 1 provides ordering information for the device.

Table 1. Ordering Information

Part Order Number	Package Size	Package Type	Operating Range
MC9328MX21SVK	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	0°C–70°C
MC9328MX21SCVK	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	-40°C–85°C
MC9328MX21SVM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	0°C–70°C
MC9328MX21SCVM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	-40°C–85°C

1.4 Features

The i.MX21S boasts a robust array of features that can support a wide variety of applications. Below is a brief description of i.MX21S features.

- ARM926EJ-S Core Complex
- Display and Video Modules
  - — LCD Controller (LCDC)
  - — Smart LCD Controller (SLCDC)
- Wireless Connectivity
  - — Fast Infra-Red Interface (FIRI)
- Wired Connectivity
  - — USB On-The-Go (USBOTG) Controller

  - Three Universal Asynchronous Receiver/Transmitters (UART*x*)
  - Two Configurable Serial Peripheral Interfaces (CSPI*x*) for High Speed Data Transfer
  - Inter-IC (I^2C) Bus Module
  - Two Synchronous Serial Interfaces (SSI) with Inter-IC Sound (I^2S)
  - Digital Audio Mux
  - One-Wire Controller
  - Keypad Interface
- Memory Expansion and I/O Card Support
  - Two Multimedia Card and Secure Digital (MMC/SD) Host Controller Modules
- Memory Interface
  - External Interface Module (EIM)
  - SDRAM Controller (SDRAMC)
  - NAND Flash Controller (NFC)
  - PCMCIA/CF Interface
- Standard System Resources
  - Clock Generation Module (CGM) and Power Control Module
  - Three General-Purpose 32-Bit Counters/Timers
  - Watchdog Timer
  - Real-Time Clock/Sampling Timer (RTC)
  - Pulse-Width Modulator (PWM) Module
  - Direct Memory Access Controller (DMAC)
  - General-Purpose I/O (GPIO) Ports
  - Debug Capability

2 Signal Descriptions

Table 2 identifies and describes the i.MX21S signals. Pin assignment is provided in Section 4, “Pin Assignment and Package Information” and in the “Signal Multiplexing Scheme” table within the reference manual.

The connections of the pins in Table 2 depends solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX21S processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_48M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- TEST_WB[2:0]: These signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not utilizing these signals for GPIO functionality or for their other multiplexed function, then configure as GPIO input with pull up enabled, and leave as a no connect.
- TEST_WB[4:3]: To ensure proper operation, leave these signals as no connects.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
USBH1_RXDP	USB Host1 Receive Data Plus input signal. This signal is multiplexed with UART4_RXD and SLCDC1_DAT6. It also provides an alternative multiplex for $\overline{\text{UART4\_RTS}}$, where this signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter.
USBH1_RXDM	USB Host1 Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT5. It also provides an alternative multiplex for $\overline{\text{UART4\_CTS}}$.
USBH1_TXDP	USB Host1 Transmit Data Plus output signal. This signal is multiplexed with $\overline{\text{UART4\_CTS}}$ and SLCDC1_DAT4. It also provides an alternative multiplex for UART4_RXD, where this signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter.
USBH1_TXDM	USB Host1 Transmit Data Minus output signal. Multiplexed with UART4_TXD and SLCDC1_DAT3.
USBH1_RXDAT	USB Host1 Transceiver differential data receive signal. Multiplexed with USBH1_FS.
$\overline{\text{USBH1\_OE}}$	USB Host1 Output Enable signal. This signal is muxed with SLCDC1_DAT2.
USBH1_FS	USB Host1 Full Speed output signal. Multiplexed with $\overline{\text{UART4\_RTS}}$ and SLCDC1_DAT1 and USBH1_RXDAT.
$\overline{\text{USBH\_ON}}$	USB Host transceiver ON output signal. This signal is muxed with SLCDC1_DAT0.
USBG_SCL	USB OTG I^2C Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8.
USBG_SDA	USB OTG I^2C Data input/output signal. This signal is multiplexed with SLCDC1_DAT7.
$\overline{\text{USBG\_TXR\_INT}}$	USB OTG transceiver interrupt input. Multiplexed with USBG_FS.
Secure Digital Interface	
SD1_CMD	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added.
SD1_CLK	SD Output Clock.
SD1_D[3:0]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added.
SD2_CMD	SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1.
SD2_CLK	SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1.
SD2_D[3:0]	SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1.
UARTs – IrDA/Auto-Bauding (Note: UART2 is not used in the MC9328MX21S)	
UART1_RXD	Receive Data input signal
UART1_TXD	Transmit Data output signal
$\overline{\text{UART1\_RTS}}$	Request to Send input signal
$\overline{\text{UART1\_CTS}}$	Clear to Send output signal
UART3_RXD	Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI.
UART3_TXD	Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI.
$\overline{\text{UART3\_RTS}}$	Request to Send input signal
$\overline{\text{UART3\_CTS}}$	Clear to Send output signal
UART4_RXD	Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP.
UART4_TXD	Transmit Data output signal which is multiplexed with USBH1_TXDM.
$\overline{\text{UART4\_RTS}}$	Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave
SYS_CLK1	SSI1 master clock. Multiplexed with TOUT.
SSI2_CLK	Serial clock signal which is output in master or input in slave.
SSI2_TXD	Transmit serial data signal
SSI2_RXD	Receive serial data
SSI2_FS	Frame Sync signal which is output in master and input in slave.
SYS_CLK2	SSI2 master clock. Multiplexed with TOUT.
SSI3_CLK	Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK
SSI3_TXD	Transmit serial data signal which is multiplexed with SLCDC2_CS
SSI3_RXD	Receive serial data which is multiplexed with SLCDC2_RS
SSI3_FS	Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0.
SAP_CLK	Serial clock signal which is output in master or input in slave.
SAP_TXD	Transmit serial data
SAP_RXD	Receive serial data
SAP_FS	Frame Sync signal which is output in master and input in slave.
I^2C	
I2C_CLK	I^2C Clock
I2C_DATA	I^2C Data
1-Wire	
OWIRE	1-Wire input and output signal. This signal is multiplexed with JTAG RTCK.
PWM	
PWMO	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module.
General Purpose Input/Output	
PB[10:21], PF[16]	Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled.
Keypad	
KP_COL[7:0]	Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2\_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available.

Table 5. DC Characteristics (Continued)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V
Input leakage current (no pull-up or pull-down)	I_{in}	V_{in} = 0 or NVDD	–	–	±1	µA
I/O leakage current	I_{OZ}	$V_{I/O}$ = NVDD or 0 I/O = High impedance state	–	–	±5	µA

1. Data labeled Typical is not guaranteed, but is intended as an indication of the IC's potential performance.
2. For DSCR definition refer to the System Control chapter in the reference manual.

Table 6 shows the input and output capacitance for the device.

Table 6. Input/Output Capacitance

Parameter	Symbol	Min	Typ	Max	Units
Input capacitance	C_i	_	_	5	pF
Output capacitance	C_o	_	_	5	pF

Table 7 shows the power consumption for the device.

Table 7. Power Consumption

ID	Parameter	Conditions	Symbol	Typ	Max	Units
1	Run Current	QVDD = QVDDX = 1.65 V, NVDD1 = 1.8 V. NVDD2 through NVDD6 = VDDA = 3.1V. Core = 266 MHz, System = 133 MHz. MPEG4 Playback (QVGA) from MMC/SD card, 30fps, 44.1kHz audio.	I_{QVDD} + I_{QVDDX}	120	–	mA
			I_{NVDD1}	8	–	mA
			I_{NVDD2} through I_{NVDD6} + I_{VDDA}	6.6	–	mA
2	Sleep Current	Standby current with Well Biasing System enabled. Well Bias Control Register (WBCR) must be set as follows: WBCR: CRM_WBS bits = 01 CRM_WBFA bit = 1 CRM_WBM bits = 001 CRM_SPA_SEL bit = 1 FMCR bit = 1 For WBCR definition refer to System Control Chapter in the reference manual.	**I_{STBY}**			
			QVDD = QVDDX = 1.65V, TA[1]	–	3.0	mA
			QVDD = QVDDX = 1.65V, 25°	–	700	µA
			QVDD = QVDDX = 1.55V, 25°	320	–	µA

1. TA = 70°C for suffixes VK, VM, DVK, DVM, and SVK. TA = 85°C for suffixes CVK, CVM, and SCVK.

3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 11. In this table, T_{ref} is a reference clock period after the predivider and T_{dck} is the output double clock period.

Table 11. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock frequency range	Vcc = 1.5V	16	–	320	MHz
Pre-divider output clock frequency range	Vcc = 1.5V	16	–	32	MHz
Double clock frequency range	Vcc = 1.5V	220	–	560	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Frequency lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	350	400	450	T_{ref}
Frequency lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	280	330	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	480	530	580	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	360	410	460	T_{ref}
Frequency jitter (p-p)	–	–	0.02	0.03	$2 \bullet T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.7V	–	1.0	1.5	ns
Power dissipation	FOL mode, integer MF, f_{dck} = 560 MHz, Vcc = 1.5V	–	1.5	–	mW (Avg)

3.6 Reset Module

The timing relationships of the Reset module with the $\overline{\text{POR}}$ and $\overline{\text{RESET\_IN}}$ are shown in Figure 2 and Figure 3. Be aware that NVDD must ramp up to at least 1.7V for NVDD1 and 2.7V for NVDD2-6 before QVDD is powered up to prevent forward biasing.

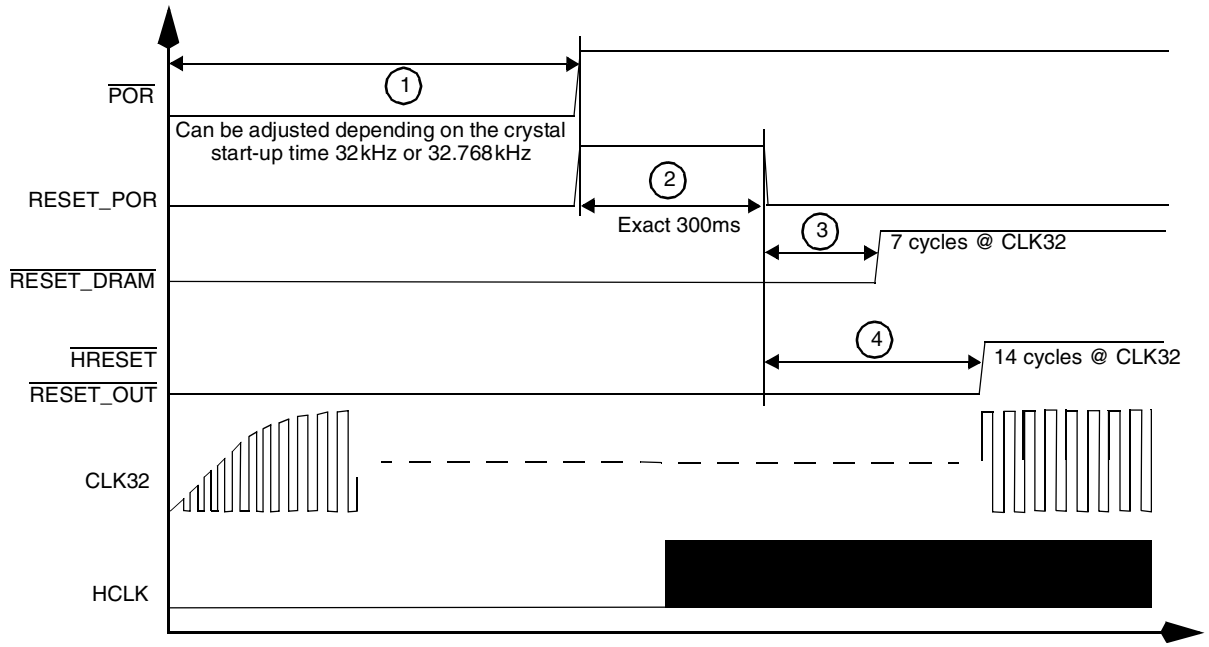


Figure 2. Timing Relationship with $\overline{\text{POR}}$

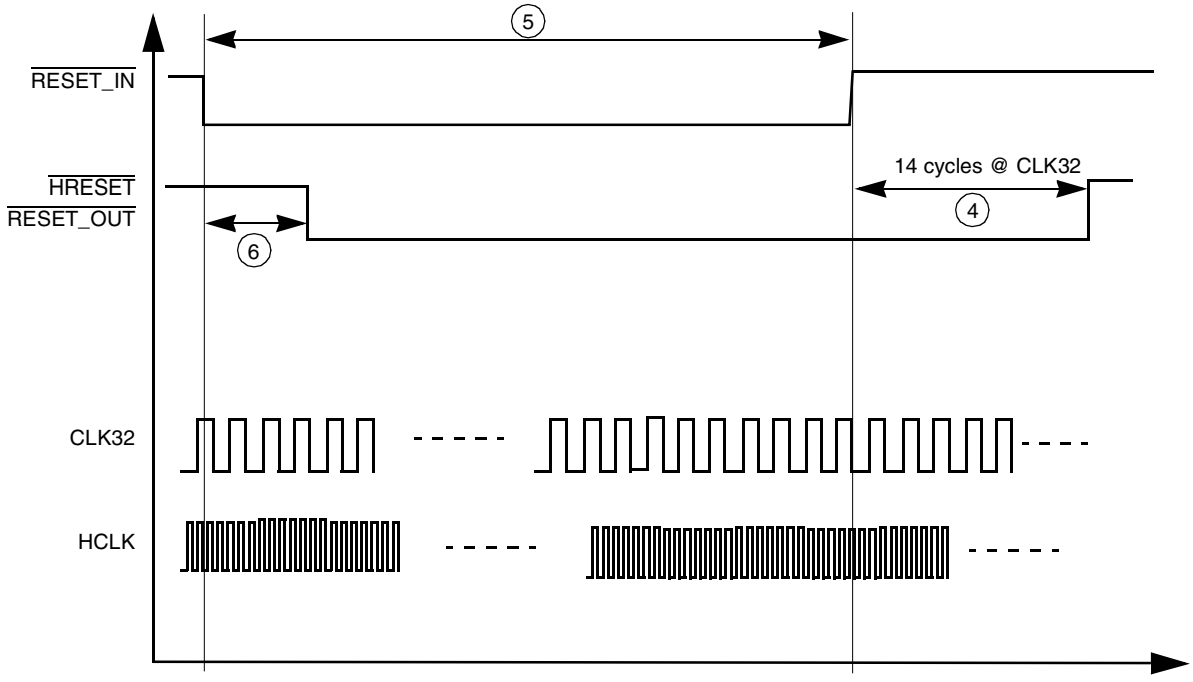


Figure 3. Timing Relationship with $\overline{\text{RESET\_IN}}$

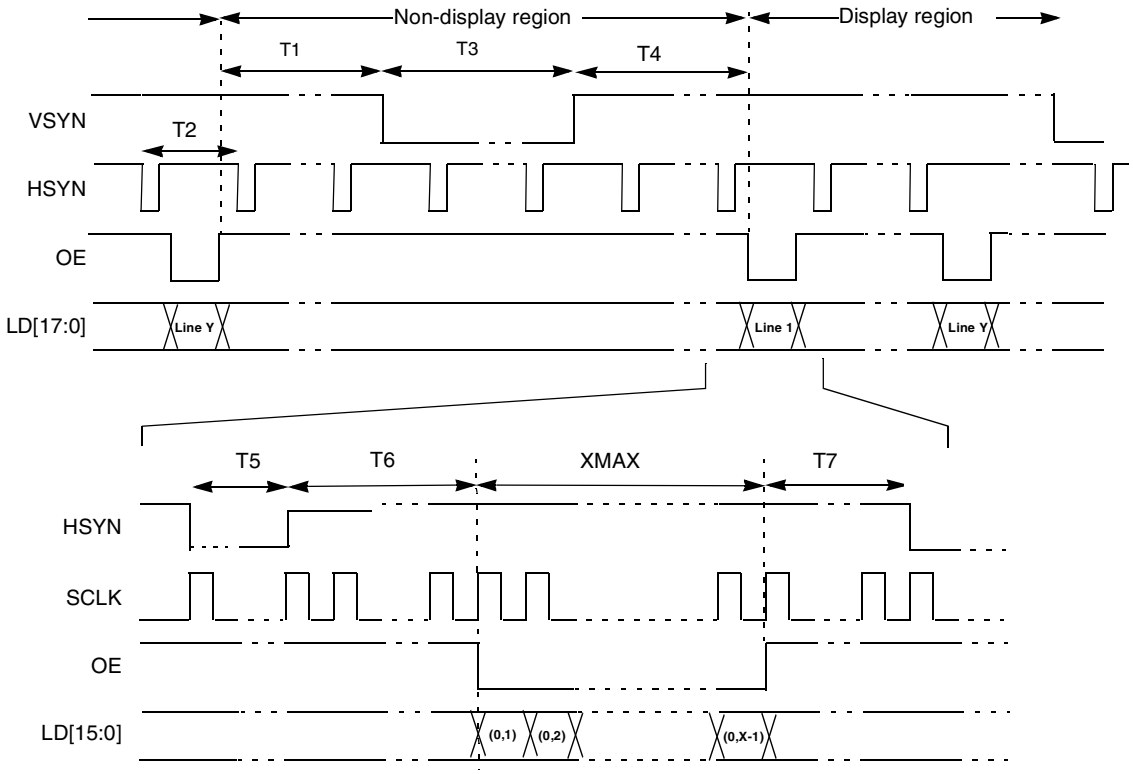


Figure 12. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 16. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	End of OE to beginning of VSYN	T5+T6+T7-1	(VWAIT1·T2)+T5+T6+T7-1	Ts
T2	HSYN period	–	XMAX+T5+T6+T7	Ts
T3	VSYN pulse width	T2	VWIDTH·T2	Ts
T4	End of VSYN to beginning of OE	1	(VWAIT2·T2)+1	Ts
T5	HSYN pulse width	1	HWIDTH+1	Ts
T6	End of HSYN to beginning to OE	3	HWAIT2+3	Ts
T7	End of OE to beginning of HSYN	1	HWAIT1+1	Ts

Note:
- Ts is the SCLK period.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 12, all 3 signals are active low.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 12, SCLK is always active.
- XMAX is defined in number of pixels in one line.

Table 19. SLCDC Serial Transfer Timing

Symbol	Description	Minimum	Maximum	Unit
T1	Pixel clock period	42	962	ns
T2	Chip select setup time	5	–	ns
T3	Chip select hold time	5	–	ns
T4	Data setup time	5	–	ns
T4	Data hold time	5	–	ns
T6	Register select setup time	5	–	ns
T7	Register select hold time	5	–	ns

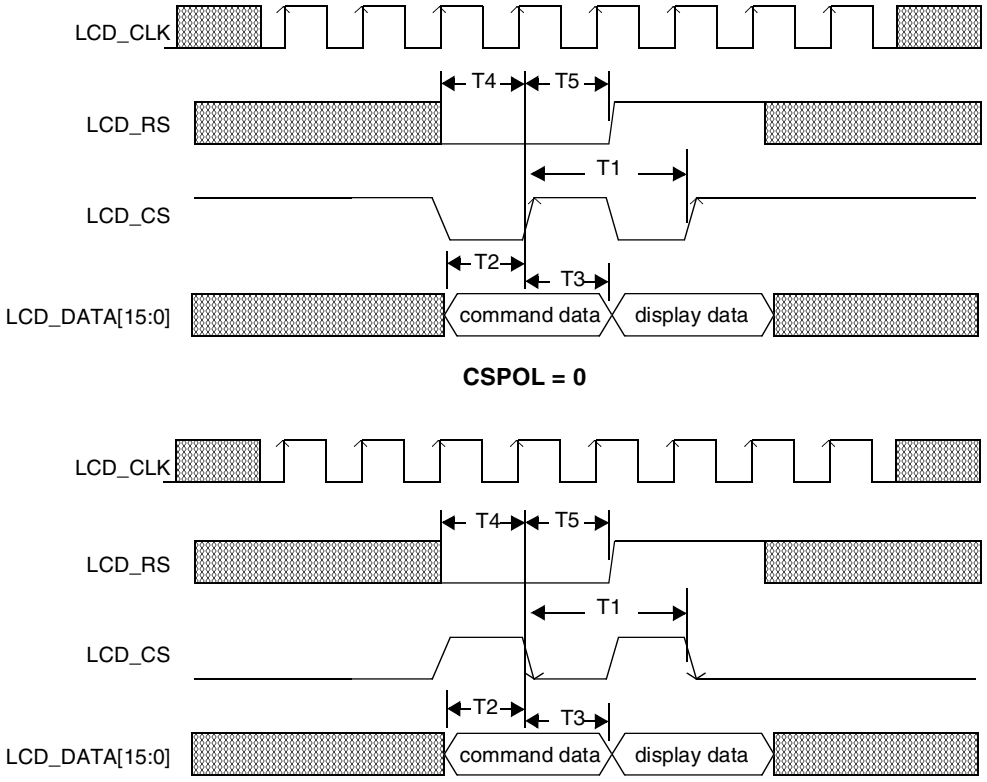


Figure 16. SLCDC Parallel Transfers Timing

Table 20. SLCDC Parallel Transfers Timing

Symbol	Description	Minimum	Maximum	Unit
T1	Pixel clock period	23	962	ns
T2	Data setup time	5	–	ns
T3	Data hold time	5	–	ns
T4	Register select setup time	5	–	ns
T5	Register select hold time	5	–	ns

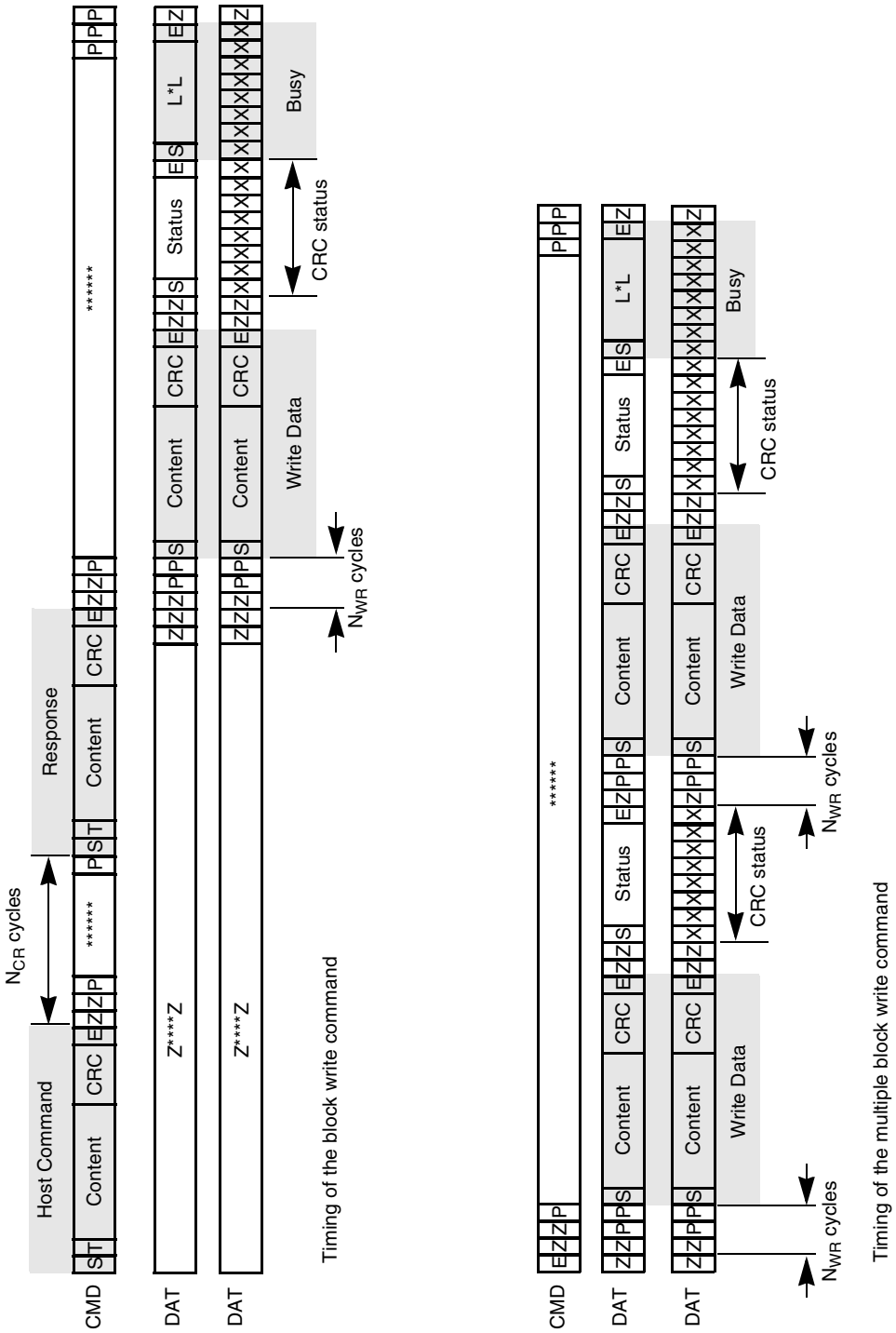


Figure 21. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 22 shows the different scenarios on the bus.

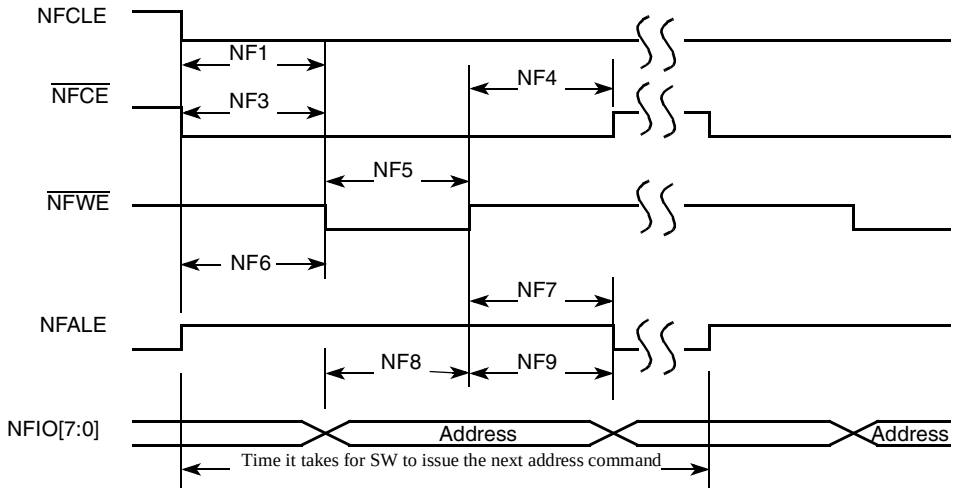


Figure 26. Address Latch Cycle Timing Diagram

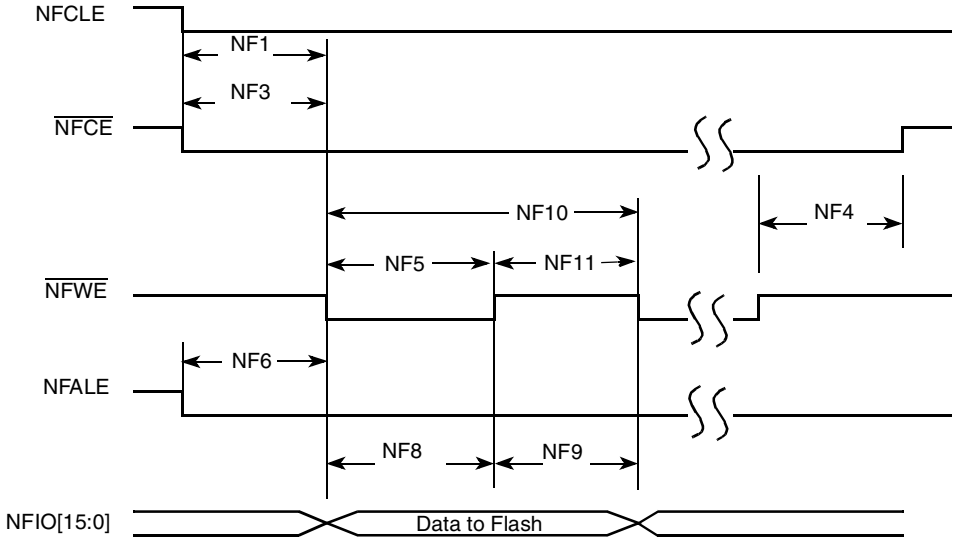


Figure 27. Write Data Latch Timing Diagram

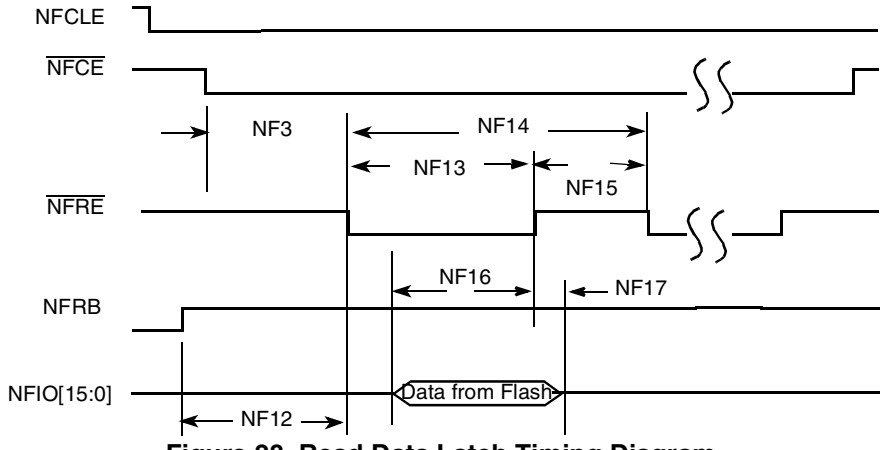


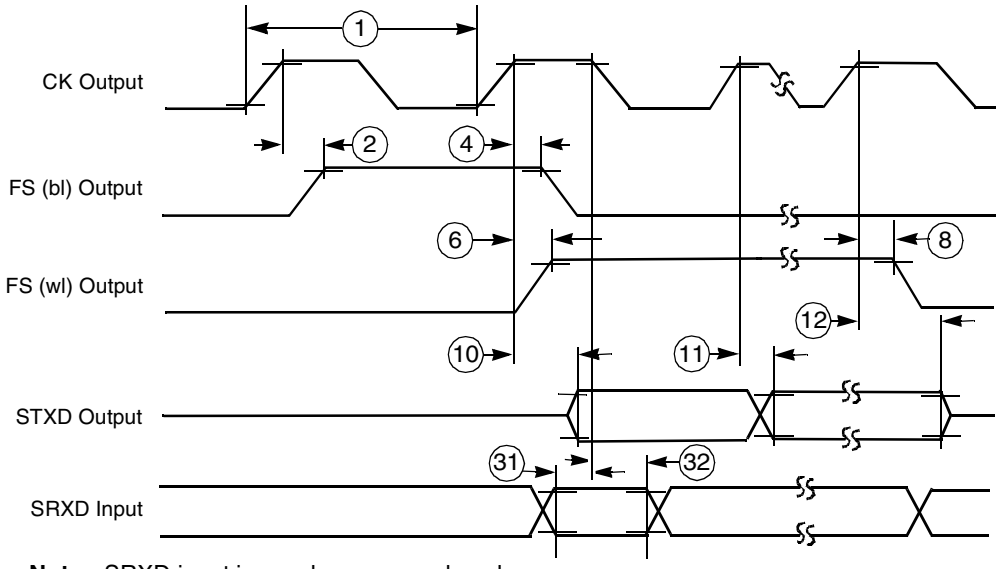
Figure 28. Read Data Latch Timing Diagram

3.15 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 34 through Figure 37.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.

The SSI can be connected to 4 set of ports, SAP, SSI1, SSI2 and SSI3.



Note: SRXD input in synchronous mode only.

Figure 34. SSI Transmitter Internal Clock Timing Diagram

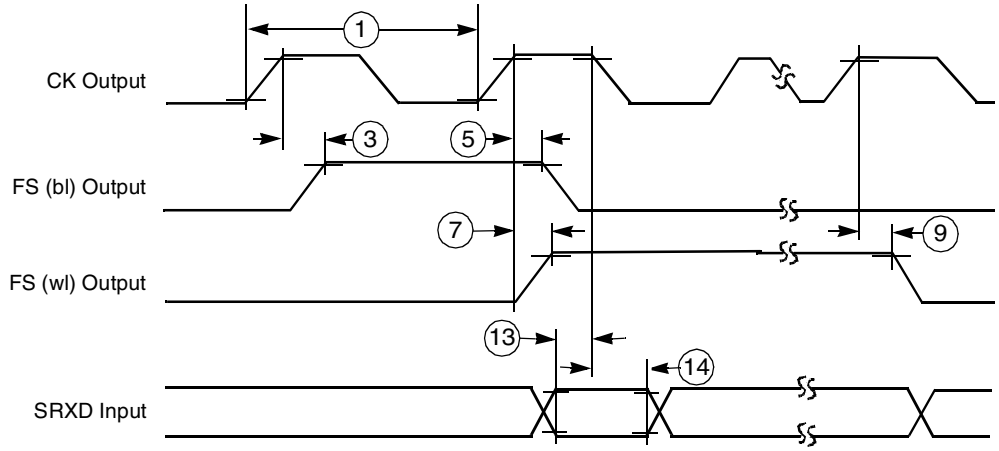
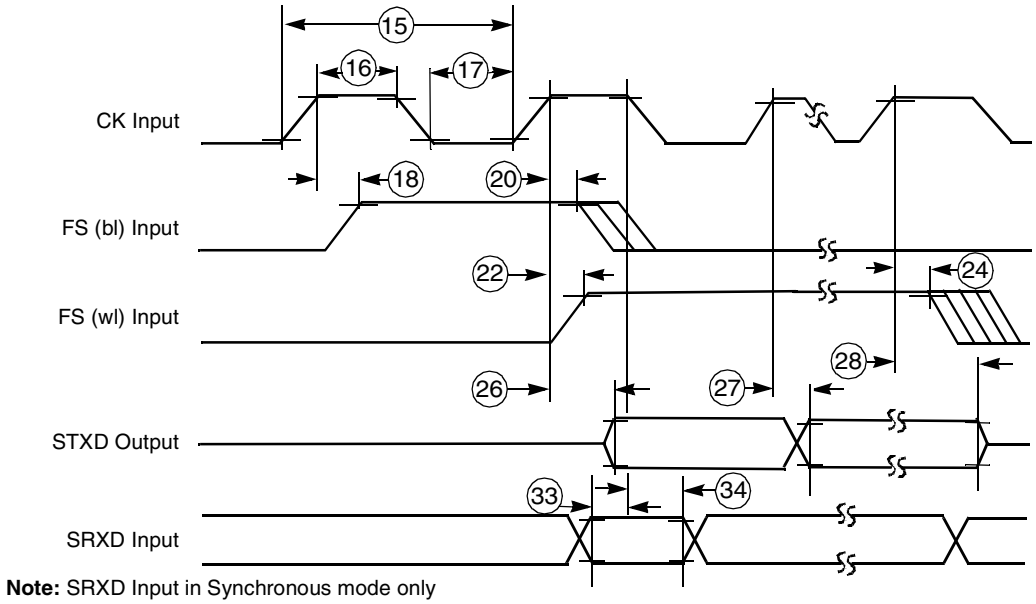


Figure 35. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 36. SSI Transmitter External Clock Timing Diagram

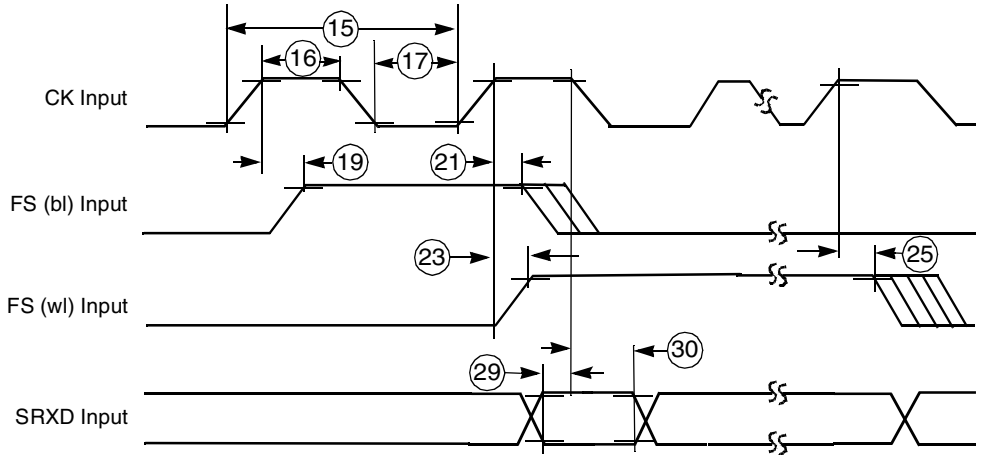


Figure 37. SSI Receiver External Clock Timing Diagram

control register PST. When the PST bit is set to a one, it means that a DS2502 is present; if the bit is set to a zero, then no device was found.

3.16.2 Write 0

The Write 0 function simply writes a zero bit to the DS2502. The sequence takes 117 us. The one-wire bus is held low for 100us.

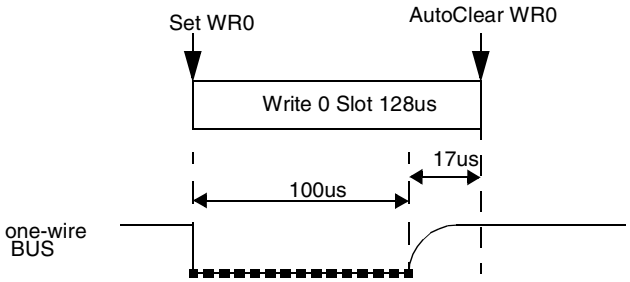


Figure 39. Write 0 Timing

The Write 0 pulse sequence is initiated when the WR0 control bit register is set. When the write is complete, the WR0 register will be auto cleared.

3.16.3 Write 1/Read Data

The Write 1 and Read timing is identical. The time slot is first driven low. According to the DS2502 documentation, the DS2502 has a delay circuit which is used to synchronize the DS2502 with the bus master (one-wire). This delay circuit is triggered by the falling edge of the data line and is used to decide when the DS2502 should sample the line. In the case of a write 1 or read 1, after a delay, a 1 will be transmitted / received. When a read 0 slot is issued, the delay circuit will hold the data line low to override the 1 generated by the bus master (one-wire).

For the Write 1 or Read, the control register WR1/RD is set and auto-cleared when the sequence has been completed. After a Read, the control register RDST bit is set to the value of the read.

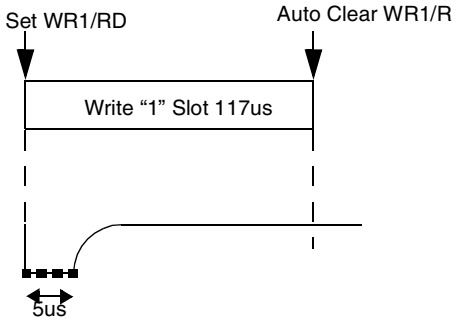


Figure 40. Write 1 Timing

3.18.1 EIM External Bus Timing Diagrams

The following timing diagrams show the timing of accesses to memory or a peripheral.

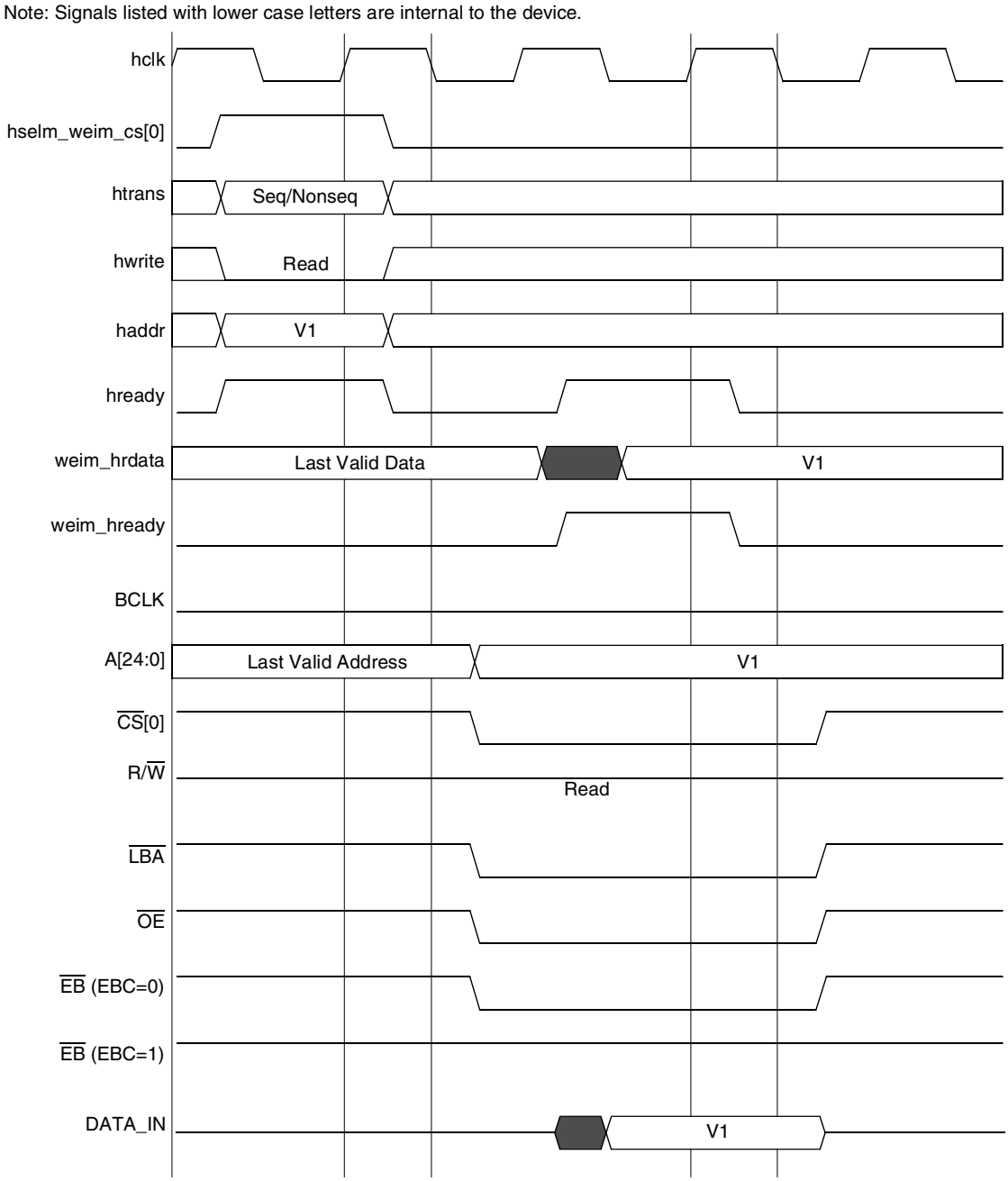


Figure 46. WSC = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

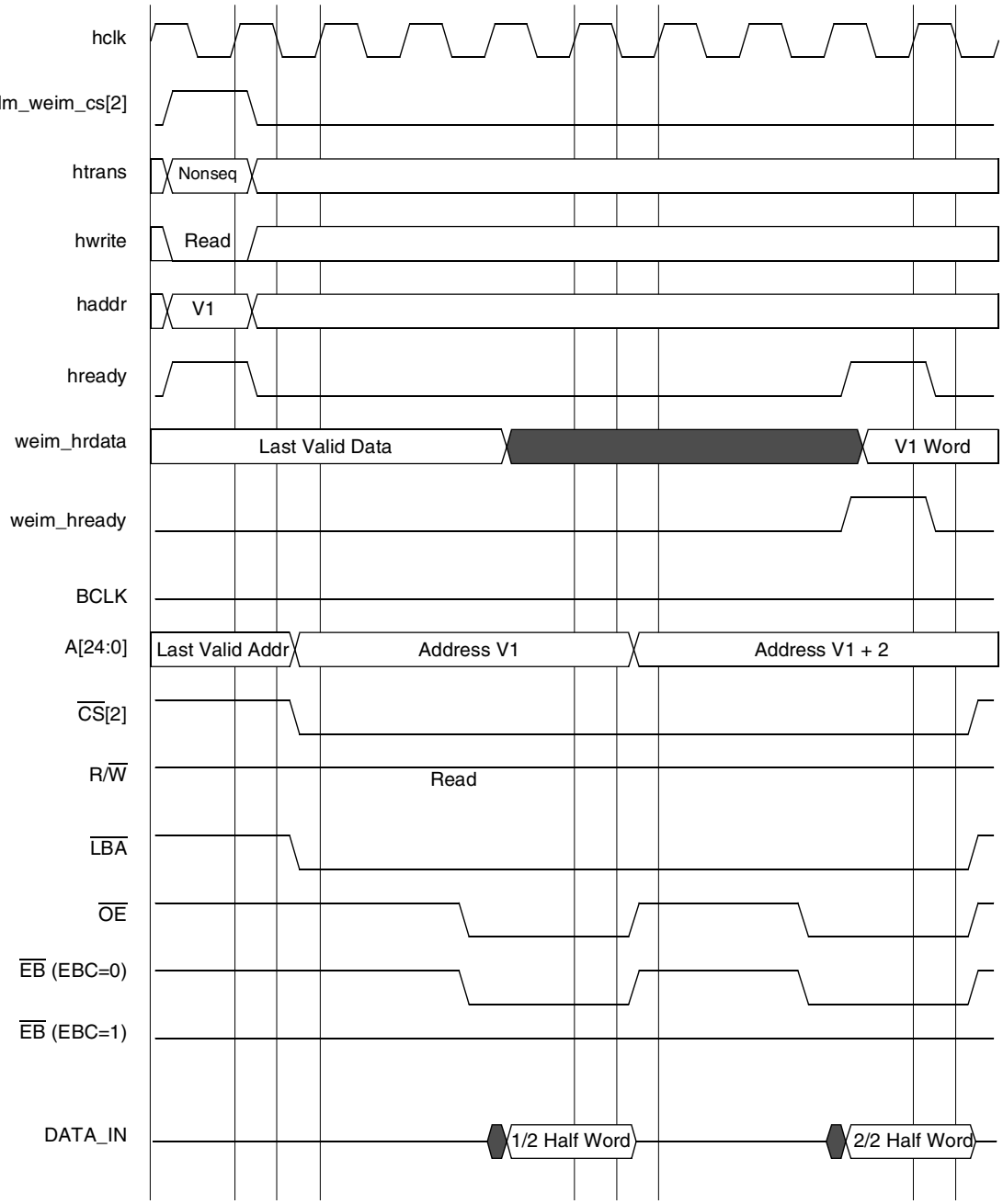


Figure 52. WSC = 3, OEA = 4, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

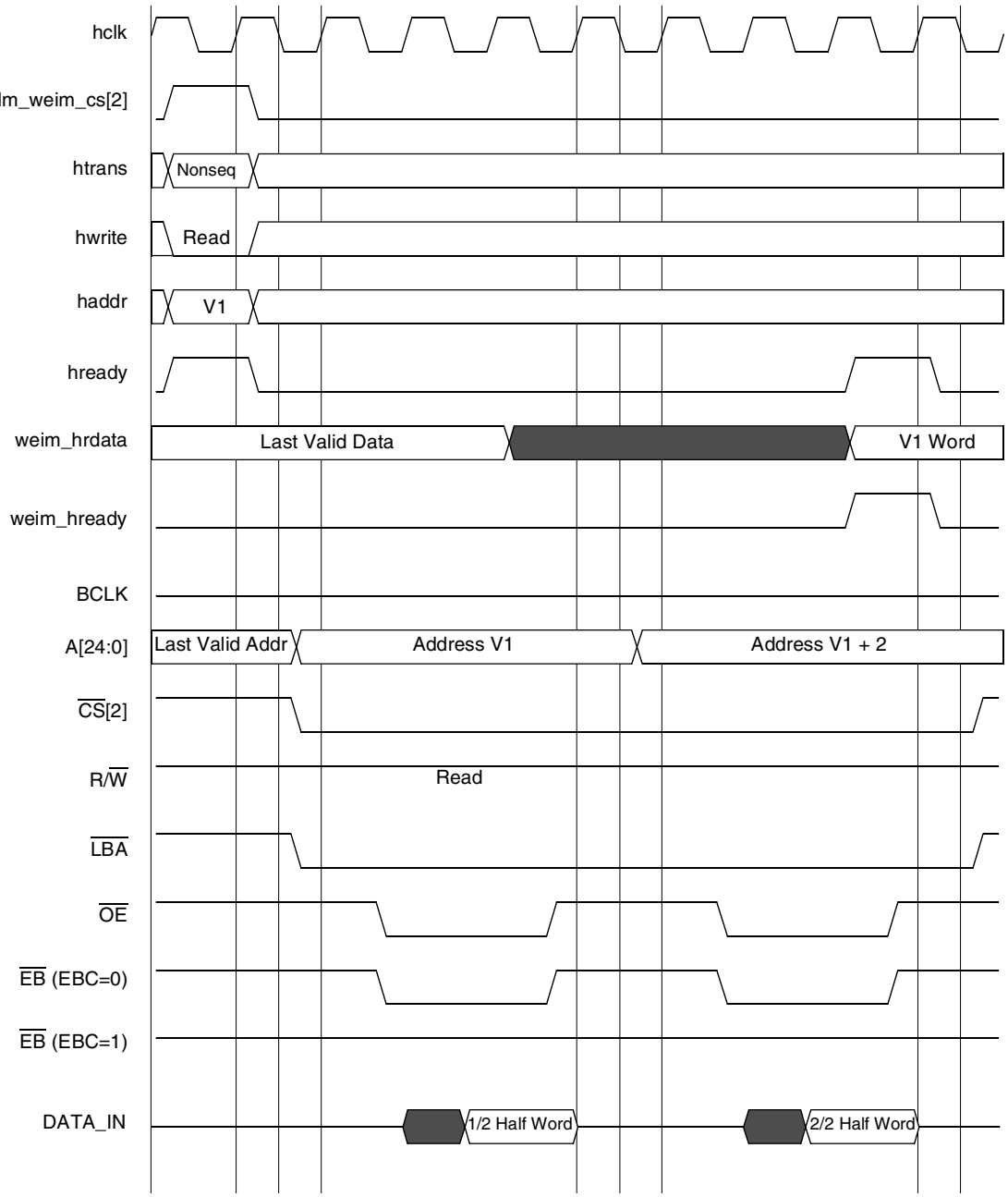


Figure 55. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

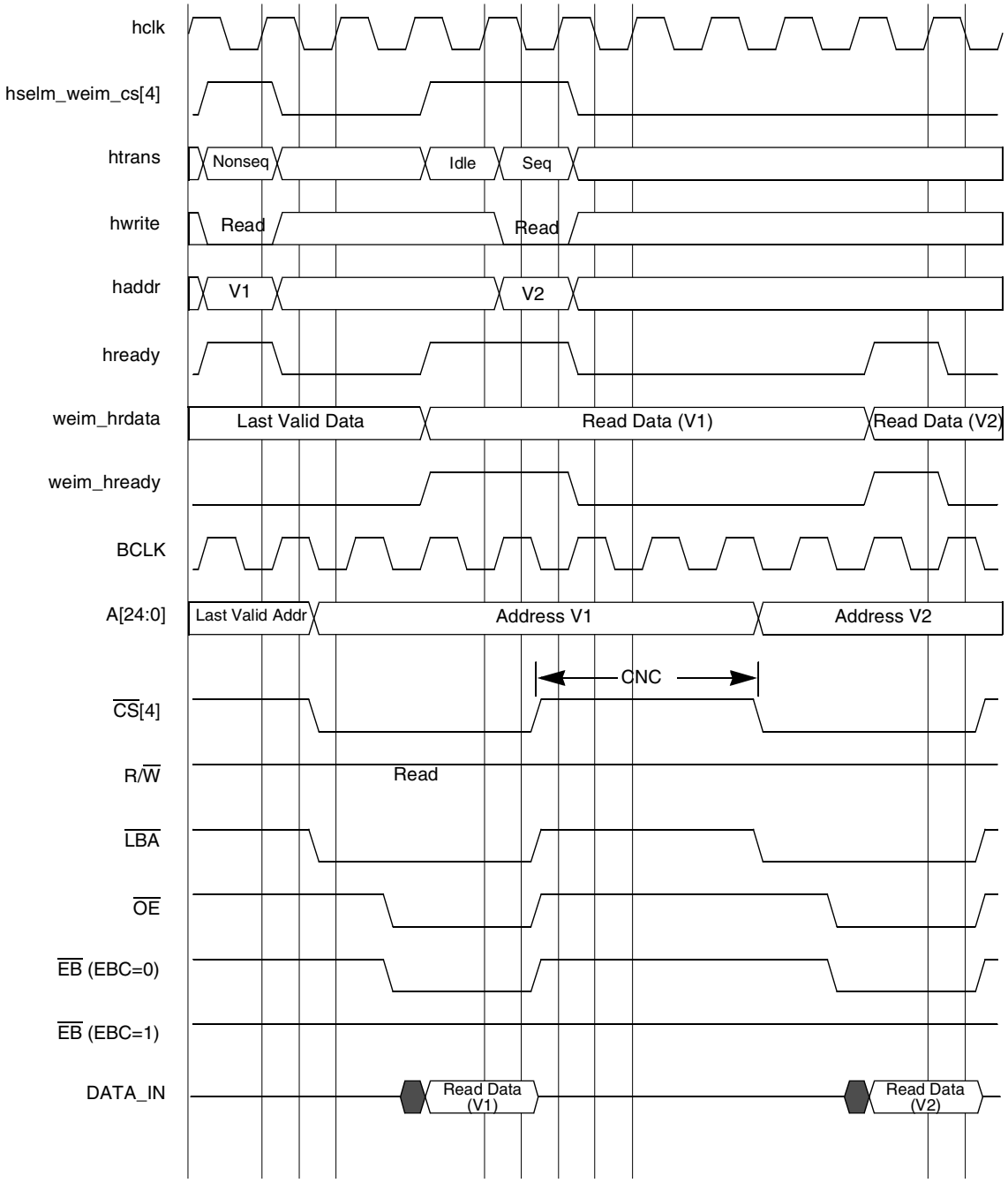


Figure 62. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

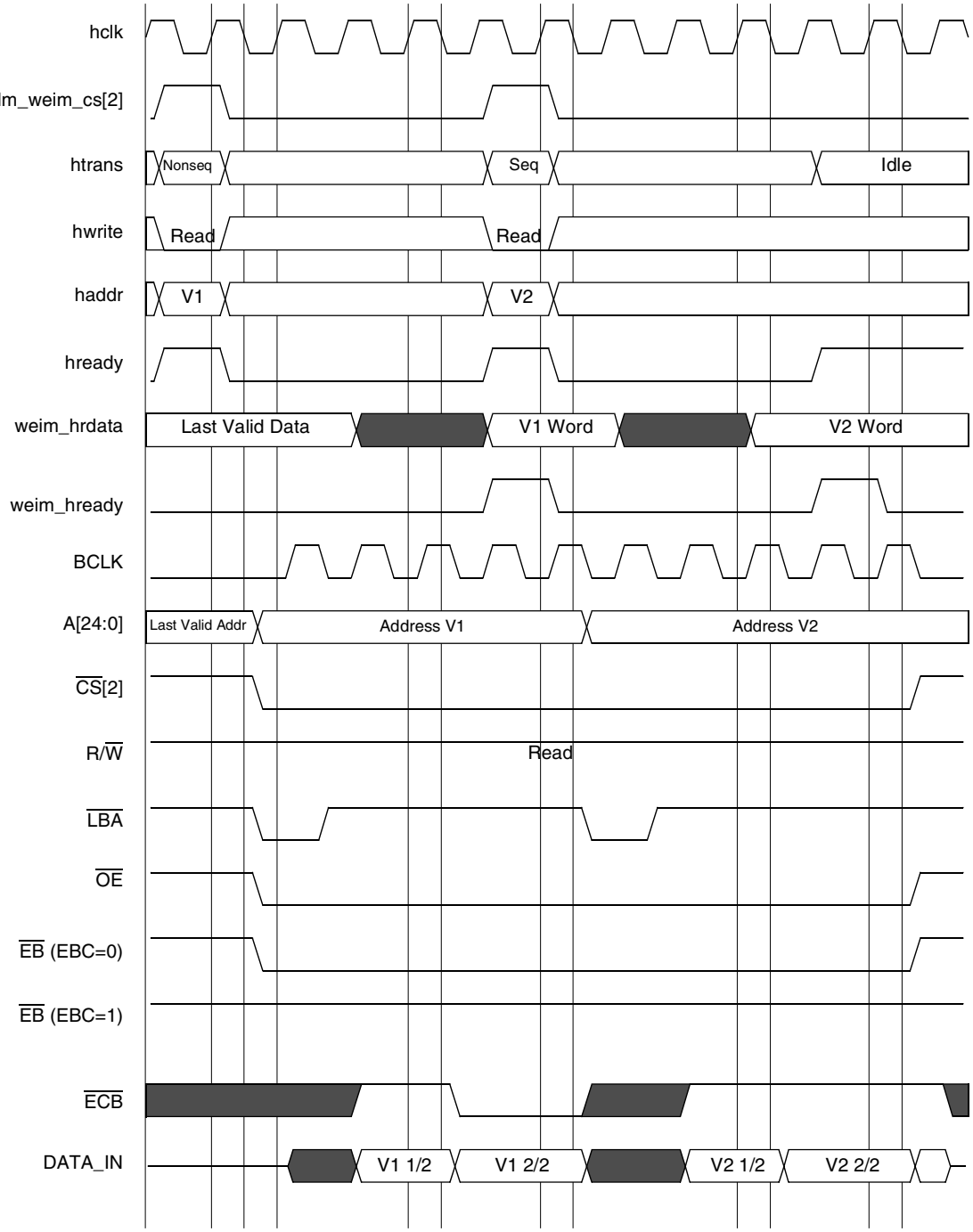


Figure 66. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

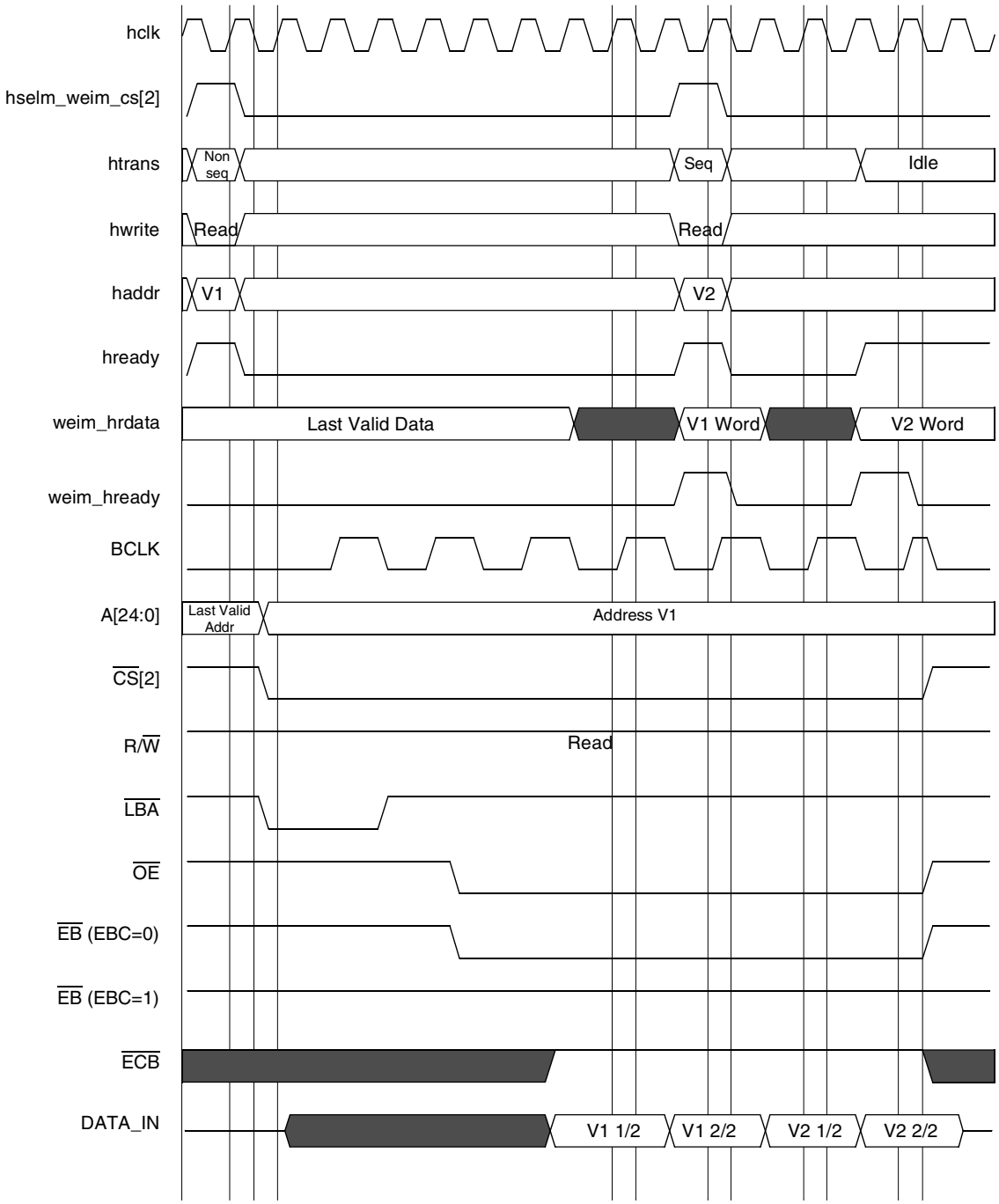


Figure 67. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF