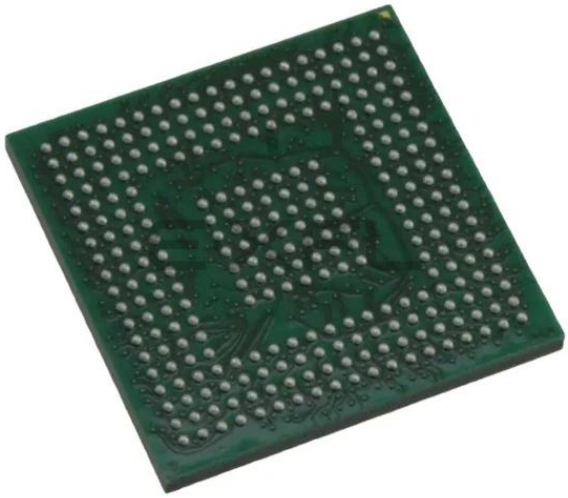

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx21scvm

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
PC_POE	PCMCIA Output Enable signal to enable voltage translation buffers and transceivers. This signal is multiplexed with NFCLE signal of NF.
$\overline{\text{PC\_RW}}$	PCMCIA Read Write output signal to control external transceiver direction. Asserted high for read access and negated low for write access. This signal is multiplexed with $\overline{\text{NFRE}}$ signal of NF.
PC_PWRON	PCMCIA input signal to indicate that the card power has been applied and stabilized.
CSPI	
CSPI1_MOSI	Master Out/Slave In signal
CSPI1_MISO	Master In/Slave Out signal
CSPI1_SS[2:0]	Slave Select (Selectable polarity) signal. CSPI1_SS2 is also multiplexed with USBG_RXDAT and CSPI1_SS1 is multiplexed with $\overline{\text{EXT\_DMAGRANT}}$.
CSPI1_SCLK	Serial Clock signal
CSPI1_$\overline{\text{RDY}}$	Serial Data Ready signal. Also multiplexed with $\overline{\text{EXT\_DMAREQ}}$.
CSPI2_MOSI	Master Out/Slave In signal. This signal is multiplexed with USBH2_TXDP signal of USB OTG.
CSPI2_MISO	Master In/Slave Out signal. This signal is multiplexed with USBH2_TXDM signal of USB OTG.
CSPI2_SS[2:0]	Slave Select (Selectable polarity) signals. These signals are multiplexed with USBH2_FS, USBH2_RXDP and USBH2_RXDM signal of USB OTG
CSPI2_SCLK	Serial Clock signal. This signal is multiplexed with $\overline{\text{USBH2\_OE}}$ signal of USB OTG
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to all 3 timers simultaneously. This signal is muxed with the Walk-up Guard Mode $\overline{\text{WKGD}}$ signal in the PLL, Clock, and Reset Controller module.
TOUT1 (or simply TOUT)	Timer Output signal from General Purpose Timer1 (GPT1). This signal is multiplexed with SYS_CLK1 and SYS_CLK2 signal of SSI1 and SSI2. The pin name of this signal is simply TOUT.
TOUT2	Timer Output signal from General Purpose Timer1 (GPT2). This signal is multiplexed with PWMO.
TOUT3	Timer Output signal from General Purpose Timer1 (GPT3). This signal is multiplexed with PWMO.
USB On-The-Go	
$\overline{\text{USB\_BYP}}$	USB Bypass input active low signal. This signal can only be used for USB function, not for GPIO.
USB_PWR	USB Power output signal
$\overline{\text{USB\_OC}}$	USB Over current input signal. This signal can only be used for USB function, not for GPIO.
USBG_RXDP	USB OTG Receive Data Plus input signal. This signal is muxed with SLCDC1_DAT15.
USBG_RXDM	USB OTG Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT14.
USBG_TXDP	USB OTG Transmit Data Plus output signal. This signal is muxed with SLCDC1_DAT13.
USBG_TXDM	USB OTG Transmit Data Minus output signal. This signal is muxed with SLCDC1_DAT12.
USBG_RXDAT	USB OTG Transceiver differential data receive signal. Multiplexed with CSPI1_SS2.
$\overline{\text{USBG\_OE}}$	USB OTG Output Enable signal. This signal is muxed with SLCDC1_DAT11.
$\overline{\text{USBG\_ON}}$	USB OTG Transceiver ON output signal. This signal is muxed with SLCDC1_DAT9.
USBG_FS	USB OTG Full Speed output signal. This signal is multiplexed with external transceiver $\overline{\text{USBG\_TXR\_INT}}$ signal of USB OTG. This signal is muxed with SLCDC1_DAT10.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
KP_ROW[7:0]	Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2\_RTS}}$ and UART2_$\overline{\text{RXD}}$ signals respectively. Alternatively, KP_ROW7 and KP_ROW6 are available on the internal factory test signals TEST_WB0 and TEST_WB1 respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available.
Noisy Supply Pins	
NVDD	Noisy Supply for the I/O pins. There are six (6) I/O voltages, NVDD1 through NVDD6.
NVSS	Noisy Ground for the I/O pins
Supply Pins – Analog Modules	
VDDA	Supply for analog blocks
QVSS (internally connected to AVSS)	Quiet GND for analog blocks (QVSS and AVSS are synonymous)
Internal Power Supplies	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Quiet GND pins for silicon internal circuitry
QVDDX	Power supply pin for the ARM core. Externally connect directly to QVDD

3 Specifications

This section contains the electrical specifications and timing diagrams for the i.MX21S processor.

3.1 Maximum Ratings

Table 3 provides the maximum ratings.

CAUTION

Stresses beyond those listed under "Maximum Ratings," (Table 3) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "266 MHz Recommended Operating Range" (Table 4) is not implied. Exposure to maximum-rated conditions for extended periods may affect device reliability.

Table 3. Maximum Ratings

Ref. Num	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	$QVDD_{max}$, $QVDDX_{max}$	-0.3	2.1	V
		$NVDD_{max}$, $VDDA_{max}$	-0.3	3.3	V
2	Input Voltage Range	V_{Imax}	-0.3	VDD + 0.3[1]	V
3	Storage Temperature Range	$T_{storage}$	-55	150	°C

1. VDD is the supply voltage associated with the input. See *Signal Multiplexing Scheme* table in the reference manual.

3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 11. In this table, T_{ref} is a reference clock period after the predivider and T_{dck} is the output double clock period.

Table 11. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock frequency range	Vcc = 1.5V	16	–	320	MHz
Pre-divider output clock frequency range	Vcc = 1.5V	16	–	32	MHz
Double clock frequency range	Vcc = 1.5V	220	–	560	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Frequency lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	350	400	450	T_{ref}
Frequency lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	280	330	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	480	530	580	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	360	410	460	T_{ref}
Frequency jitter (p-p)	–	–	0.02	0.03	$2 \bullet T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.7V	–	1.0	1.5	ns
Power dissipation	FOL mode, integer MF, f_{dck} = 560 MHz, Vcc = 1.5V	–	1.5	–	mW (Avg)

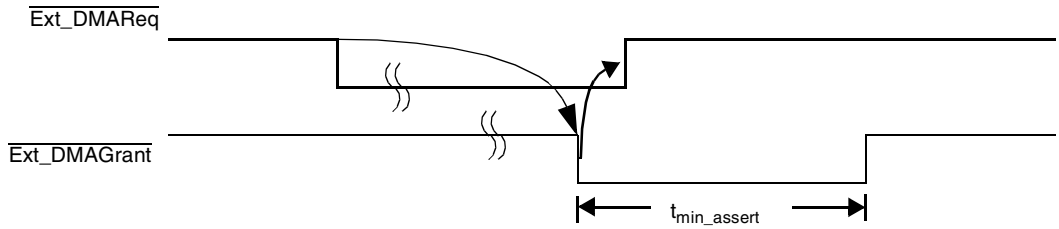
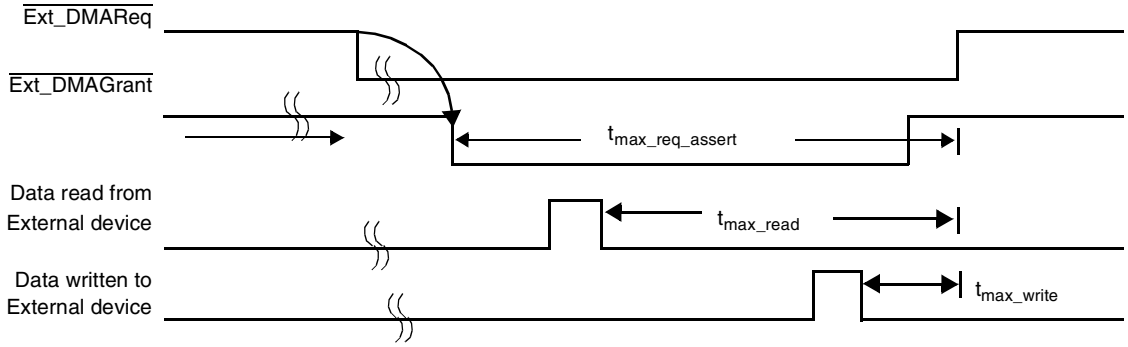


Figure 4. Assertion of DMA External Grant Signal

Figure 5 shows the safe maximum time for which External DMA request can be kept asserted, after sensing grant signal active such that a new burst is not initiated.



NOTE: Assuming in worst case the data is read/written from/to External device as per the above waveform.

Figure 5. Safe Maximum Timings for External Request De-Assertion

Table 13. DMA External Request and Grant Timing Parameters

Parameter	Description	3.0 V		1.8 V		Unit
		WCS	BCS	WCS	BCS	
t_{min_assert}	Minimum assertion time of External Grant signal	8 hclk + 8.6	8 hclk + 2.74	8 hclk + 7.17	8 hclk + 3.25	ns
$t_{max\_req\_assert}$	Maximum External request assertion time after assertion of Grant signal	9 hclk - 20.66	9 hclk - 6.7	9 hclk - 17.96	9 hclk - 8.16	ns
t_{max_read}	Maximum External request assertion time after first read completion	8 hclk - 6.21	8 hclk - 0.77	8 hclk - 5.84	8 hclk - 0.66	ns
t_{max_write}	Maximum External request assertion time after completion of first write	3 hclk - 15.87	3 hclk - 8.83	3 hclk - 15.9	3 hclk - 9.12	ns

3.8 CSPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the CSPI1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI 1 Sample Period Control Register (PERIODREG1) and the SPI 2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either CSPI1 or CSPI2. When the CSPI1 module is configured as a slave, the user can configure the SPI 1 Control Register (CONTROLREG1) to match the external CSPI master's timing. In this configuration, $\overline{SS}$

3.11.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 18. The symbols for Figure 18 through Figure 22 are defined in Table 22.

Table 22. State Signal Parameters for Figure 18 through Figure 22

Card Active		Host Active	
Symbol	**Definition**	**Symbol**	**Definition**
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

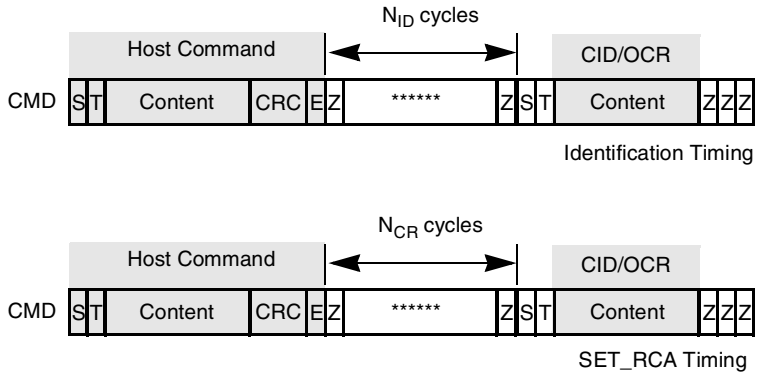


Figure 18. Timing Diagrams at Identification Mode

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in Figure 19, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC}.

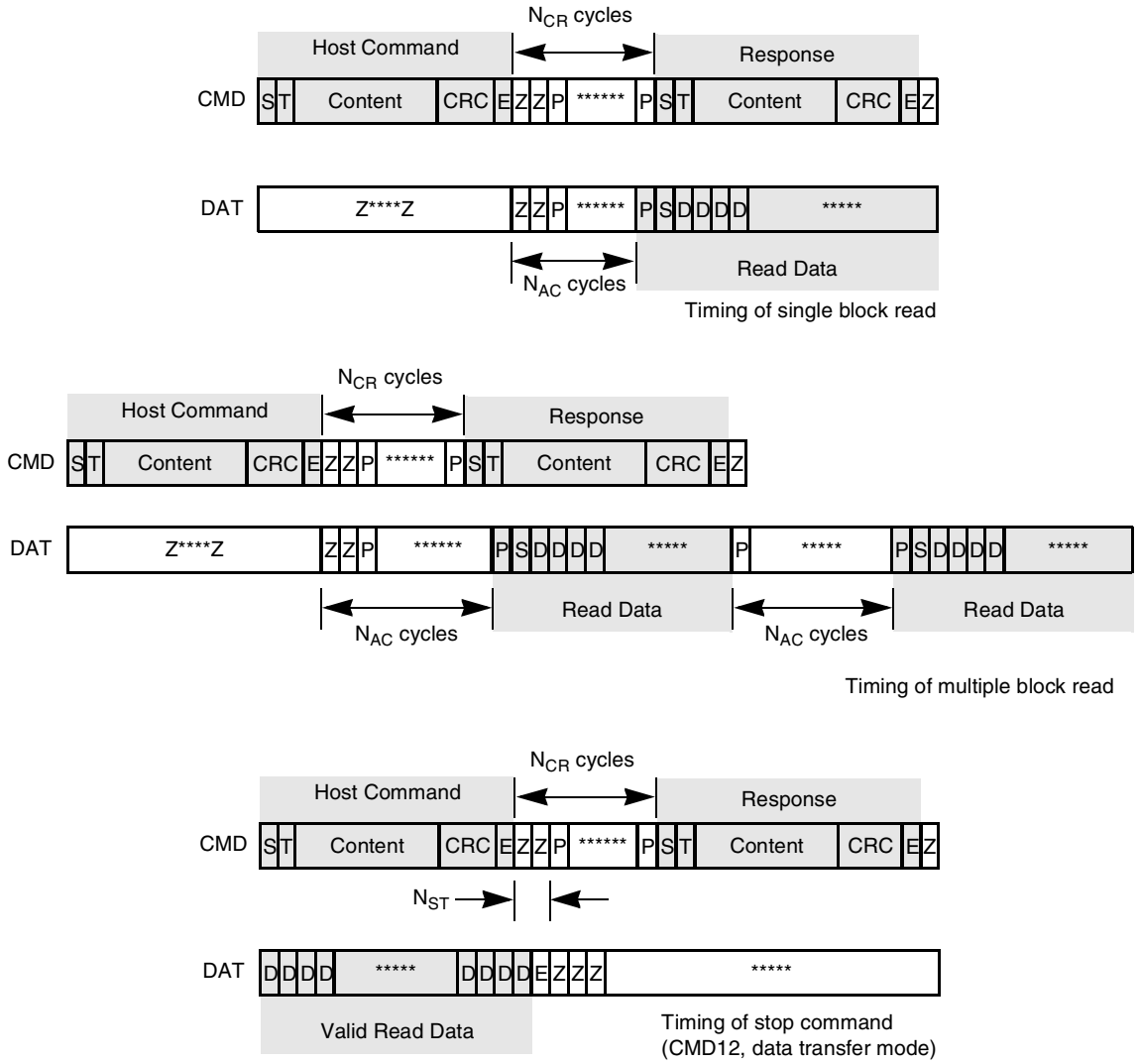


Figure 20. Timing Diagrams at Data Read

Figure 21 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

Table 23. Timing Values for Figure 18 through Figure 22 (Continued)

Parameter	Symbol	Minimum	Maximum	Unit
Command read cycle	NRC	8	–	Clock cycles
Command-command cycle	NCC	8	–	Clock cycles
Command write cycle	NWR	2	–	Clock cycles
Stop transmission cycle	NST	2	2	Clock cycles
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]				

3.11.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the *Interrupt Period* during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

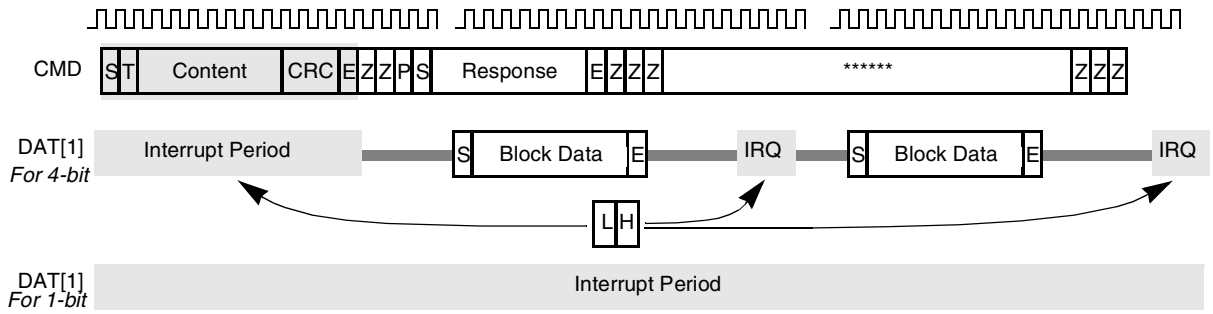


Figure 23. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

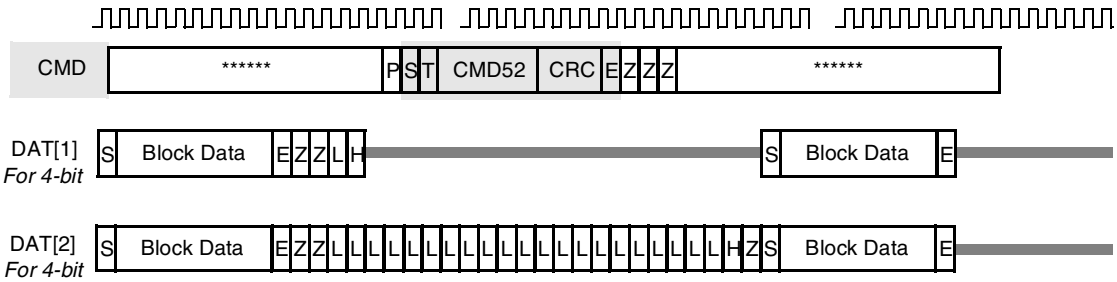


Figure 24. SDIO ReadWait Timing Diagram

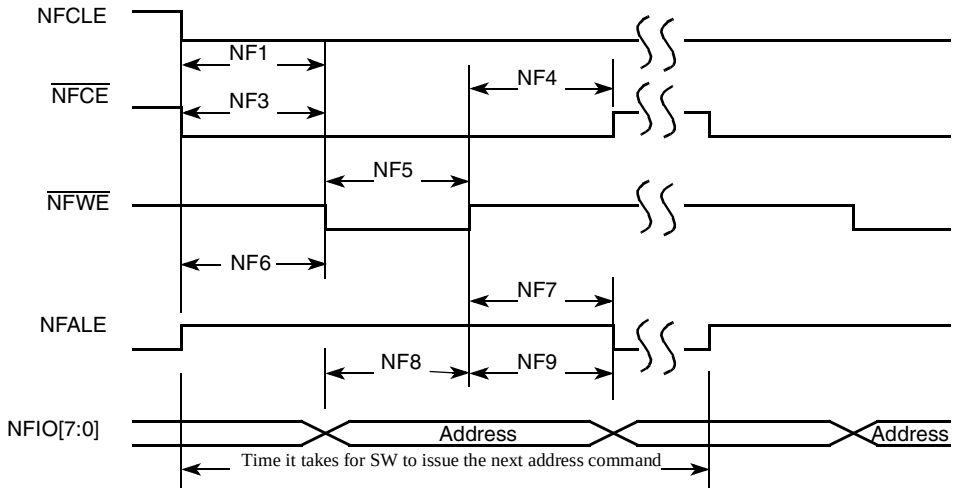


Figure 26. Address Latch Cycle Timing Diagram

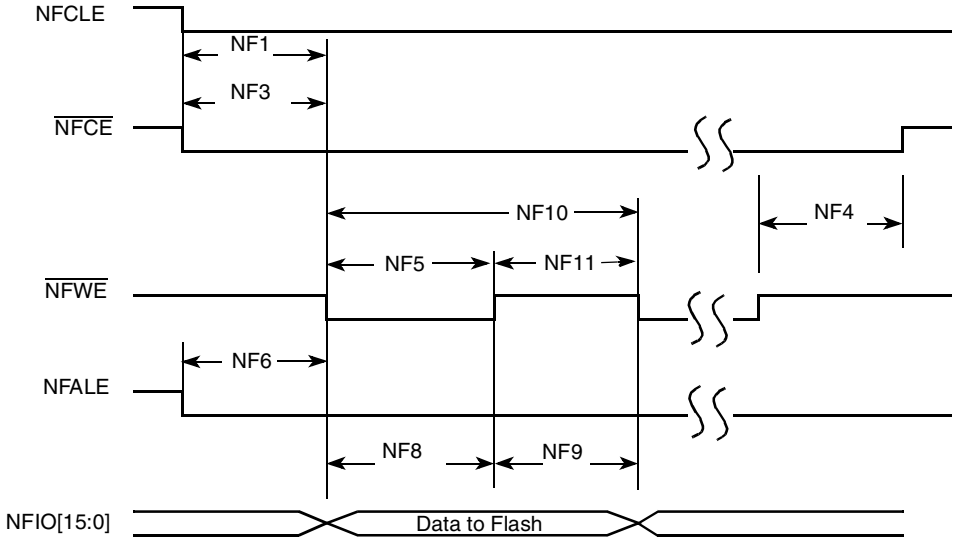


Figure 27. Write Data Latch Timing Diagram

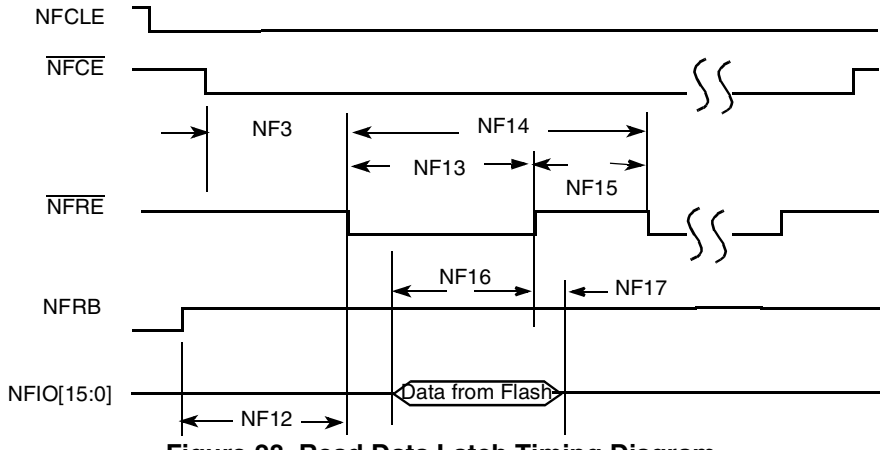


Figure 28. Read Data Latch Timing Diagram

3.13 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

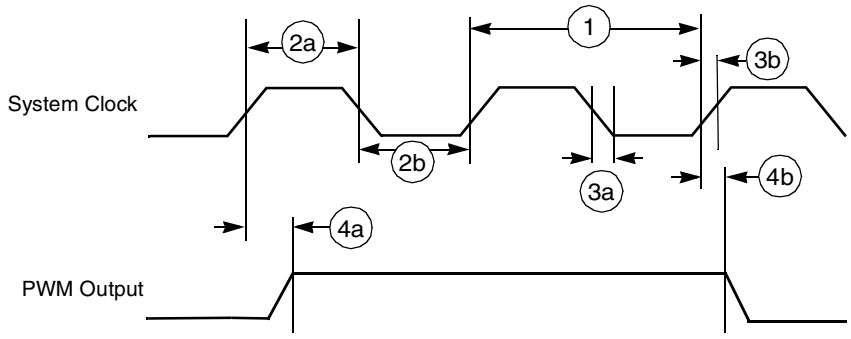


Figure 29. PWM Output Timing Diagram

Table 25. PWM Output Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	45	0	45	MHz
2a	Clock high time[1]	12.29	–	12.29	–	ns
2b	Clock low time[1]	9.91	–	9.91	–	ns
3a	Clock fall time[1]	–	0.5	–	0.5	ns
3b	Clock rise time[1]	–	0.5	–	0.5	ns
4a	Output delay time[1]	9.37	–	3.61	–	ns
4b	Output setup time[1]	8.71	–	3.03	–	ns

1. C_L of PWMO = TBD

Table 29. SSI to SAP Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SAP Ports)						
1	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-3.30	-1.16	-2.98	-1.10	ns
3	(Rx) CK high to FS (bl) high	-3.93	-1.34	-4.18	-1.43	ns
4	(Tx) CK high to FS (bl) low	-3.30	-1.16	-2.98	-1.10	ns
5	(Rx) CK high to FS (bl) low	-3.93	-1.34	-4.18	-1.43	ns
6	(Tx) CK high to FS (wl) high	-3.30	-1.16	-2.98	-1.10	ns
7	(Rx) CK high to FS (wl) high	-3.93	-1.34	-4.18	-1.43	ns
8	(Tx) CK high to FS (wl) low	-3.30	-1.16	-2.98	-1.10	ns
9	(Rx) CK high to FS (wl) low	-3.93	-1.34	-4.18	-1.43	ns
10	(Tx) CK high to STXD valid from high impedance	-2.44	-0.60	-2.65	-0.98	ns
11a	(Tx) CK high to STXD high	-2.44	-0.60	-2.65	-0.98	ns
11b	(Tx) CK high to STXD low	-2.44	-0.60	-2.65	-0.98	ns
12	(Tx) CK high to STXD high impedance	-2.67	-0.99	-2.65	-0.98	ns
13	SRXD setup time before (Rx) CK low	23.68	–	22.09	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SAP Ports)						
15	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.24	19.50	7.16	8.65	ns
19	(Rx) CK high to FS (bl) high	10.89	21.27	7.63	9.12	ns
20	(Tx) CK high to FS (bl) low	10.24	19.50	7.16	8.65	ns
21	(Rx) CK high to FS (bl) low	10.89	21.27	7.63	9.12	ns
22	(Tx) CK high to FS (wl) high	10.24	19.50	7.16	8.65	ns
23	(Rx) CK high to FS (wl) high	10.89	21.27	7.63	9.12	ns
24	(Tx) CK high to FS (wl) low	10.24	19.50	7.16	8.65	ns
25	(Rx) CK high to FS (wl) low	10.89	21.27	7.63	9.12	ns
26	(Tx) CK high to STXD valid from high impedance	12.08	19.36	7.71	9.20	ns
27a	(Tx) CK high to STXD high	10.80	19.36	7.71	9.20	ns
27b	(Tx) CK high to STXD low	10.80	19.36	7.71	9.20	ns
28	(Tx) CK high to STXD high impedance	12.08	19.36	7.71	9.20	ns
29	SRXD setup time before (Rx) CK low	0.37	–	0.42	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns

Table 30. SSI to SSI1 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
20	(Tx) CK high to FS (bl) low	10.22	17.63	8.82	16.24	ns
21	(Rx) CK high to FS (bl) low	10.79	19.67	9.39	18.28	ns
22	(Tx) CK high to FS (wl) high	10.22	17.63	8.82	16.24	ns
23	(Rx) CK high to FS (wl) high	10.79	19.67	9.39	18.28	ns
24	(Tx) CK high to FS (wl) low	10.22	17.63	8.82	16.24	ns
25	(Rx) CK high to FS (wl) low	10.79	19.67	9.39	18.28	ns
26	(Tx) CK high to STXD valid from high impedance	10.05	15.75	8.66	14.36	ns
27a	(Tx) CK high to STXD high	10.00	15.63	8.61	14.24	ns
27b	(Tx) CK high to STXD low	10.00	15.63	8.61	14.24	ns
28	(Tx) CK high to STXD high impedance	10.05	15.75	8.66	14.36	ns
29	SRXD setup time before (Rx) CK low	0.78	–	0.47	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI1 Ports)						
31	SRXD setup before (Tx) CK falling	19.90	–	19.90	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI1 Ports)						
33	SRXD setup before (Tx) CK falling	2.59	–	2.28	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 31. SSI to SSI2 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI2 Ports)						
1	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	0.01	0.15	0.01	0.15	ns
3	(Rx) CK high to FS (bl) high	-0.21	0.05	-0.21	0.05	ns
4	(Tx) CK high to FS (bl) low	0.01	0.15	0.01	0.15	ns
5	(Rx) CK high to FS (bl) low	-0.21	0.05	-0.21	0.05	ns
6	(Tx) CK high to FS (wl) high	0.01	0.15	0.01	0.15	ns
7	(Rx) CK high to FS (wl) high	-0.21	0.05	-0.21	0.05	ns
8	(Tx) CK high to FS (wl) low	0.01	0.15	0.01	0.15	ns
9	(Rx) CK high to FS (wl) low	-0.21	0.05	-0.21	0.05	ns
10	(Tx) CK high to STXD valid from high impedance	0.34	0.72	0.34	0.72	ns

Table 31. SSI to SSI2 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
11a	(Tx) CK high to STXD high	0.34	0.72	0.34	0.72	ns
11b	(Tx) CK high to STXD low	0.34	0.72	0.34	0.72	ns
12	(Tx) CK high to STXD high impedance	0.34	0.48	0.34	0.48	ns
13	SRXD setup time before (Rx) CK low	21.50	–	21.50	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI2 Ports)						
15	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.40	17.37	8.67	15.88	ns
19	(Rx) CK high to FS (bl) high	11.00	19.70	9.28	18.21	ns
20	(Tx) CK high to FS (bl) low	10.40	17.37	8.67	15.88	ns
21	(Rx) CK high to FS (bl) low	11.00	19.70	9.28	18.21	ns
22	(Tx) CK high to FS (wl) high	10.40	17.37	8.67	15.88	ns
23	(Rx) CK high to FS (wl) high	11.00	19.70	9.28	18.21	ns
24	(Tx) CK high to FS (wl) low	10.40	17.37	8.67	15.88	ns
25	(Rx) CK high to FS (wl) low	11.00	19.70	9.28	18.21	ns
26	(Tx) CK high to STXD valid from high impedance	9.59	17.08	7.86	15.59	ns
27a	(Tx) CK high to STXD high	9.59	17.08	7.86	15.59	ns
27b	(Tx) CK high to STXD low	9.59	17.08	7.86	15.59	ns
28	(Tx) CK high to STXD high impedance	9.59	16.84	7.86	15.35	ns
29	SRXD setup time before (Rx) CK low	2.52	–	2.52	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI2 Ports)						
31	SRXD setup before (Tx) CK falling	20.78	–	20.78	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI2 Ports)						
33	SRXD setup before (Tx) CK falling	4.42	–	4.42	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

3.17 USB On-The-Go

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, but because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

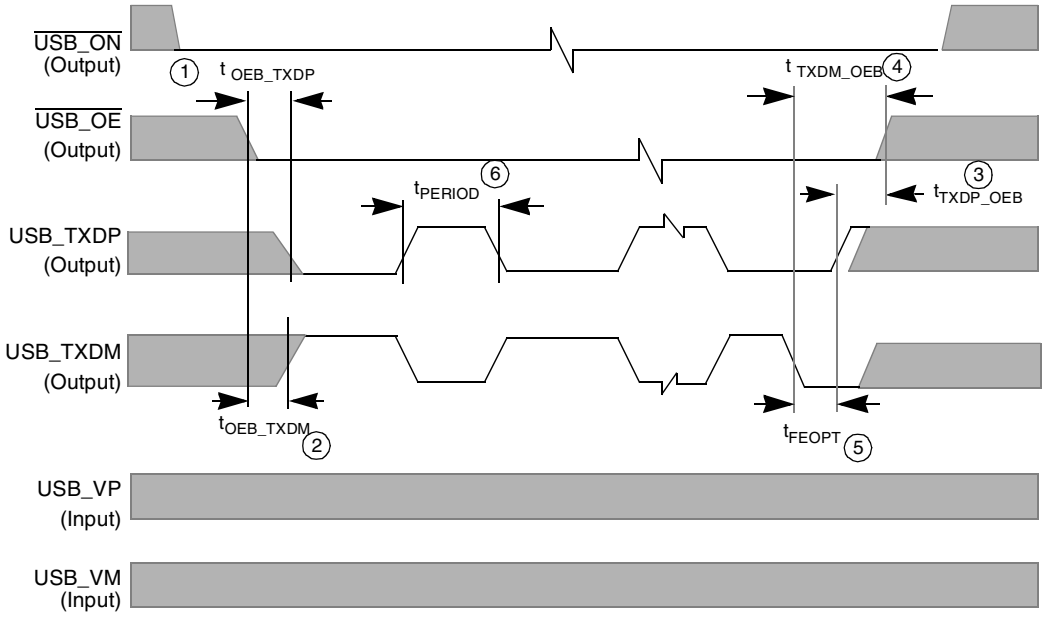


Figure 42. USB Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 35. USB Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{OEB_TXDP}; $\overline{USBD\_OE}$ active to USBD_TXDP low	83.14	83.47	ns
2	t_{OEB_TXDM}; $\overline{USBD\_OE}$ active to USBD_TXDM high	81.55	81.98	ns
3	t_{TXDP_OEB}; USBD_TXDP high to $\overline{USBD\_OE}$ deactivated	83.54	83.8	ns
4	t_{TXDM_OEB}; USBD_TXDM low to $\overline{USBD\_OE}$ deactivated (includes SE0)	248.9	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160	175	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

Note: Signals listed with lower case letters are internal to the device.

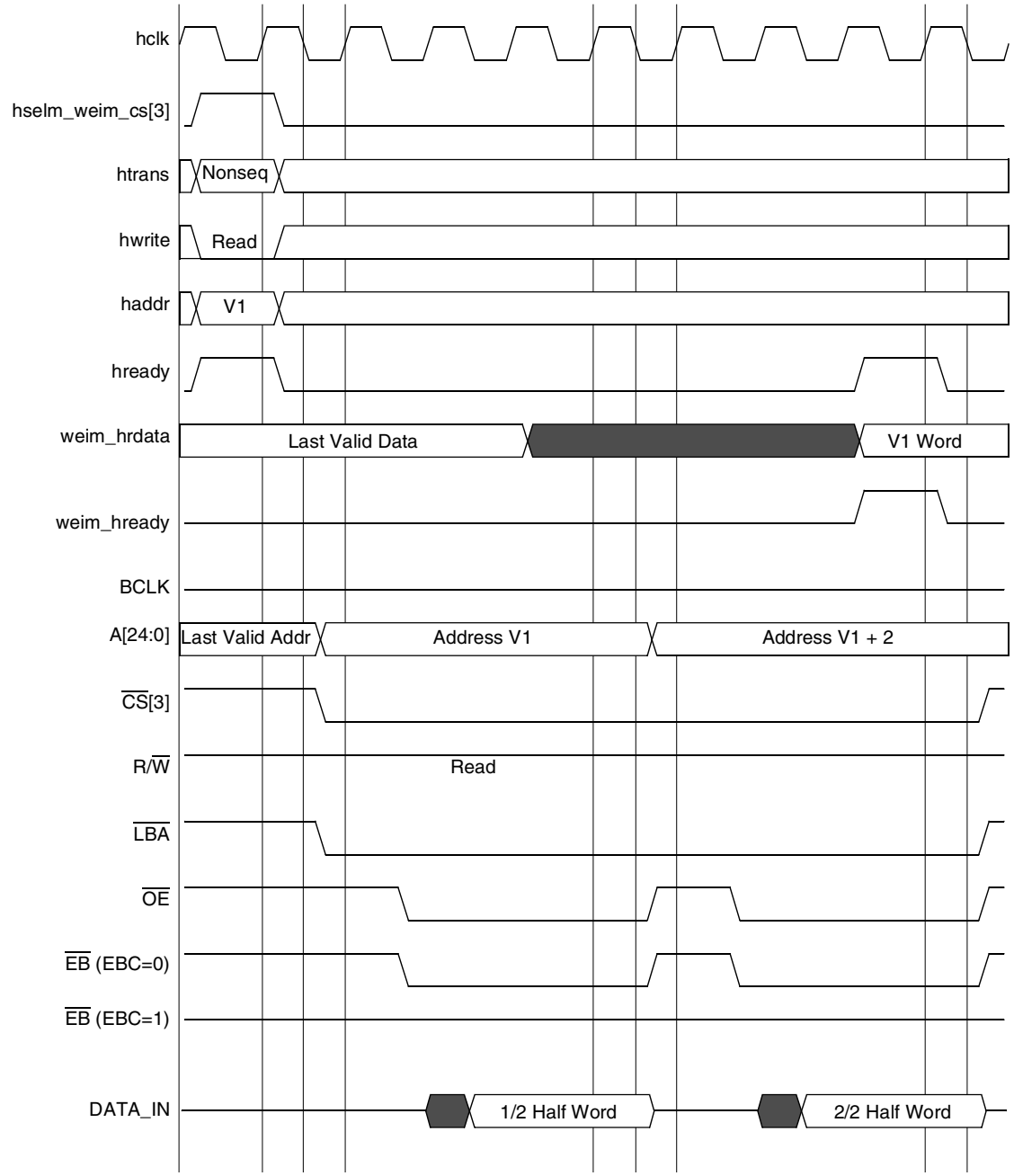


Figure 50. WSC = 3, OEA = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

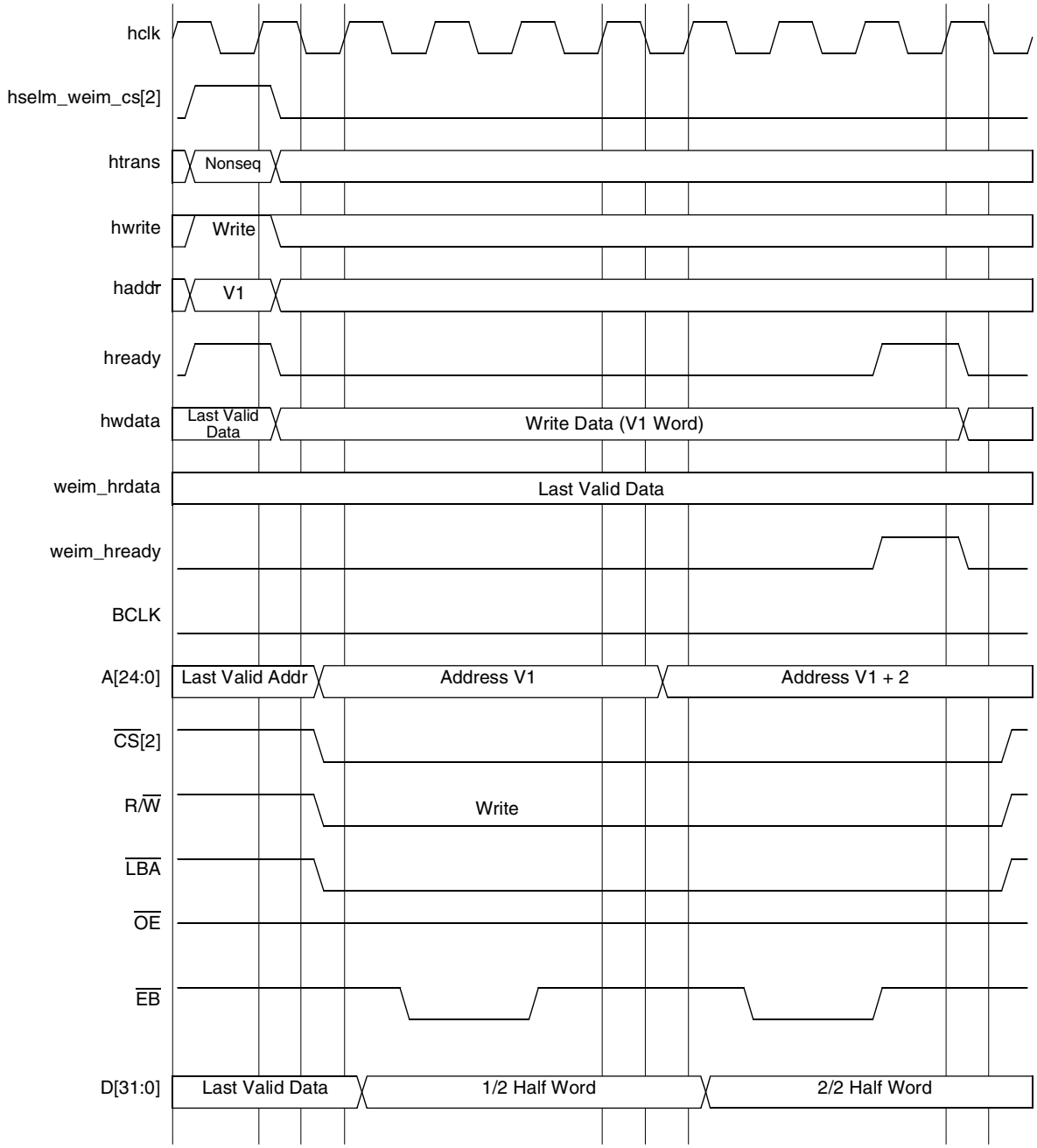


Figure 53. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

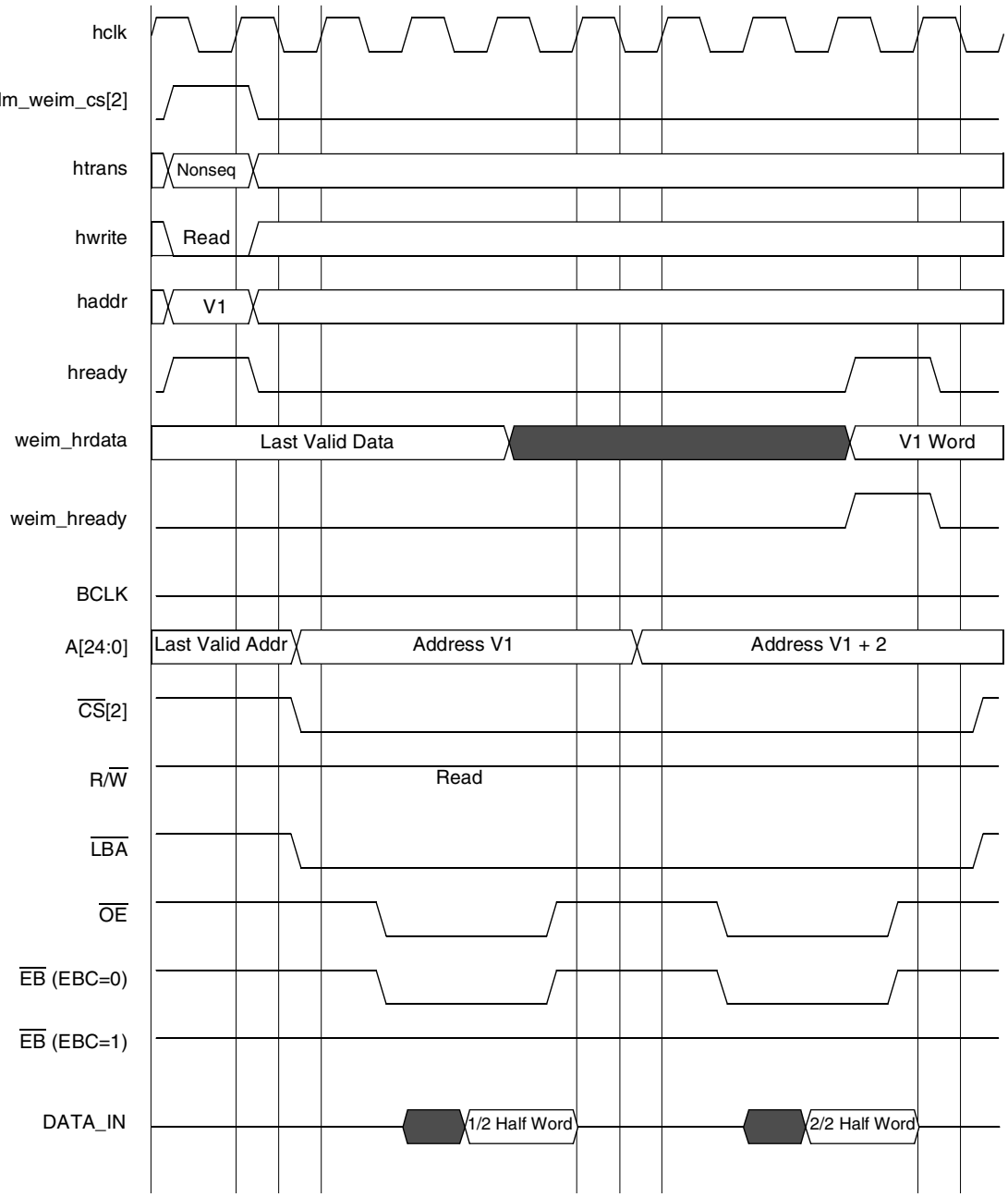


Figure 55. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

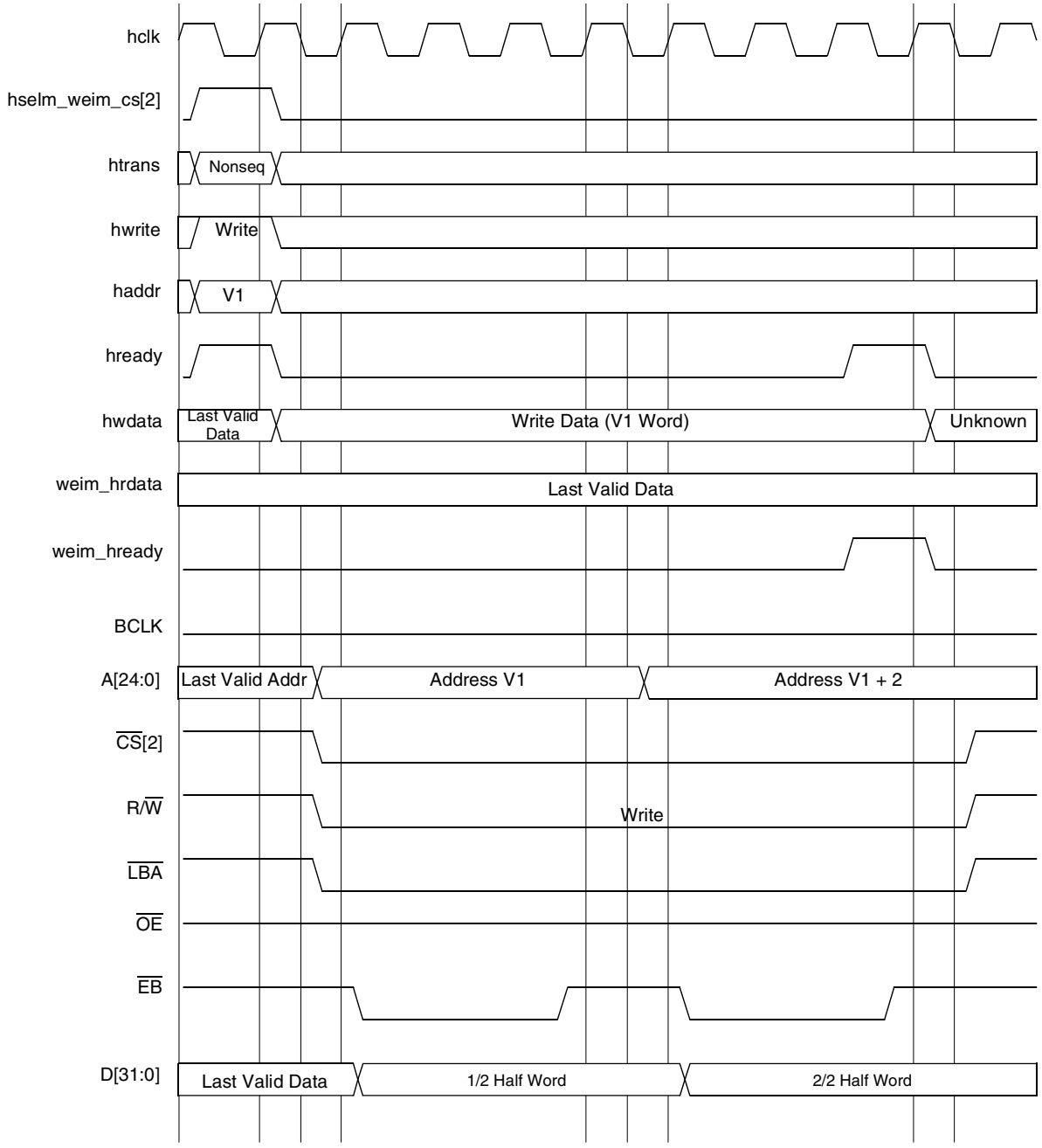


Figure 56. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

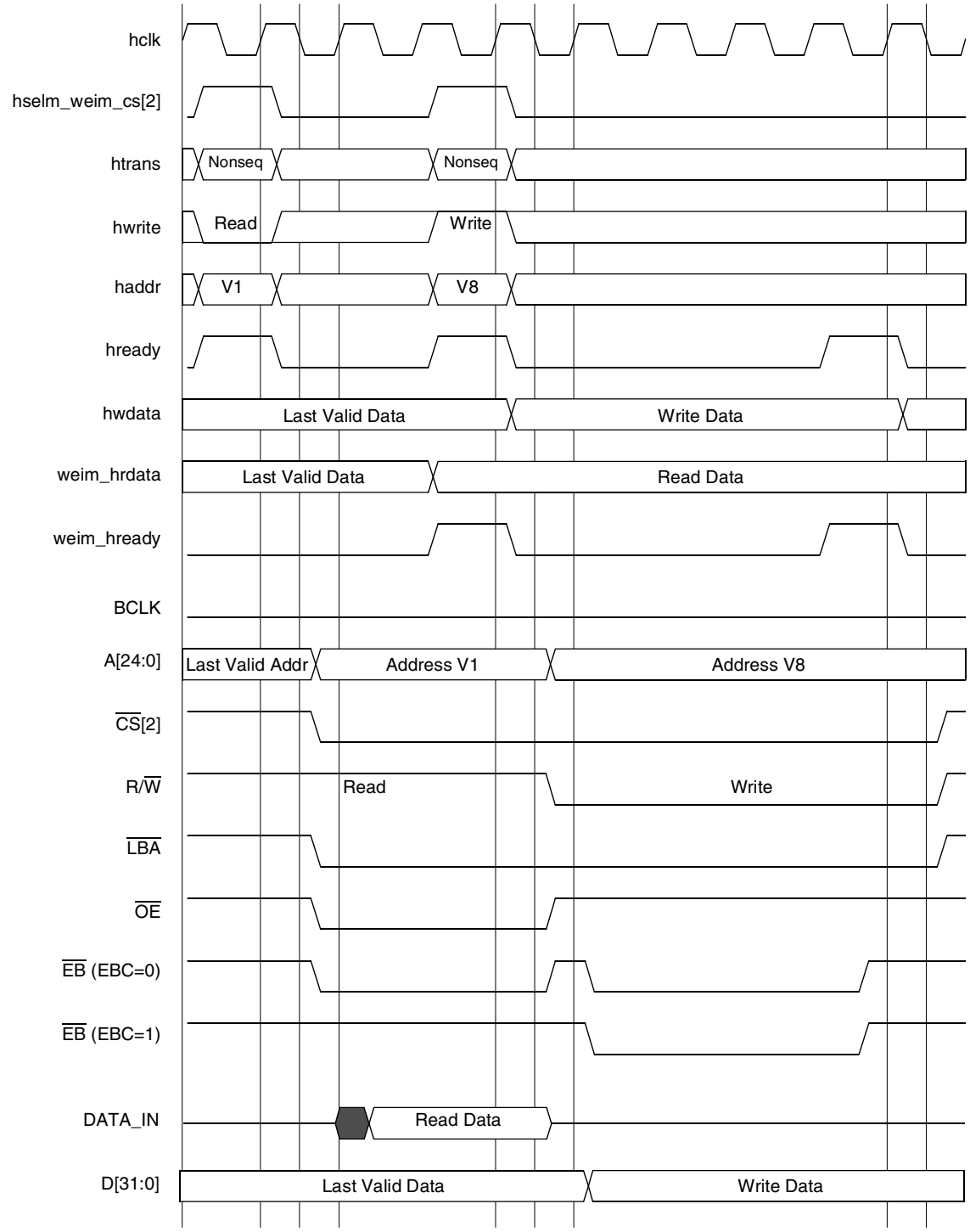


Figure 58. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

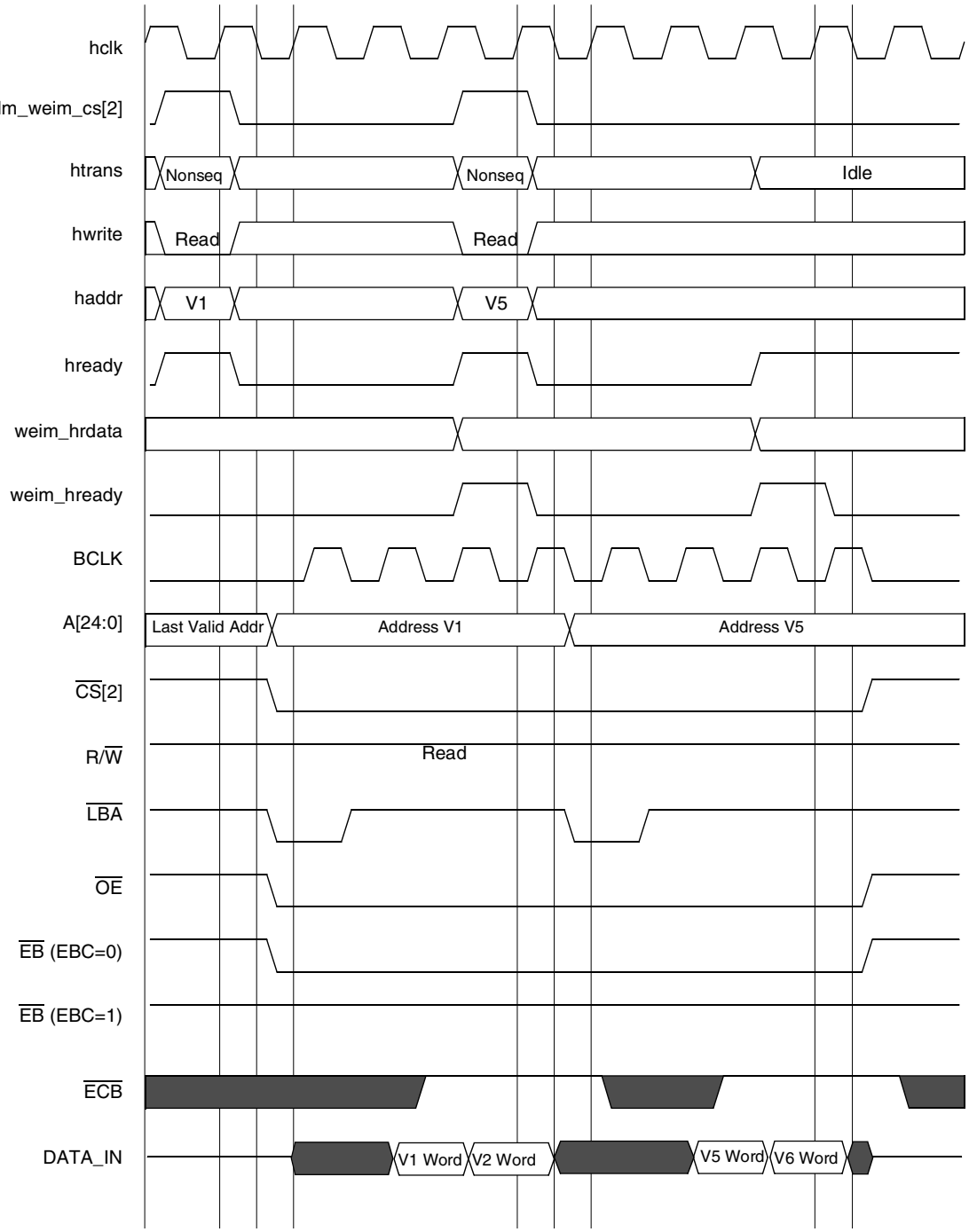
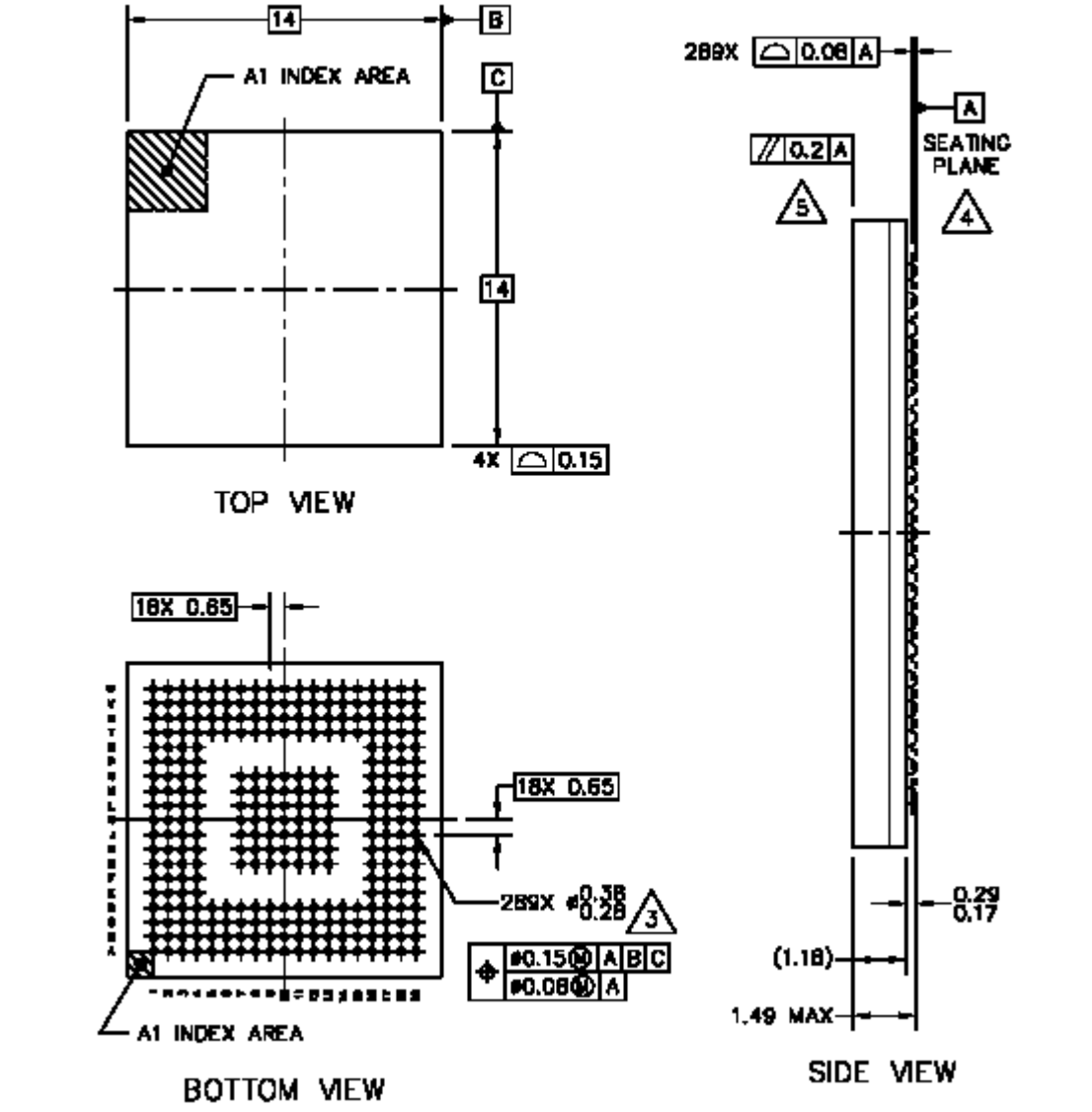


Figure 64. WSC = 3, SYNC = 1, A.HALF/E.HALF

4.1 MAPBGA Package Dimensions

Figure 73 illustrates the MAPBGA 14 mm × 14 mm × 1.41 mm package, which has 0.65 mm ball pitch.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 73. i.MX21 MAPBGA Mechanical Drawing