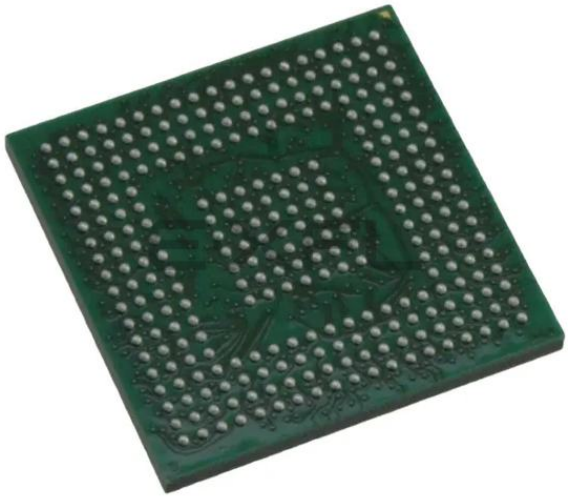

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx21scvmr2

devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

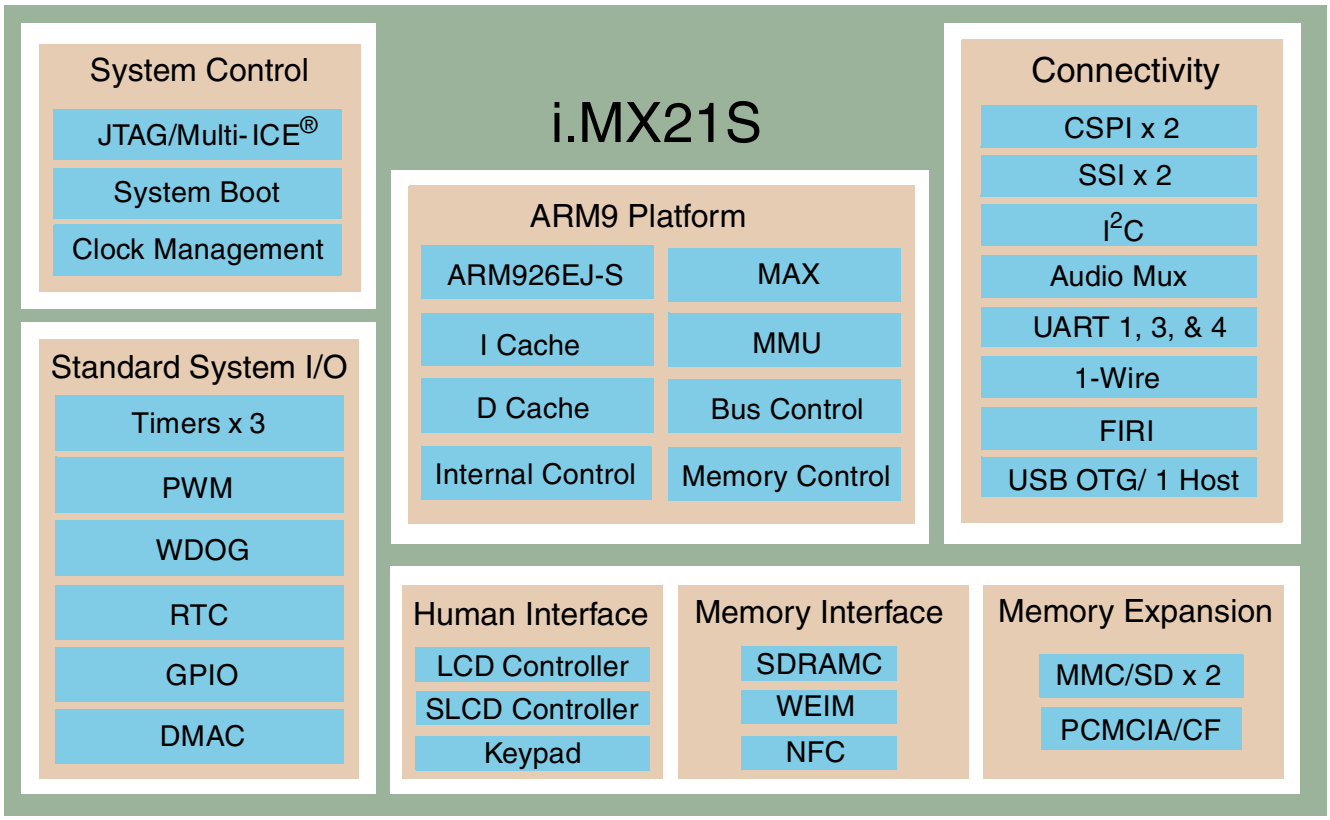


Figure 1. i.MX21S Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
RTCK	JTAG Return Clock used to enhance stability of JTAG debug interface devices. This signal is multiplexed with 1-Wire, therefore using 1-Wire renders RTCK unusable and vice versa.
LCD Controller	
LD [17:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off. LD[15:0] signals are multiplexed with SLCDC1_DAT[15:0] from SLCDC1. LD[16] is multiplexed with $\overline{\text{EXT\_DMAGRANT}}$.
FLM_VSYNC (or simply referred to as VSYNC)	Frame Sync or Vsync—This signal also serves as the clock signal output for gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP_HSYNC (or simply referred to as HSYNC)	Line Pulse or HSync
LSCLK	Shift Clock.
OE_ACD	Alternate Crystal Direction/Output Enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Sampling start signal for left and right scanning. This signal is multiplexed with the SLCDC1_CLK.
PS	Control signal output for source driver (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_CS.
CLS	Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_RS.
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal). This signal is multiplexed with SLCDC1_D0.
Smart LCD Controller	
SLCDC1_CLK	SLCDC Clock output signal. This signal is multiplexed and available at 2 alternate locations. These are SPL_SPR and SD2_CLK signals of LCDC and SD2, respectively.
SLCDC1_CS	SLCDC Chip Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are PS and SD2_CMD signals of LCDC and SD2, respectively.
SLCDC1_RS	SLCDC Register Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are CLS and SD2_D3 signals of LCDC and SD2, respectively.
SLCDC1_D0	SLCDC serial data output signal. This signal is multiplexed and available at 2 alternate signal locations. These are and REV and SD2_D2 signals of LCDC and SD2, respectively. This signal is inactive when a parallel data interface is used.
SLCDC1_DAT[15:0]	SLCDC Data output signals for connection to a parallel SLCD panel interface. These signals are multiplexed with LD[15:0] while an alternate 8-bit SLCD muxing is available on LD[15:8]. Further alternate muxing of these signals are available on some of the USB OTG and USBH1 signals.
SLCDC2_CLK	SLCDC Clock input signal for pass through to SLCD device. This signal is multiplexed with SSI3_CLK signal from SSI3.
SLCDC2_CS	SLCDC Chip Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_TXD signal from SSI3.
SLCDC2_RS	SLCDC Register Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_RXD signal from SSI3.
SLCDC2_D0	SLCD Data input signal for pass through to SLCD device. This signal is multiplexed with SSI3_FS signal from SSI3.

3.2 Recommended Operating Range

Table 4 provides the recommended operating ranges. The device has multiple pairs of VDD and VSS power supply and return pins. QVDD, QVDDx, and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because VDDA pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the VDDA pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 4.

Table 4. 266 MHz Recommended Operating Range

Rating		Symbol	Minimum	Maximum	Unit
Operating temperature range	**Part No. Suffix**				
	VK/VM	T_A	0	70	°C
	CVK/CVM	T_A	- 40	85	°C
I/O supply voltage NVDD 1–6		$NVDD_x$	1.70	3.30	V
Internal supply voltage (Core = 266 MHz)		QVDD, QVDDx	1.45	1.65	V
Analog supply voltage		VDDA	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21S.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA

3.6 Reset Module

The timing relationships of the Reset module with the $\overline{\text{POR}}$ and $\overline{\text{RESET\_IN}}$ are shown in Figure 2 and Figure 3. Be aware that NVDD must ramp up to at least 1.7V for NVDD1 and 2.7V for NVDD2-6 before QVDD is powered up to prevent forward biasing.

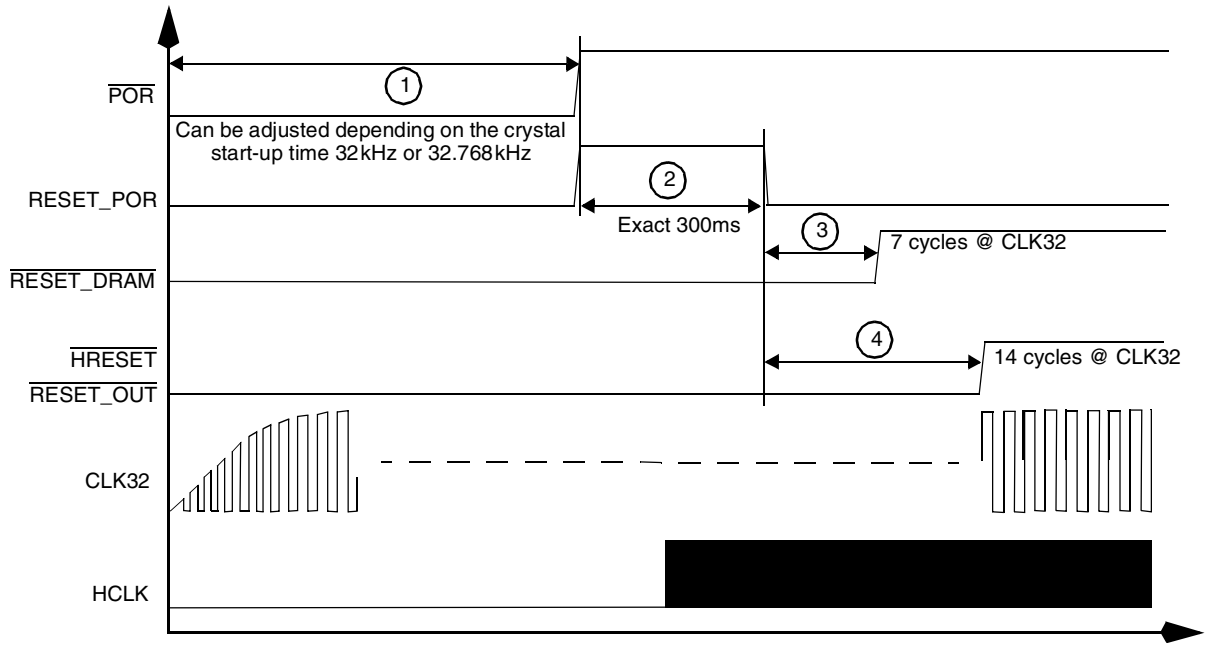


Figure 2. Timing Relationship with $\overline{\text{POR}}$

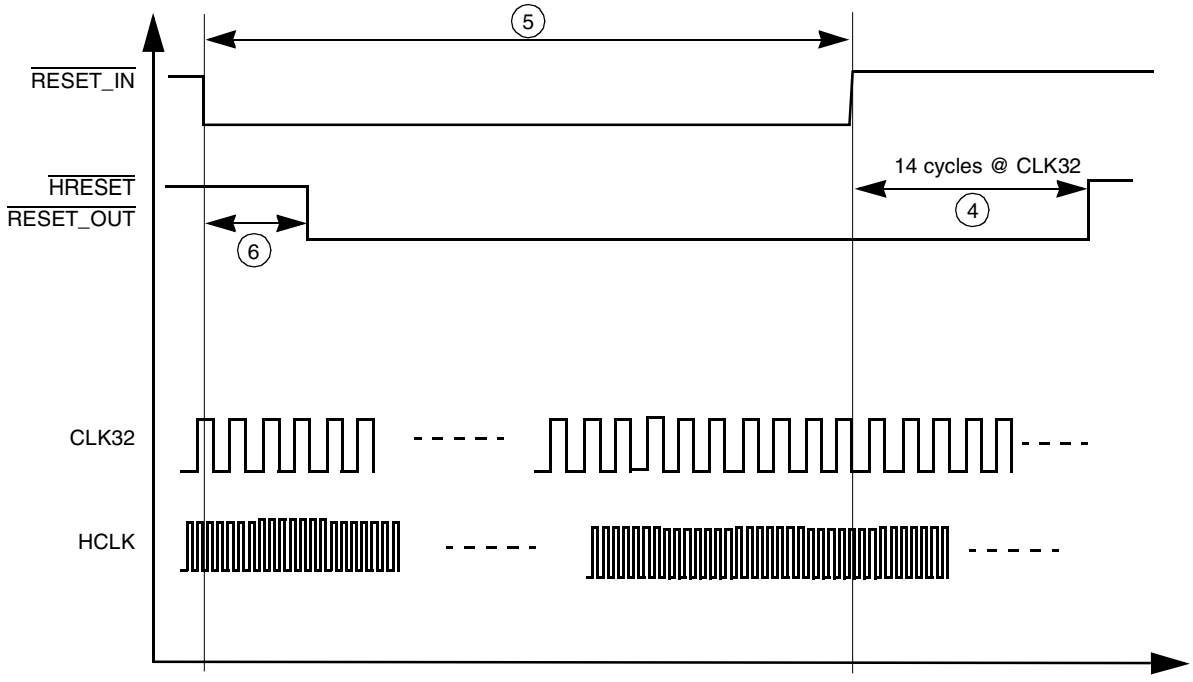


Figure 3. Timing Relationship with $\overline{\text{RESET\_IN}}$

becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO.

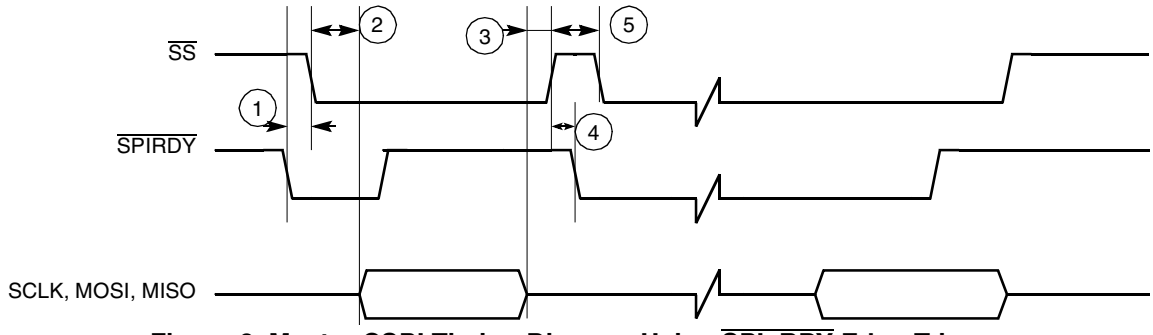


Figure 6. Master CSPI Timing Diagram Using SPI_RDY Edge Trigger

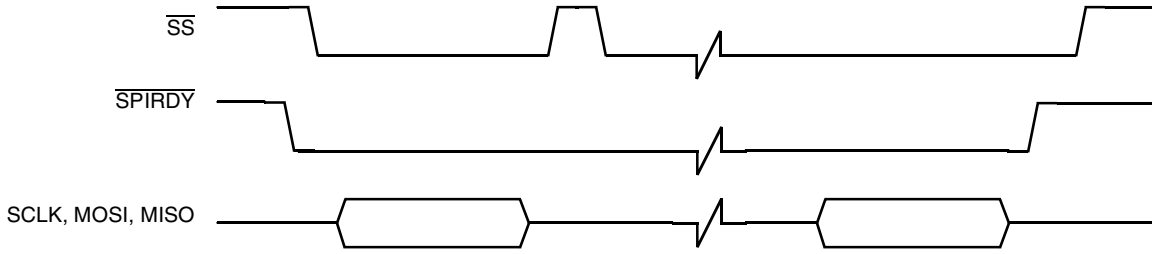


Figure 7. Master CSPI Timing Diagram Using SPI_RDY Level Trigger

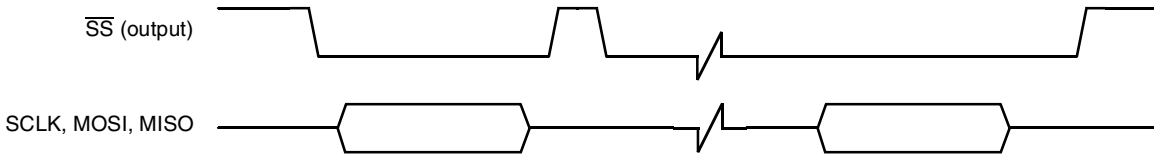


Figure 8. Master CSPI Timing Diagram Ignore SPI_RDY Level Trigger

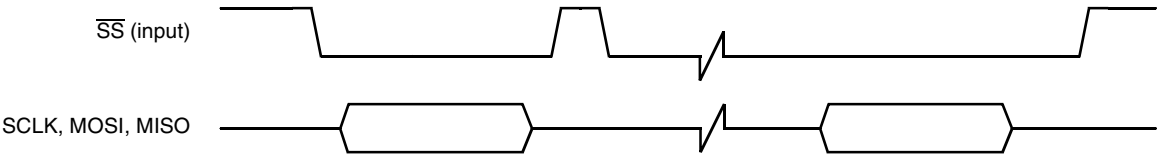


Figure 9. Slave CSPI Timing Diagram FIFO Advanced by BIT COUNT

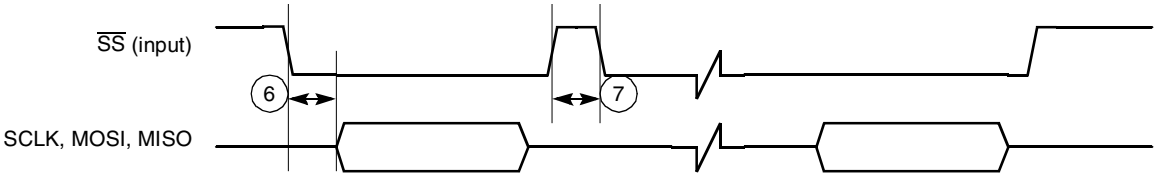


Figure 10. Slave CSPI Timing Diagram FIFO Advanced by SS Rising Edge

3.10 Smart LCD Controller

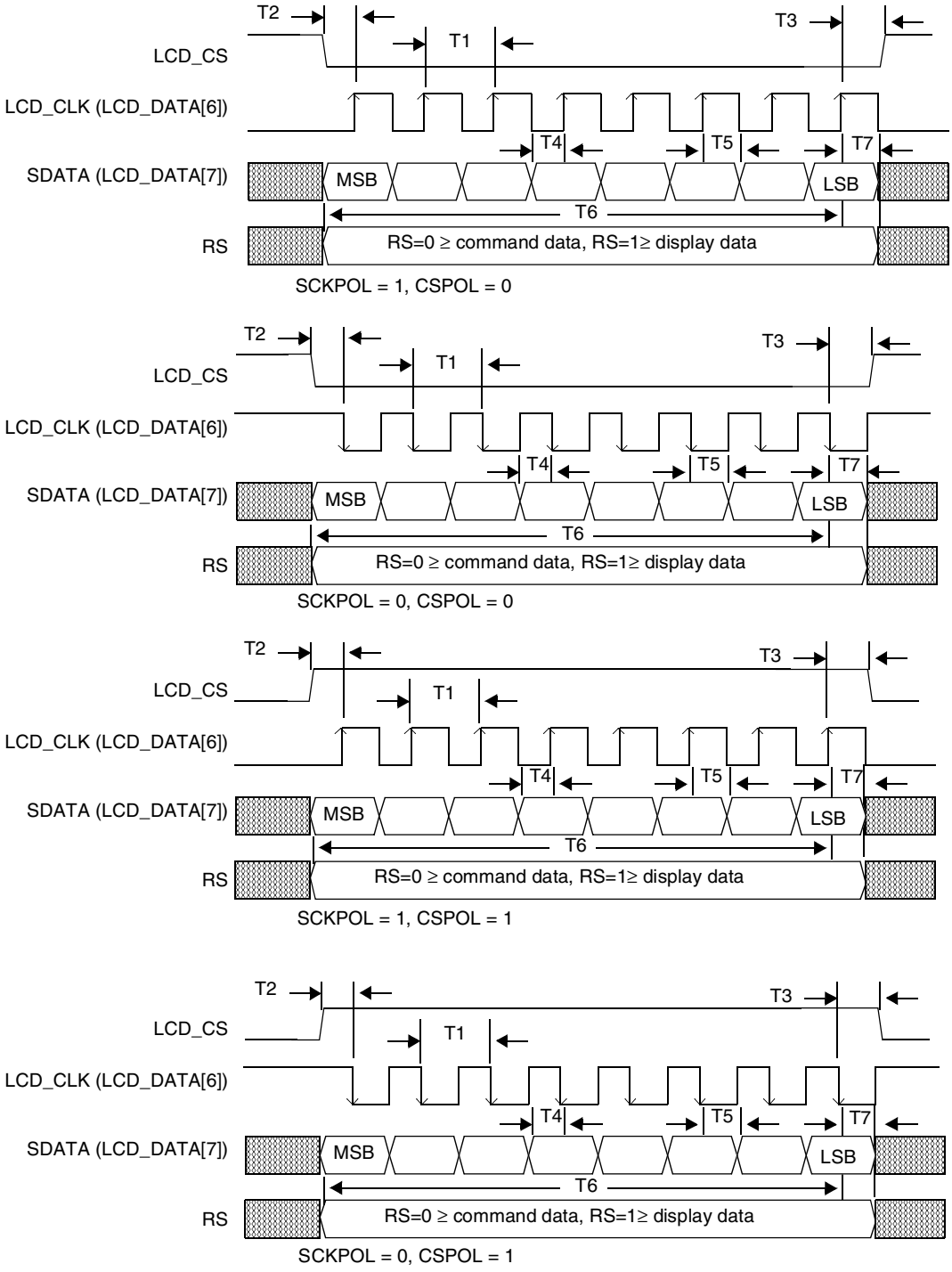


Figure 15. SLCDC Serial Transfer Timing

3.12 External Memory Interface (EMI) Electricals

3.12.1 NAND-Flash Controller (NFC) Interface

Figure 25, Figure 26, Figure 27, and Figure 28 depict the relative timing requirements among different signals of the NFC at module level, and Table 24 lists the timing parameters. The NAND Flash Controller (NFC) timing parameters are based on the internal NFC clock generated by the Clock Controller module, where time T is the period of the NFC clock in ns. Per the i.MX21S Reference Manual, specifically the *Phase-Locked (PLL), Clock, and Reset Controller* chapter, the NFC clock is derived from the same clock which drives the CPU clock (FCLK) that is fed through the NFCDIV block to generate the NFC clock. The relationship between the NFC clock and the external timing parameters of the NFC is provided in Table 24.

Table 24 also provides two examples of external timing parameters with NFC clock frequencies of 22.17 MHz and 33.25 MHz. For example, assuming a 266 MHz FCLK (CPU clock), NFCDIV should be set to divide-by-12 to generate a 22.17 MHz NFC clock and divide-by-8 to generate a 33.25 MHz NFC clock. The user should compare the parameters of the selected NAND Flash memory with the NFC external timing parameters to determine the proper NFC clock. *The maximum NFC clock allowed is 66 MHz*. It should also be noted that the default NFC clock on power up is 16.63 MHz.

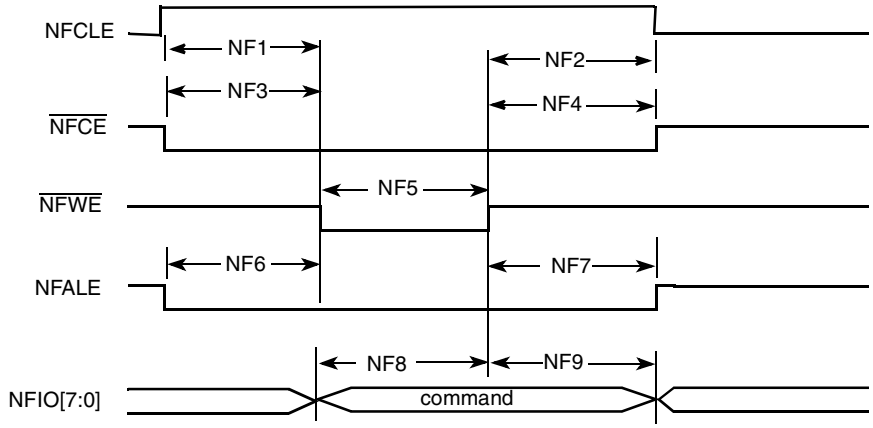
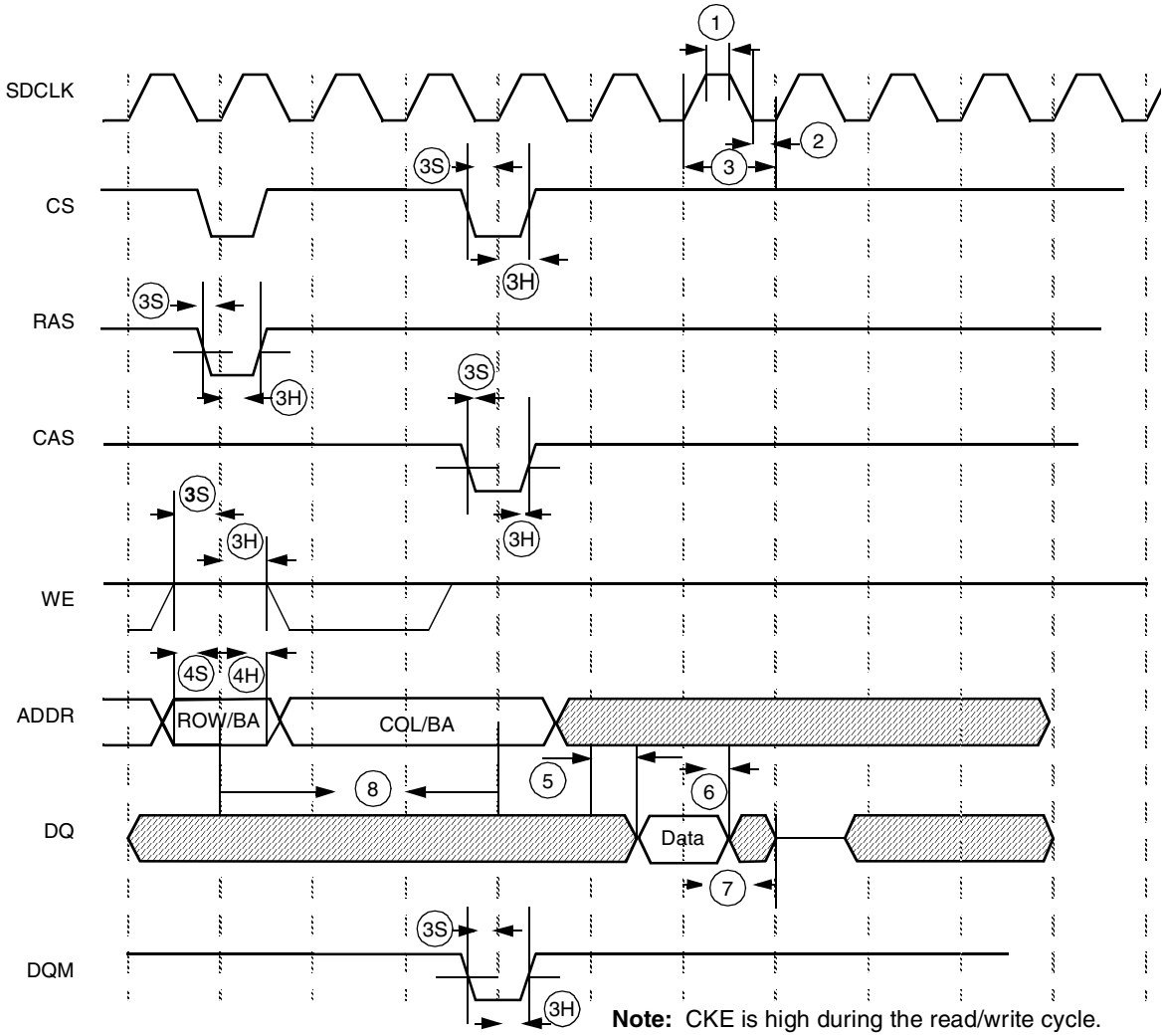


Figure 25. Command Latch Cycle Timing Diagram

3.14 SDRAM Memory Controller

The following figures (Figure 30 through Figure 33) and their associated tables specify the timings related to the SDRAMC module in the i.MX21S.



Note: CKE is high during the read/write cycle.

Figure 30. SDRAM Read Cycle Timing Diagram

Table 26. SDRAM Read Cycle Timing Parameter

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	$\overline{\text{SDRAM}}$ clock low-level width	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	4.78	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	3.03	–	2	–	ns

Table 27. SDRAM Write Cycle Timing Parameter

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	$\overline{\text{SDRAM clock low-level width}}$	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
4	Address setup time	3.67	–	2	–	ns
5	Address hold time	2.95	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP}[2]	–	ns
7	Active to read/write command delay	t_{RCD}[2]	–	t_{RCD}[2]	–	ns
8	Data setup time	3.41	–	2	–	ns
9	Data hold time	2.45	–	2	–	ns

1. Precharge cycle timing is included in the write timing diagram.
2. t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

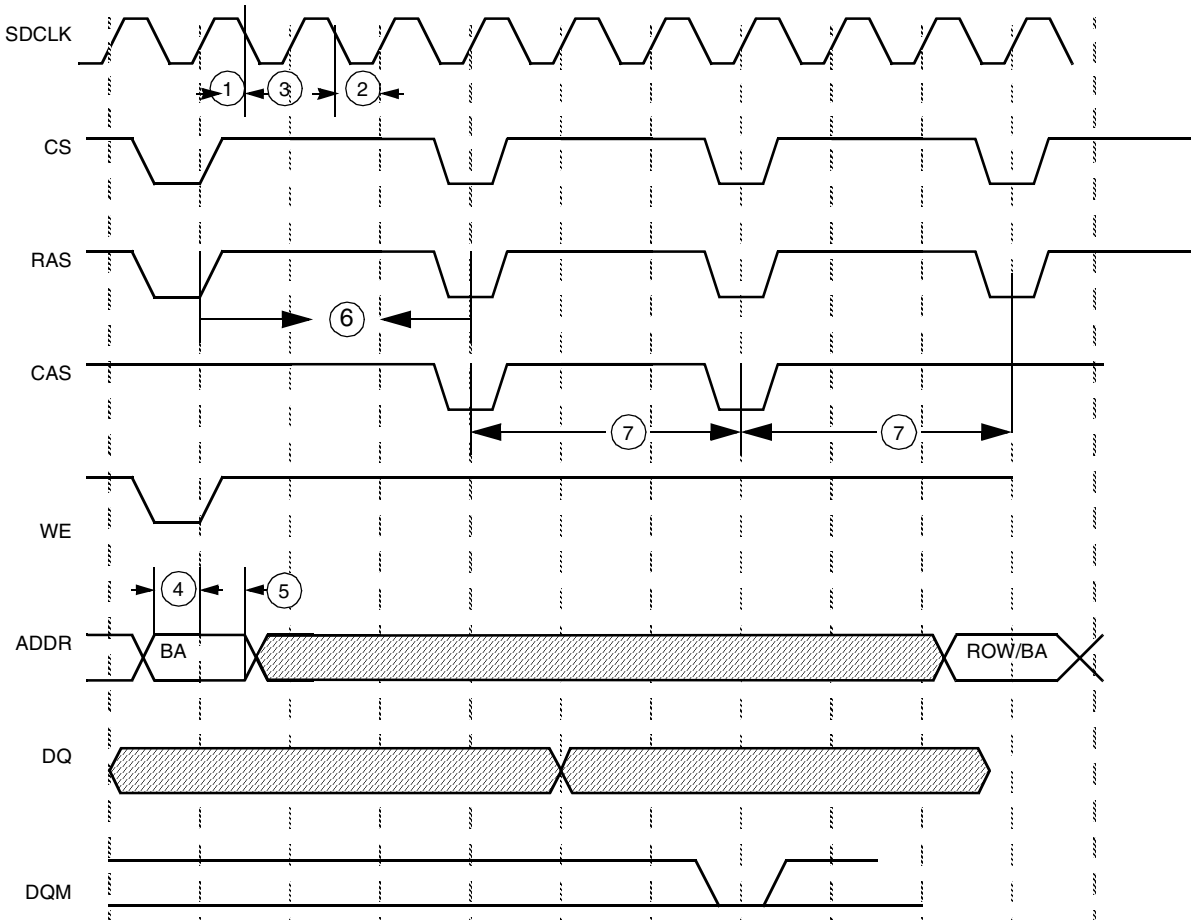


Figure 32. SDRAM Refresh Timing Diagram

Table 32. SSI to SSI3 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI3 Ports)						
1	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-2.09	-0.66	-2.09	-0.66	ns
3	(Rx) CK high to FS (bl) high	-2.74	-0.84	-2.74	-0.84	ns
4	(Tx) CK high to FS (bl) low	-2.09	-0.66	-2.09	-0.66	ns
5	(Rx) CK high to FS (bl) low	-2.74	-0.84	-2.74	-0.84	ns
6	(Tx) CK high to FS (wl) high	-2.09	-0.66	-2.09	-0.66	ns
7	(Rx) CK high to FS (wl) high	-2.74	-0.84	-2.74	-0.84	ns
8	(Tx) CK high to FS (wl) low	-2.09	-0.66	-2.09	-0.66	ns
9	(Rx) CK high to FS (wl) low	-2.74	-0.84	-2.74	-0.84	ns
10	(Tx) CK high to STXD valid from high impedance	-1.73	-0.26	-1.73	-0.26	ns
11a	(Tx) CK high to STXD high	-2.87	-0.80	-2.87	-0.80	ns
11b	(Tx) CK high to STXD low	-2.87	-0.80	-2.87	-0.80	ns
12	(Tx) CK high to STXD high impedance	-1.73	-0.26	-1.73	-0.26	ns
13	SRXD setup time before (Rx) CK low	22.77	–	22.77	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI3 Ports)						
15	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	9.62	17.10	7.90	15.61	ns
19	(Rx) CK high to FS (bl) high	10.30	19.54	8.58	18.05	ns
20	(Tx) CK high to FS (bl) low	9.62	17.10	7.90	15.61	ns
21	(Rx) CK high to FS (bl) low	10.30	19.54	8.58	18.05	ns
22	(Tx) CK high to FS (wl) high	9.62	17.10	7.90	15.61	ns
23	(Rx) CK high to FS (wl) high	10.30	19.54	8.58	18.05	ns
24	(Tx) CK high to FS (wl) low	9.62	17.10	7.90	15.61	ns
25	(Rx) CK high to FS (wl) low	10.30	19.54	8.58	18.05	ns
26	(Tx) CK high to STXD valid from high impedance	9.02	16.46	7.29	14.97	ns
27a	(Tx) CK high to STXD high	8.48	15.32	6.75	13.83	ns
27b	(Tx) CK high to STXD low	8.48	15.32	6.75	13.83	ns

3.18.1 EIM External Bus Timing Diagrams

The following timing diagrams show the timing of accesses to memory or a peripheral.

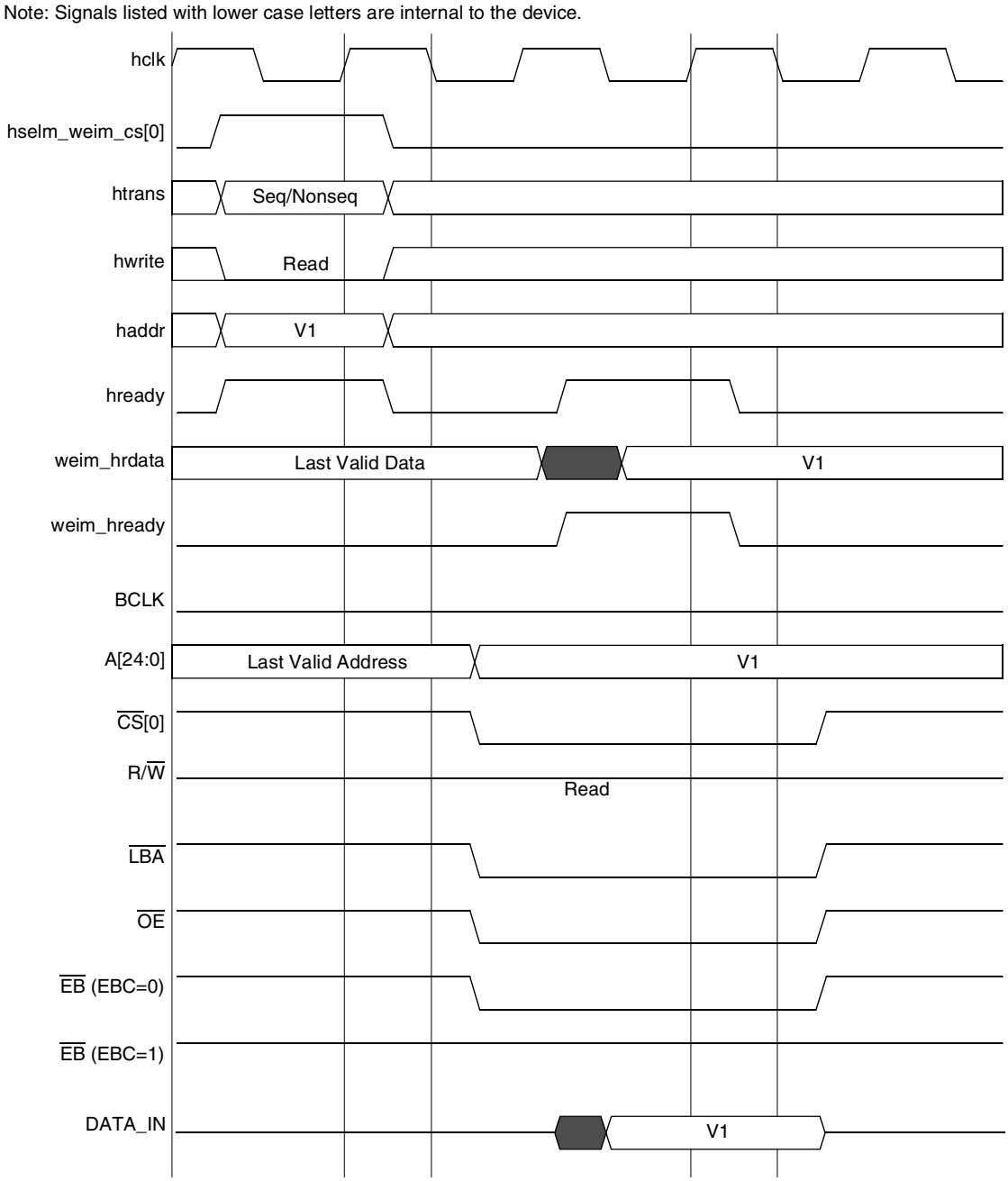


Figure 46. WSC = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

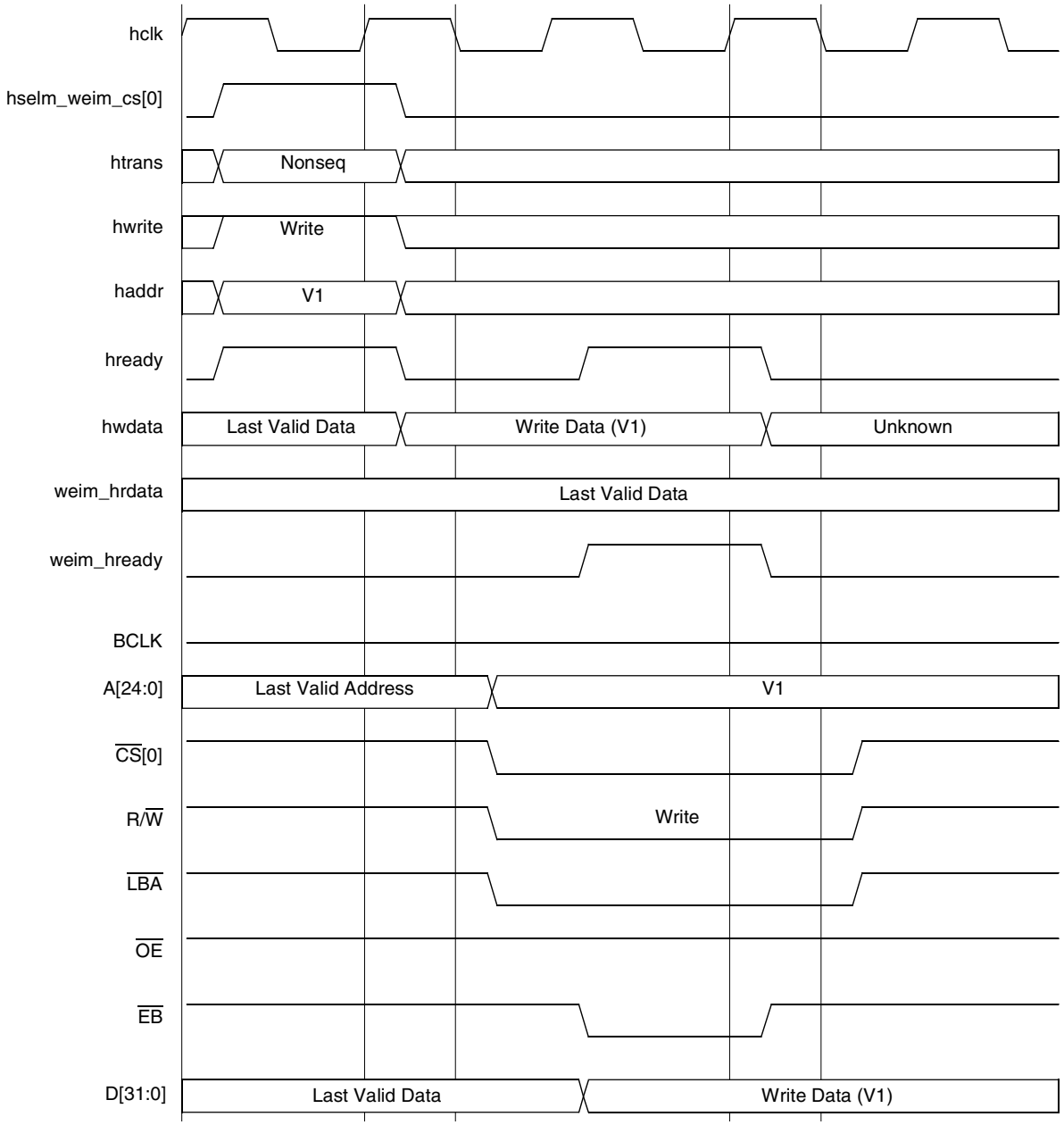


Figure 47. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

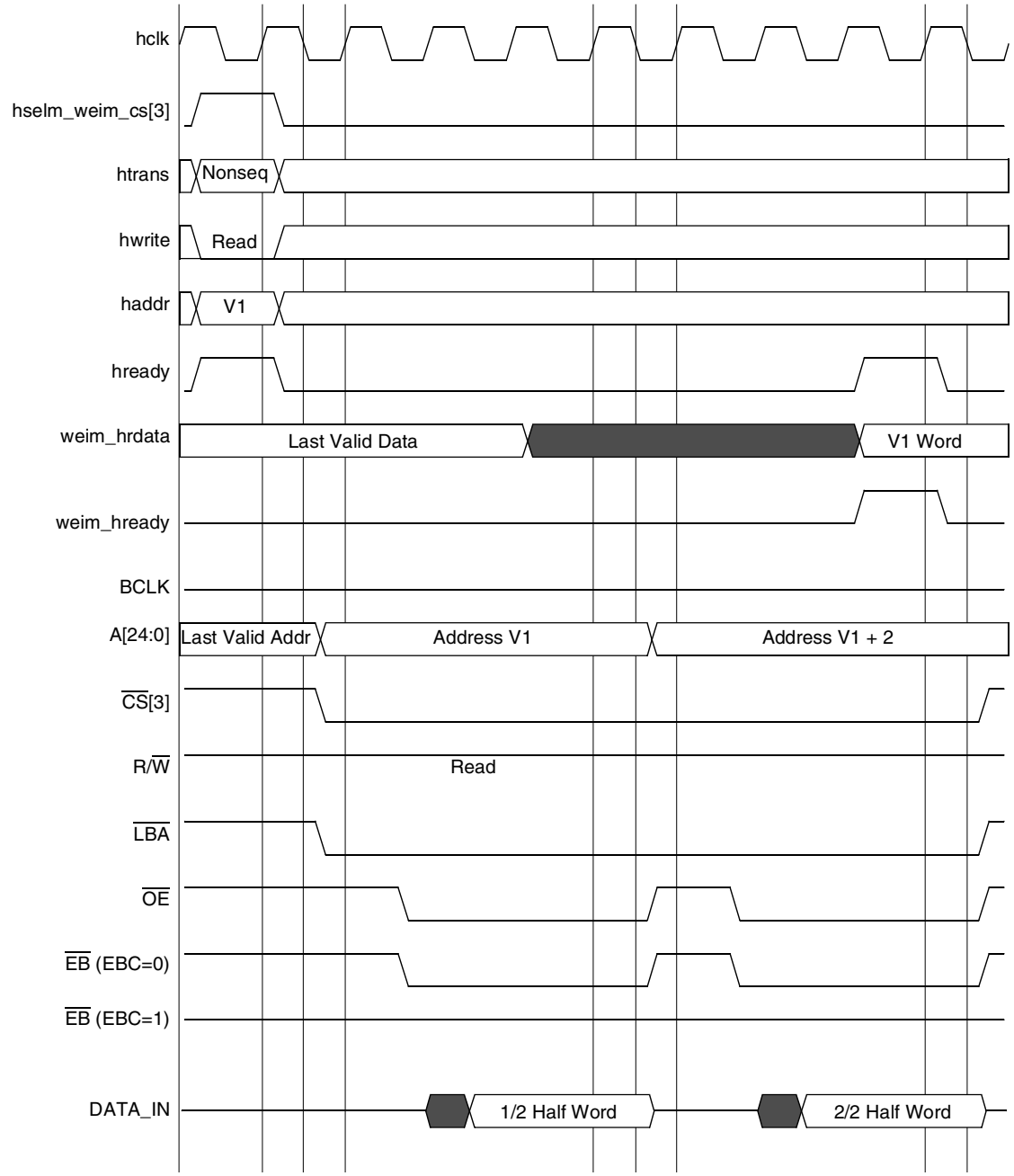


Figure 50. WSC = 3, OEA = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

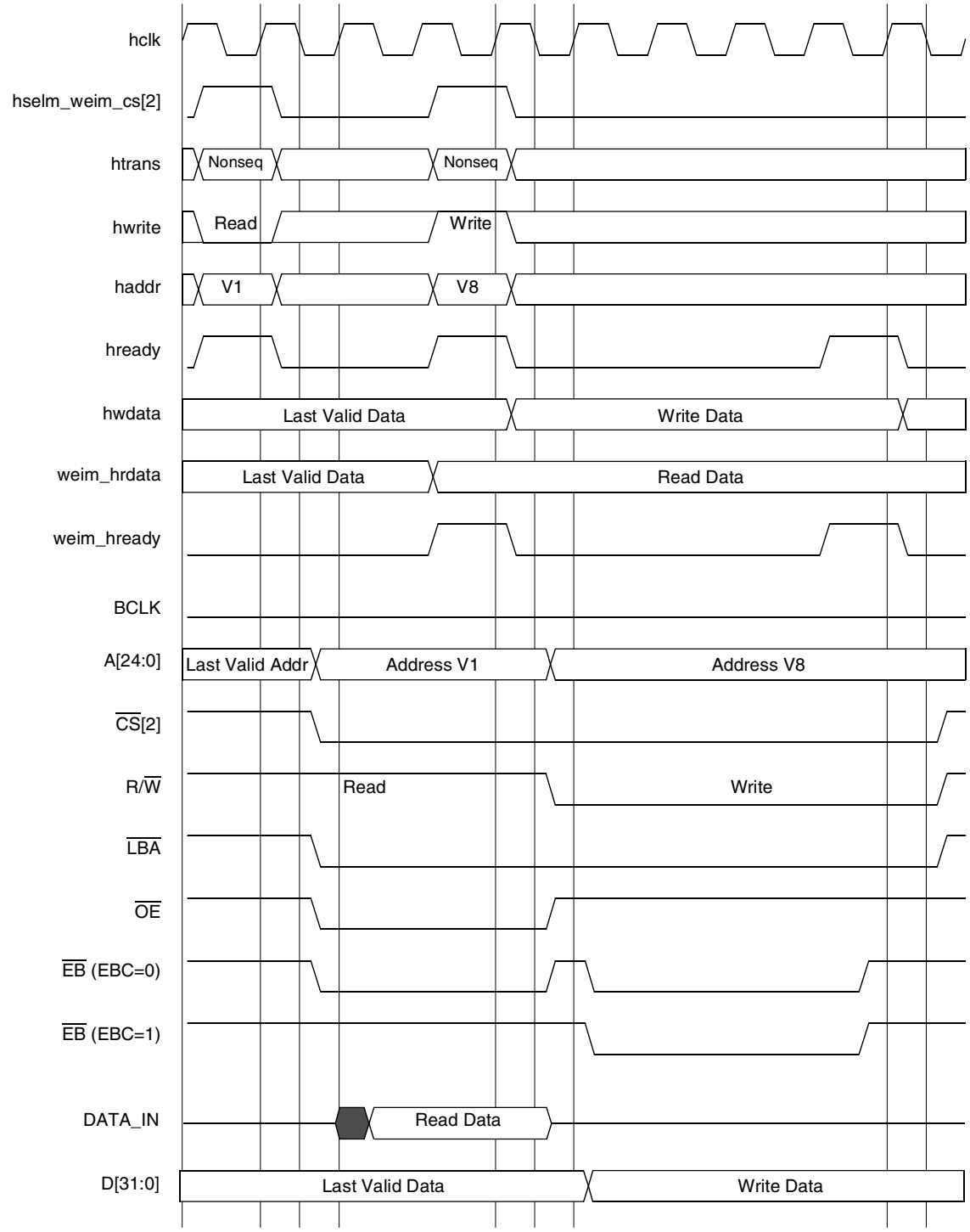


Figure 58. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

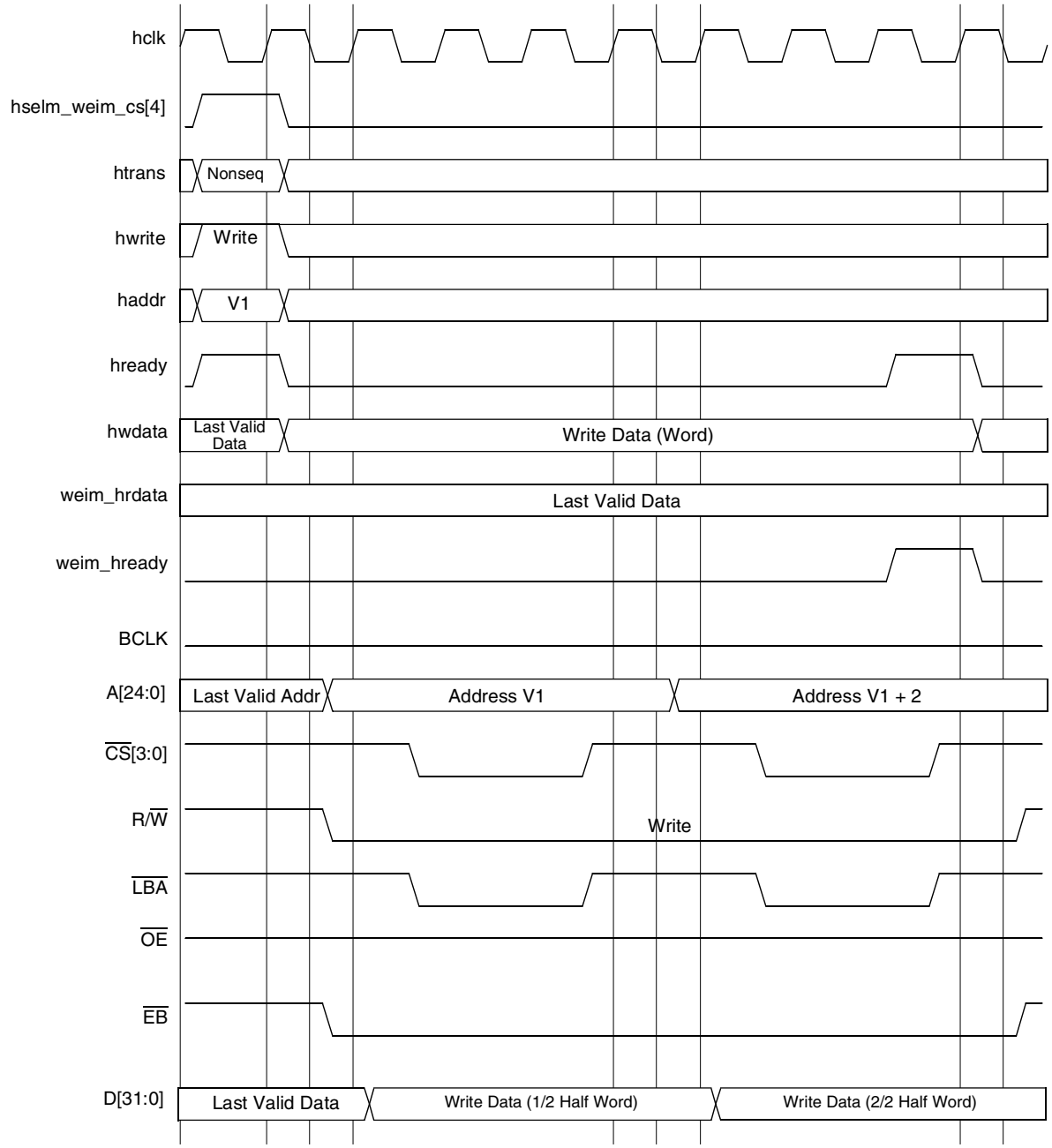


Figure 60. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

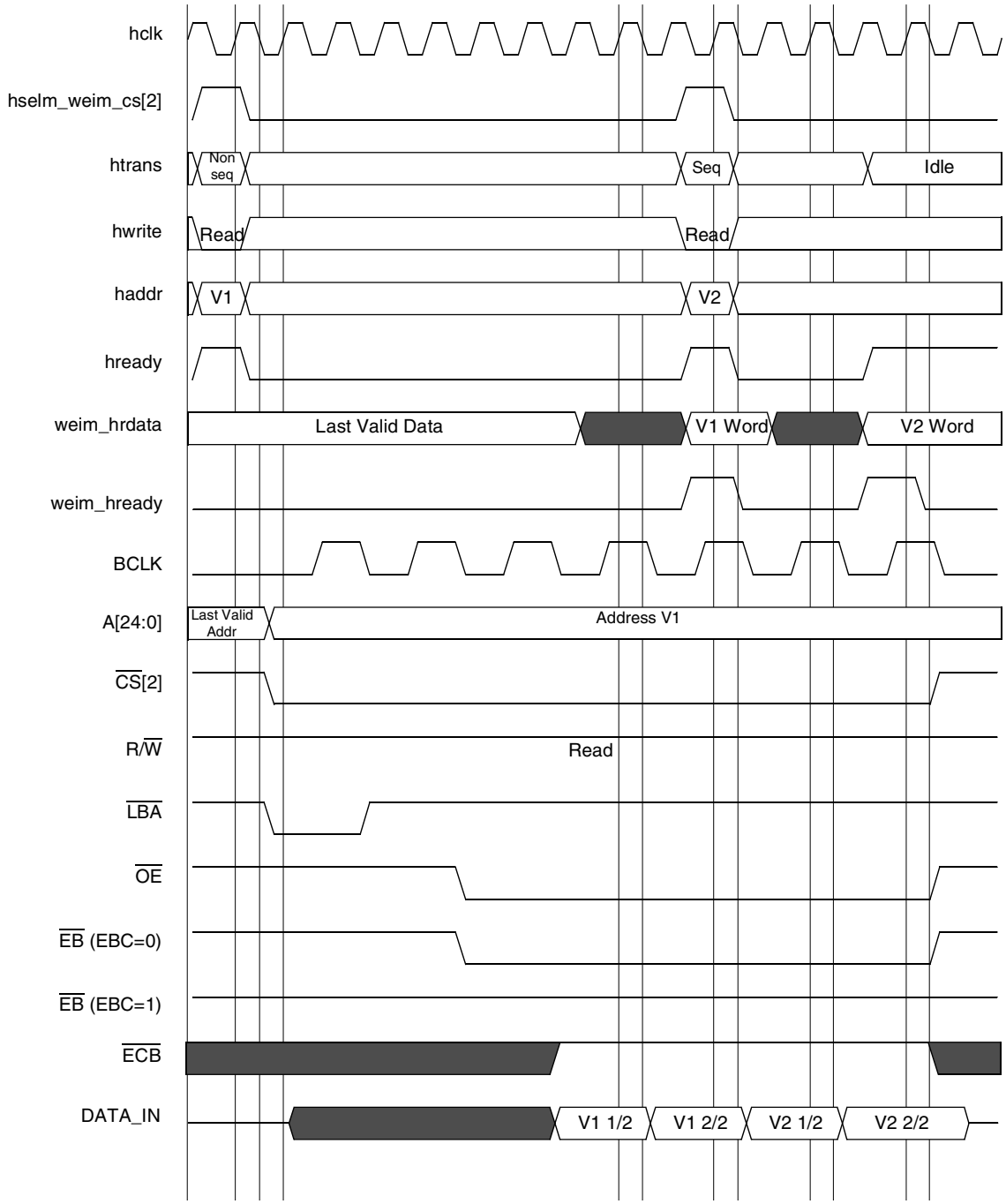


Figure 68. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

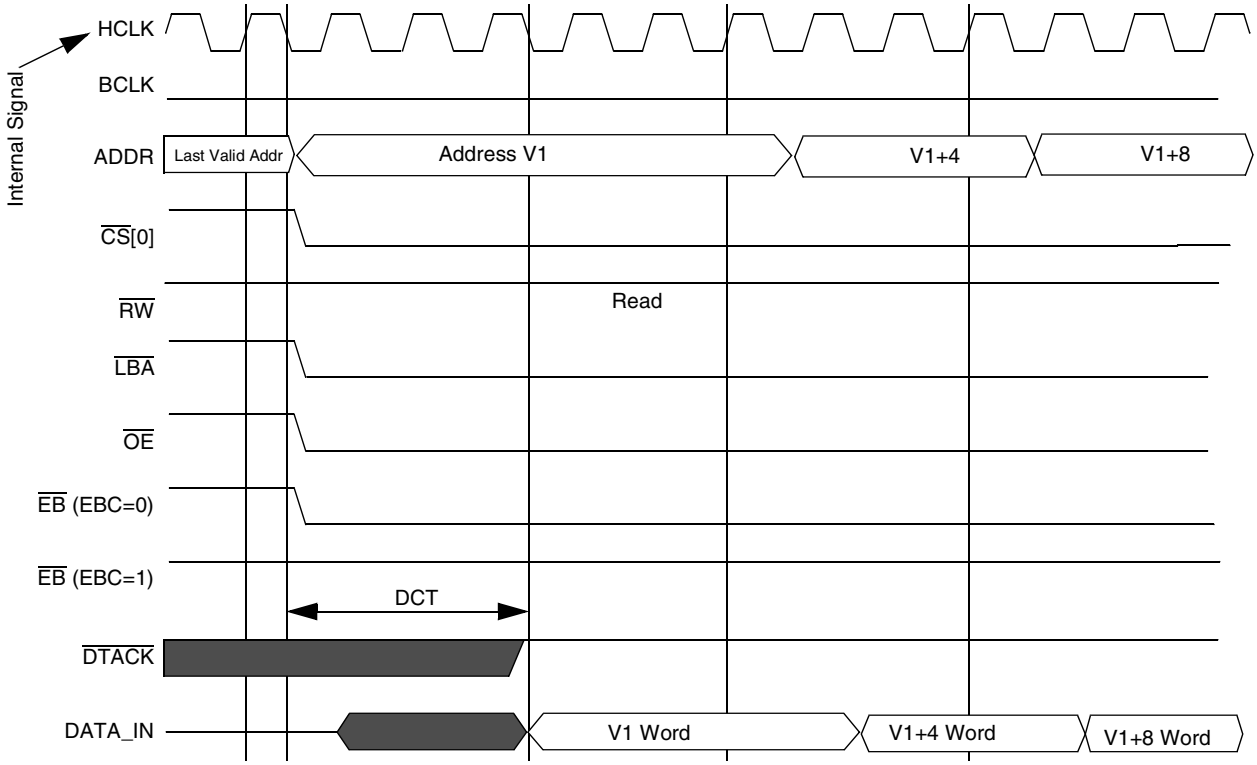


Figure 70. DTACK Level Sensitive Sequential Read Accesses, WSC=2, EW=1, DCT=1, AGE=0 (Example of DTACK Remaining High)

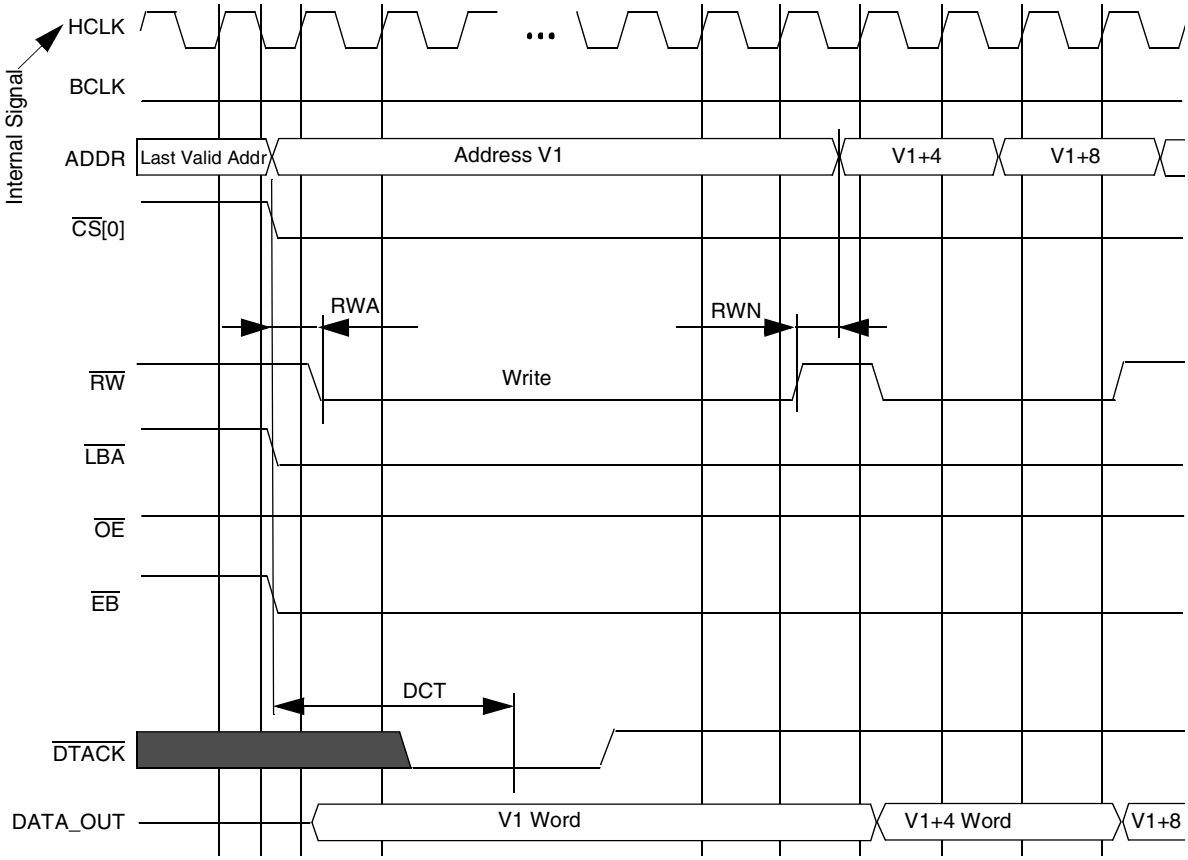
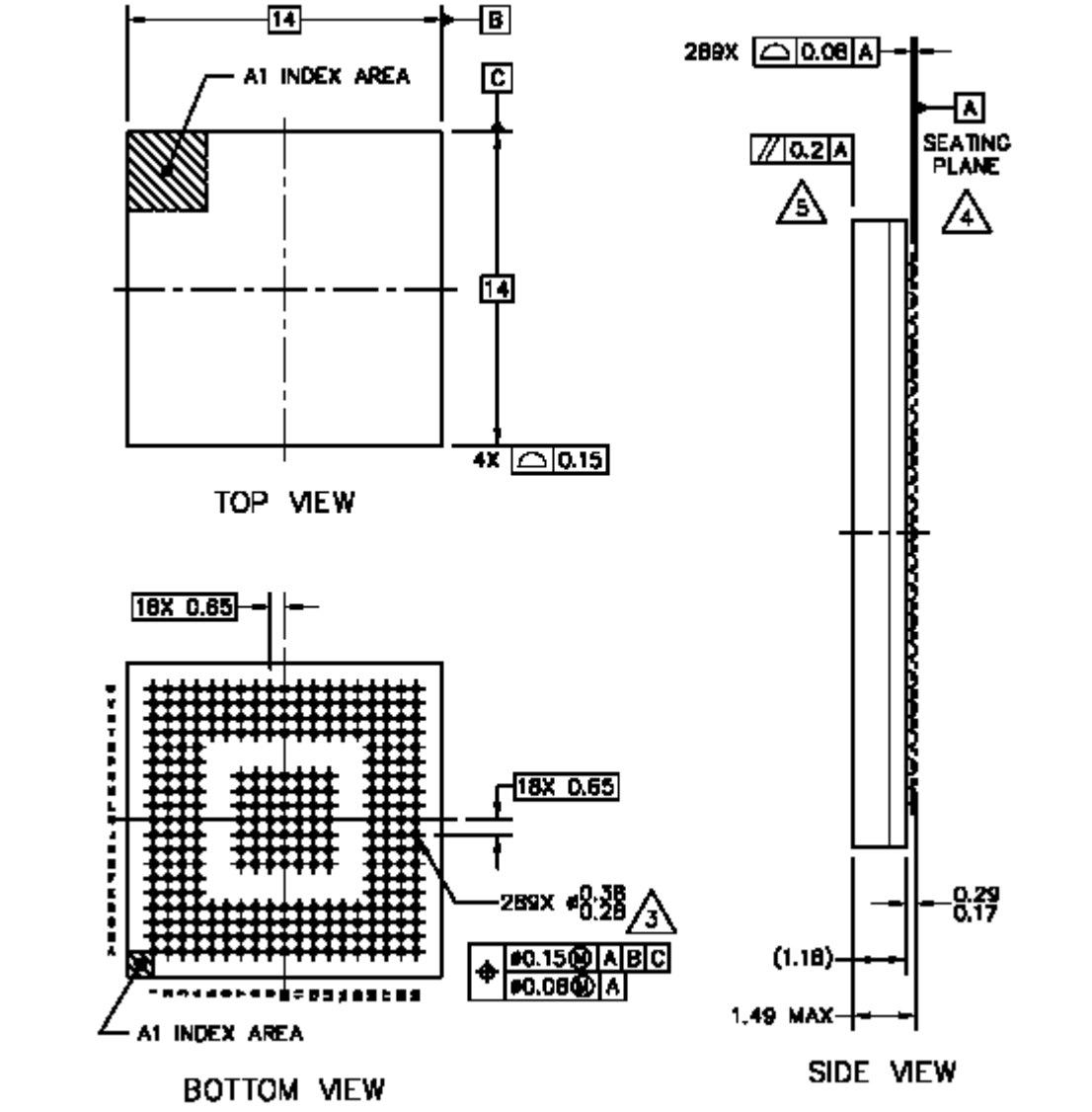


Figure 71. DTACK Level Sensitive Sequential Write Accesses, WSC=2, EW=1, RWA=1, RWN=1, DCT=1, AGE=0 (Example of DTACK Asserting)

4.1 MAPBGA Package Dimensions

Figure 73 illustrates the MAPBGA 14 mm × 14 mm × 1.41 mm package, which has 0.65 mm ball pitch.



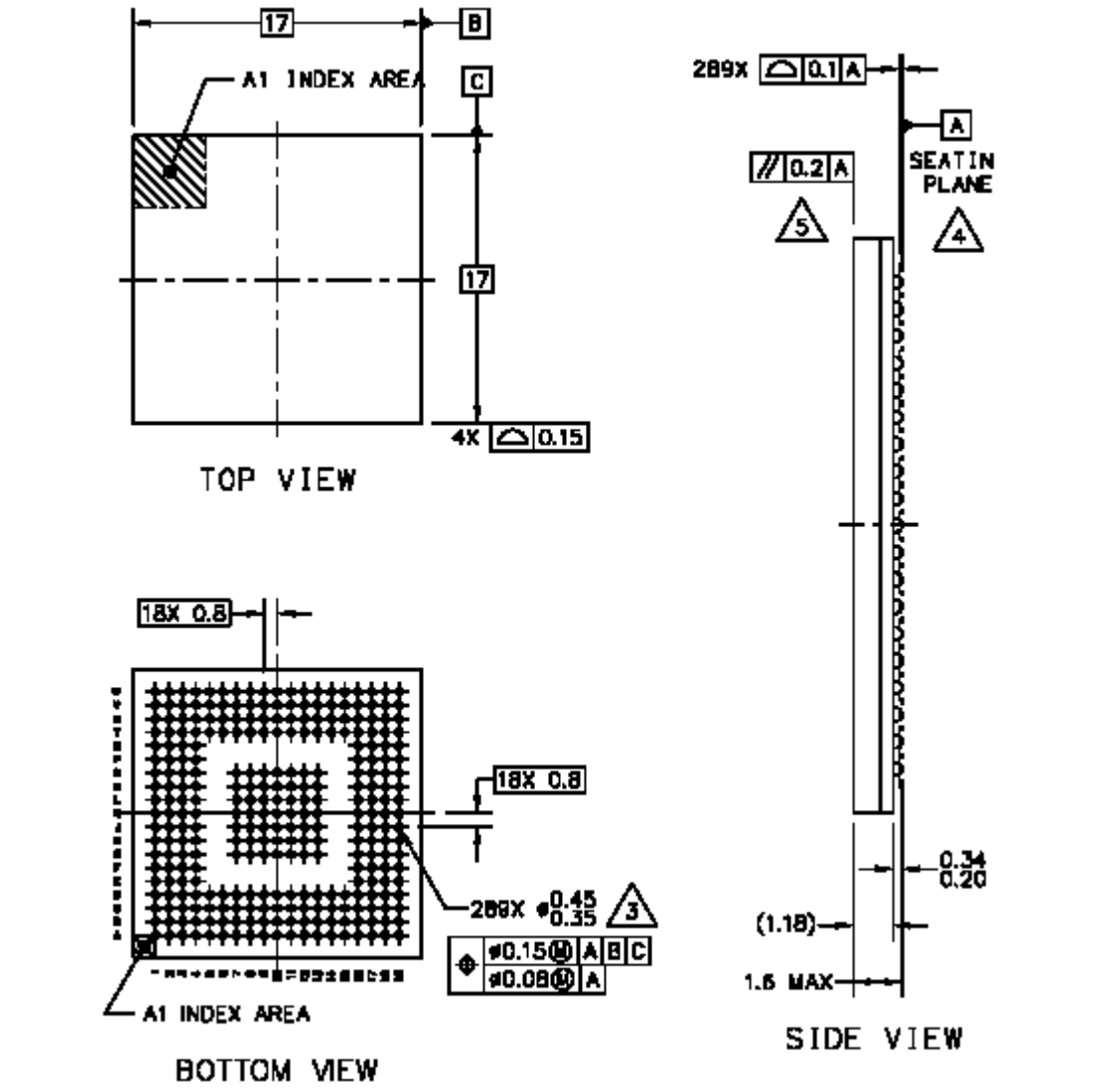
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 73. i.MX21 MAPBGA Mechanical Drawing

4.2 MAPBGA Package Dimensions

Figure 74 illustrates the MAPBGA 17 mm × 17 mm × 1.45 mm package, which has 0.8 mm spacing between the pads.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 74. i.MX21 MAPBGA Mechanical Drawing