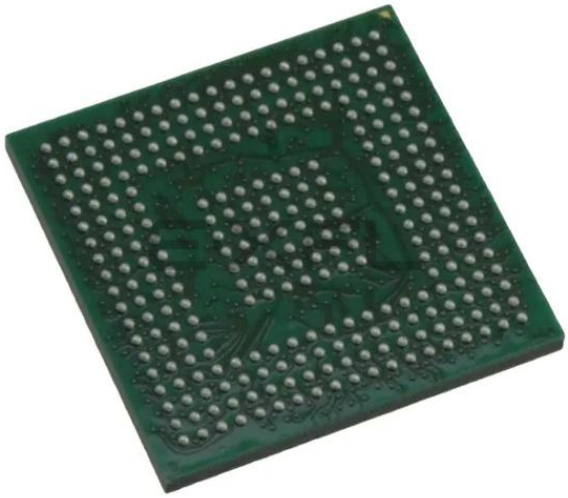

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mx21svkr2

- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Reference Documentation

The following documents are required for a complete description of the i.MX21S and are necessary to design properly with the device. Especially for those not familiar with the ARM926EJ-S processor the following documents are helpful when used in conjunction with this manual.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM7TDMI Data Sheet (ARM Ltd., order number ARM DDI 0029)

ARM920T Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

MC9328MX21S Product Brief (order number MC9328MX21SPB)

The Freescale manuals are available on the Freescale Semiconductor Web site at http://www.freescale.com. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

1.3 Ordering Information

Table 1 provides ordering information for the device.

Table 1. Ordering Information

Part Order Number	Package Size	Package Type	Operating Range
MC9328MX21SVK	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	0°C–70°C
MC9328MX21SCVK	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	-40°C–85°C
MC9328MX21SVM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	0°C–70°C
MC9328MX21SCVM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	-40°C–85°C

1.4 Features

The i.MX21S boasts a robust array of features that can support a wide variety of applications. Below is a brief description of i.MX21S features.

- ARM926EJ-S Core Complex
- Display and Video Modules
  - — LCD Controller (LCDC)
  - — Smart LCD Controller (SLCDC)
- Wireless Connectivity
  - — Fast Infra-Red Interface (FIRI)
- Wired Connectivity
  - — USB On-The-Go (USBOTG) Controller

  - Three Universal Asynchronous Receiver/Transmitters (UART*x*)
  - Two Configurable Serial Peripheral Interfaces (CSPI*x*) for High Speed Data Transfer
  - Inter-IC (I^2C) Bus Module
  - Two Synchronous Serial Interfaces (SSI) with Inter-IC Sound (I^2S)
  - Digital Audio Mux
  - One-Wire Controller
  - Keypad Interface
- Memory Expansion and I/O Card Support
  - Two Multimedia Card and Secure Digital (MMC/SD) Host Controller Modules
- Memory Interface
  - External Interface Module (EIM)
  - SDRAM Controller (SDRAMC)
  - NAND Flash Controller (NFC)
  - PCMCIA/CF Interface
- Standard System Resources
  - Clock Generation Module (CGM) and Power Control Module
  - Three General-Purpose 32-Bit Counters/Timers
  - Watchdog Timer
  - Real-Time Clock/Sampling Timer (RTC)
  - Pulse-Width Modulator (PWM) Module
  - Direct Memory Access Controller (DMAC)
  - General-Purpose I/O (GPIO) Ports
  - Debug Capability

2 Signal Descriptions

Table 2 identifies and describes the i.MX21S signals. Pin assignment is provided in Section 4, “Pin Assignment and Package Information” and in the “Signal Multiplexing Scheme” table within the reference manual.

The connections of the pins in Table 2 depends solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX21S processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_48M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- TEST_WB[2:0]: These signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not utilizing these signals for GPIO functionality or for their other multiplexed function, then configure as GPIO input with pull up enabled, and leave as a no connect.
- TEST_WB[4:3]: To ensure proper operation, leave these signals as no connects.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{CAS}$	SDRAM Column Address Select signal
$\overline{SDWE}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
Clocks and Resets	
EXTAL26M	Crystal input (26MHz), or a 16 MHz to 32 MHz oscillator (or square-wave) input when the internal oscillator circuit is shut down. When using an external signal source, feed this input with a square wave signal switching from GND to VDDA.
XTAL26M	Oscillator output to external crystal. When using an external signal source, float this output.
EXTAL32K	32 kHz or 32.768 kHz crystal input. When using an external signal source, feed this input with a square wave signal switching from GND to QVDD5.
XTAL32K	Oscillator output to external crystal. When using an external signal source, float this output.
CLKO	Clock Out signal selected from internal clock signals. Please refer to clock controller for internal clock selection.
EXT_48M	This is a special factory test signal. To ensure proper operation, connect this signal to ground.
EXT_266M	This is a special factory test signal. To ensure proper operation, connect this signal to ground.
$\overline{RESET\_IN}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
$\overline{RESET\_OUT}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{RESET\_IN}$), and Watchdog time-out.
$\overline{POR}$	Power On Reset—Active low Schmitt trigger input signal. The $\overline{POR}$ signal is normally generated by an external RC circuit designed to detect a power-up event.
CLKMODE[1:0]	These are special factory test signals. To ensure proper operation, leave these signals as no connects.
OSC26M_TEST	This is a special factory test signal. To ensure proper operation, leave this signal as a no connect.
TEST_WB[2:0]	These are special factory test signals. However, these signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not using these signals for GPIO functions or for other multiplexed functions, then configure as GPIO input with pull-up enabled, and leave as a no connect.
TEST_WB[4:3]	These are special factory test signals. To ensure proper operation, leave these signals as no connects.
WKGD	Battery indicator input used to qualify the walk-up process. Also multiplexed with TIN.
JTAG For termination recommendations, see the Table "*JTAG pinouts*" in the *Multi-ICE® User Guide* from ARM® Limited.	
$\overline{TRST}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
TDO	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
JTAG_CTRL	JTAG Controller select signal—JTAG_CTRL is sampled during the rising edge of TRST. Must be pulled to logic high for proper JTAG interface to debugger. Pulling JTAG_CRTL low is for internal test purposes only.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave
SYS_CLK1	SSI1 master clock. Multiplexed with TOUT.
SSI2_CLK	Serial clock signal which is output in master or input in slave.
SSI2_TXD	Transmit serial data signal
SSI2_RXD	Receive serial data
SSI2_FS	Frame Sync signal which is output in master and input in slave.
SYS_CLK2	SSI2 master clock. Multiplexed with TOUT.
SSI3_CLK	Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK
SSI3_TXD	Transmit serial data signal which is multiplexed with SLCDC2_CS
SSI3_RXD	Receive serial data which is multiplexed with SLCDC2_RS
SSI3_FS	Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0.
SAP_CLK	Serial clock signal which is output in master or input in slave.
SAP_TXD	Transmit serial data
SAP_RXD	Receive serial data
SAP_FS	Frame Sync signal which is output in master and input in slave.
I^2C	
I2C_CLK	I^2C Clock
I2C_DATA	I^2C Data
1-Wire	
OWIRE	1-Wire input and output signal. This signal is multiplexed with JTAG RTCK.
PWM	
PWMO	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module.
General Purpose Input/Output	
PB[10:21], PF[16]	Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled.
Keypad	
KP_COL[7:0]	Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2\_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available.

Table 5. DC Characteristics (Continued)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V
Input leakage current (no pull-up or pull-down)	I_{in}	V_{in} = 0 or NVDD	–	–	±1	µA
I/O leakage current	I_{OZ}	$V_{I/O}$ = NVDD or 0 I/O = High impedance state	–	–	±5	µA

1. Data labeled Typical is not guaranteed, but is intended as an indication of the IC's potential performance.
2. For DSCR definition refer to the System Control chapter in the reference manual.

Table 6 shows the input and output capacitance for the device.

Table 6. Input/Output Capacitance

Parameter	Symbol	Min	Typ	Max	Units
Input capacitance	C_i	_	_	5	pF
Output capacitance	C_o	_	_	5	pF

Table 7 shows the power consumption for the device.

Table 7. Power Consumption

ID	Parameter	Conditions	Symbol	Typ	Max	Units
1	Run Current	QVDD = QVDDX = 1.65 V, NVDD1 = 1.8 V. NVDD2 through NVDD6 = VDDA = 3.1V. Core = 266 MHz, System = 133 MHz. MPEG4 Playback (QVGA) from MMC/SD card, 30fps, 44.1kHz audio.	I_{QVDD} + I_{QVDDX}	120	–	mA
			I_{NVDD1}	8	–	mA
			I_{NVDD2} through I_{NVDD6} + I_{VDDA}	6.6	–	mA
2	Sleep Current	Standby current with Well Biasing System enabled. Well Bias Control Register (WBCR) must be set as follows: WBCR: CRM_WBS bits = 01 CRM_WBFA bit = 1 CRM_WBM bits = 001 CRM_SPA_SEL bit = 1 FMCR bit = 1 For WBCR definition refer to System Control Chapter in the reference manual.	**I_{STBY}**			
			QVDD = QVDDX = 1.65V, TA[1]	–	3.0	mA
			QVDD = QVDDX = 1.65V, 25°	–	700	µA
			QVDD = QVDDX = 1.55V, 25°	320	–	µA

1. TA = 70°C for suffixes VK, VM, DVK, DVM, and SVK. TA = 85°C for suffixes CVK, CVM, and SCVK.

3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 11. In this table, T_{ref} is a reference clock period after the predivider and T_{dck} is the output double clock period.

Table 11. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock frequency range	Vcc = 1.5V	16	–	320	MHz
Pre-divider output clock frequency range	Vcc = 1.5V	16	–	32	MHz
Double clock frequency range	Vcc = 1.5V	220	–	560	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Frequency lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	350	400	450	T_{ref}
Frequency lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	280	330	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	480	530	580	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	360	410	460	T_{ref}
Frequency jitter (p-p)	–	–	0.02	0.03	$2 \bullet T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.7V	–	1.0	1.5	ns
Power dissipation	FOL mode, integer MF, f_{dck} = 560 MHz, Vcc = 1.5V	–	1.5	–	mW (Avg)

3.10 Smart LCD Controller

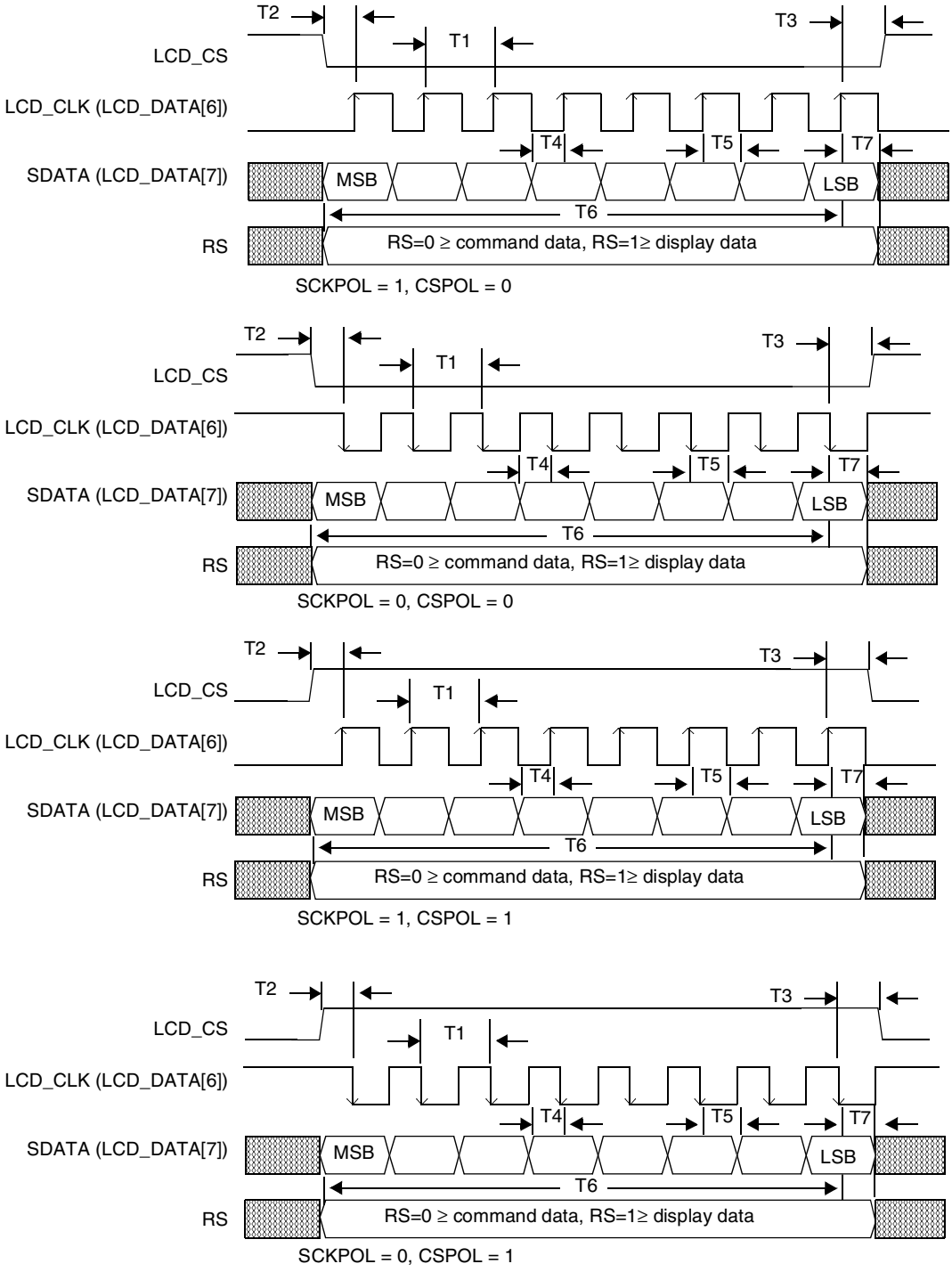


Figure 15. SLCDC Serial Transfer Timing

3.12 External Memory Interface (EMI) Electricals

3.12.1 NAND-Flash Controller (NFC) Interface

Figure 25, Figure 26, Figure 27, and Figure 28 depict the relative timing requirements among different signals of the NFC at module level, and Table 24 lists the timing parameters. The NAND Flash Controller (NFC) timing parameters are based on the internal NFC clock generated by the Clock Controller module, where time T is the period of the NFC clock in ns. Per the i.MX21S Reference Manual, specifically the *Phase-Locked (PLL), Clock, and Reset Controller* chapter, the NFC clock is derived from the same clock which drives the CPU clock (FCLK) that is fed through the NFCDIV block to generate the NFC clock. The relationship between the NFC clock and the external timing parameters of the NFC is provided in Table 24.

Table 24 also provides two examples of external timing parameters with NFC clock frequencies of 22.17 MHz and 33.25 MHz. For example, assuming a 266 MHz FCLK (CPU clock), NFCDIV should be set to divide-by-12 to generate a 22.17 MHz NFC clock and divide-by-8 to generate a 33.25 MHz NFC clock. The user should compare the parameters of the selected NAND Flash memory with the NFC external timing parameters to determine the proper NFC clock. *The maximum NFC clock allowed is 66 MHz*. It should also be noted that the default NFC clock on power up is 16.63 MHz.

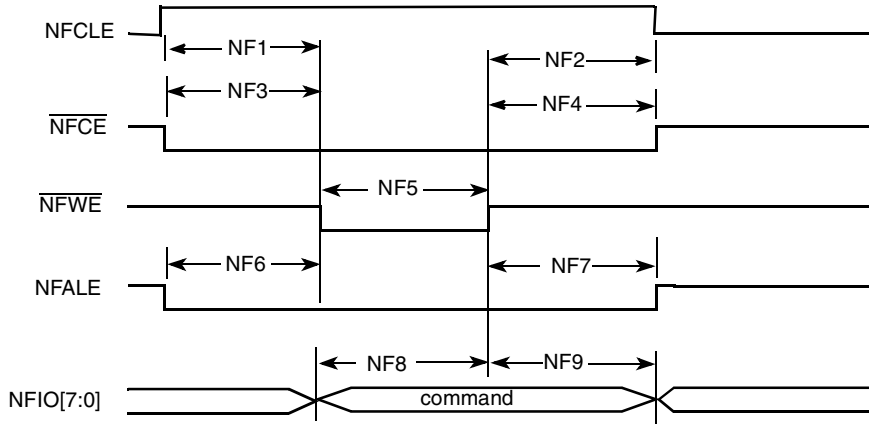


Figure 25. Command Latch Cycle Timing Diagram

3.13 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

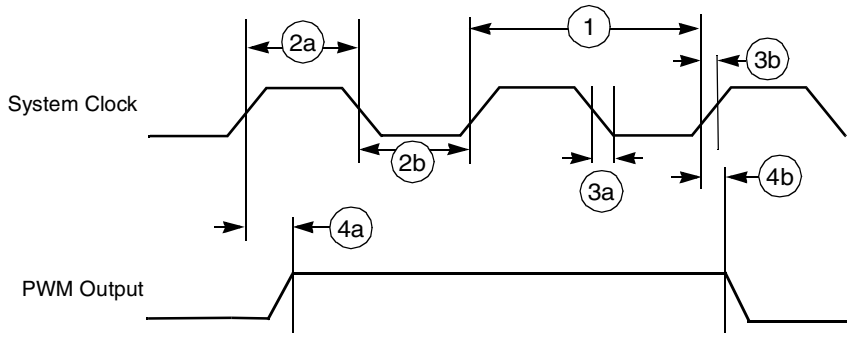


Figure 29. PWM Output Timing Diagram

Table 25. PWM Output Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	45	0	45	MHz
2a	Clock high time[1]	12.29	–	12.29	–	ns
2b	Clock low time[1]	9.91	–	9.91	–	ns
3a	Clock fall time[1]	–	0.5	–	0.5	ns
3b	Clock rise time[1]	–	0.5	–	0.5	ns
4a	Output delay time[1]	9.37	–	3.61	–	ns
4b	Output setup time[1]	8.71	–	3.03	–	ns

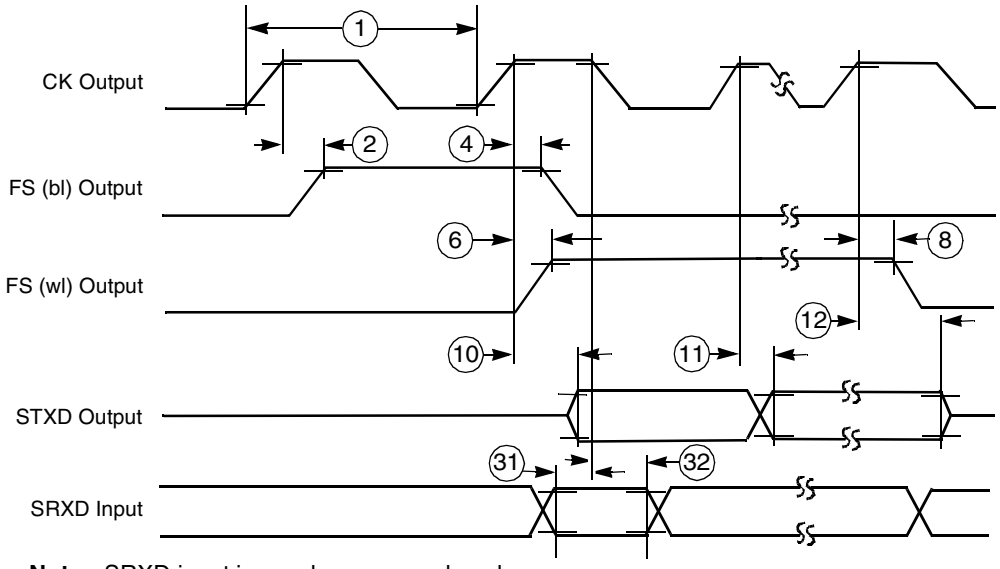
1. C_L of PWMO = TBD

3.15 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 34 through Figure 37.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.

The SSI can be connected to 4 set of ports, SAP, SSI1, SSI2 and SSI3.



Note: SRXD input in synchronous mode only.

Figure 34. SSI Transmitter Internal Clock Timing Diagram

Table 30. SSI to SSI1 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
20	(Tx) CK high to FS (bl) low	10.22	17.63	8.82	16.24	ns
21	(Rx) CK high to FS (bl) low	10.79	19.67	9.39	18.28	ns
22	(Tx) CK high to FS (wl) high	10.22	17.63	8.82	16.24	ns
23	(Rx) CK high to FS (wl) high	10.79	19.67	9.39	18.28	ns
24	(Tx) CK high to FS (wl) low	10.22	17.63	8.82	16.24	ns
25	(Rx) CK high to FS (wl) low	10.79	19.67	9.39	18.28	ns
26	(Tx) CK high to STXD valid from high impedance	10.05	15.75	8.66	14.36	ns
27a	(Tx) CK high to STXD high	10.00	15.63	8.61	14.24	ns
27b	(Tx) CK high to STXD low	10.00	15.63	8.61	14.24	ns
28	(Tx) CK high to STXD high impedance	10.05	15.75	8.66	14.36	ns
29	SRXD setup time before (Rx) CK low	0.78	–	0.47	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI1 Ports)						
31	SRXD setup before (Tx) CK falling	19.90	–	19.90	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI1 Ports)						
33	SRXD setup before (Tx) CK falling	2.59	–	2.28	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 31. SSI to SSI2 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI2 Ports)						
1	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	0.01	0.15	0.01	0.15	ns
3	(Rx) CK high to FS (bl) high	-0.21	0.05	-0.21	0.05	ns
4	(Tx) CK high to FS (bl) low	0.01	0.15	0.01	0.15	ns
5	(Rx) CK high to FS (bl) low	-0.21	0.05	-0.21	0.05	ns
6	(Tx) CK high to FS (wl) high	0.01	0.15	0.01	0.15	ns
7	(Rx) CK high to FS (wl) high	-0.21	0.05	-0.21	0.05	ns
8	(Tx) CK high to FS (wl) low	0.01	0.15	0.01	0.15	ns
9	(Rx) CK high to FS (wl) low	-0.21	0.05	-0.21	0.05	ns
10	(Tx) CK high to STXD valid from high impedance	0.34	0.72	0.34	0.72	ns

Table 32. SSI to SSI3 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI3 Ports)						
1	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	-2.09	-0.66	-2.09	-0.66	ns
3	(Rx) CK high to FS (bl) high	-2.74	-0.84	-2.74	-0.84	ns
4	(Tx) CK high to FS (bl) low	-2.09	-0.66	-2.09	-0.66	ns
5	(Rx) CK high to FS (bl) low	-2.74	-0.84	-2.74	-0.84	ns
6	(Tx) CK high to FS (wl) high	-2.09	-0.66	-2.09	-0.66	ns
7	(Rx) CK high to FS (wl) high	-2.74	-0.84	-2.74	-0.84	ns
8	(Tx) CK high to FS (wl) low	-2.09	-0.66	-2.09	-0.66	ns
9	(Rx) CK high to FS (wl) low	-2.74	-0.84	-2.74	-0.84	ns
10	(Tx) CK high to STXD valid from high impedance	-1.73	-0.26	-1.73	-0.26	ns
11a	(Tx) CK high to STXD high	-2.87	-0.80	-2.87	-0.80	ns
11b	(Tx) CK high to STXD low	-2.87	-0.80	-2.87	-0.80	ns
12	(Tx) CK high to STXD high impedance	-1.73	-0.26	-1.73	-0.26	ns
13	SRXD setup time before (Rx) CK low	22.77	–	22.77	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI3 Ports)						
15	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	9.62	17.10	7.90	15.61	ns
19	(Rx) CK high to FS (bl) high	10.30	19.54	8.58	18.05	ns
20	(Tx) CK high to FS (bl) low	9.62	17.10	7.90	15.61	ns
21	(Rx) CK high to FS (bl) low	10.30	19.54	8.58	18.05	ns
22	(Tx) CK high to FS (wl) high	9.62	17.10	7.90	15.61	ns
23	(Rx) CK high to FS (wl) high	10.30	19.54	8.58	18.05	ns
24	(Tx) CK high to FS (wl) low	9.62	17.10	7.90	15.61	ns
25	(Rx) CK high to FS (wl) low	10.30	19.54	8.58	18.05	ns
26	(Tx) CK high to STXD valid from high impedance	9.02	16.46	7.29	14.97	ns
27a	(Tx) CK high to STXD high	8.48	15.32	6.75	13.83	ns
27b	(Tx) CK high to STXD low	8.48	15.32	6.75	13.83	ns

Table 32. SSI to SSI3 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	(Tx) CK high to STXD high impedance	9.02	16.46	7.29	14.97	ns
29	SRXD setup time before (Rx) CK low	1.49	–	1.49	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI3 Ports)						
31	SRXD setup before (Tx) CK falling	21.99	–	21.99	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI3 Ports)						
33	SRXD setup before (Tx) CK falling	3.80	–	3.80	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

3.16 1-Wire Interface Timing

3.16.1 Reset Sequence with Reset Pulse Presence Pulse

To begin any communications with the DS2502, it is required that an initialization procedure be issued. A reset pulse must be generated and then a presence pulse must be detected. The minimum reset pulse length is 480 us. The bus master (one-wire) will generate this pulse, then after the DS2502 detects a rising edge on the one-wire bus, it will wait 15-60 us before it will transmit back a presence pulse. The presence pulse will exist for 60-240 us.

The timing diagram for this sequence is shown in Figure 38.

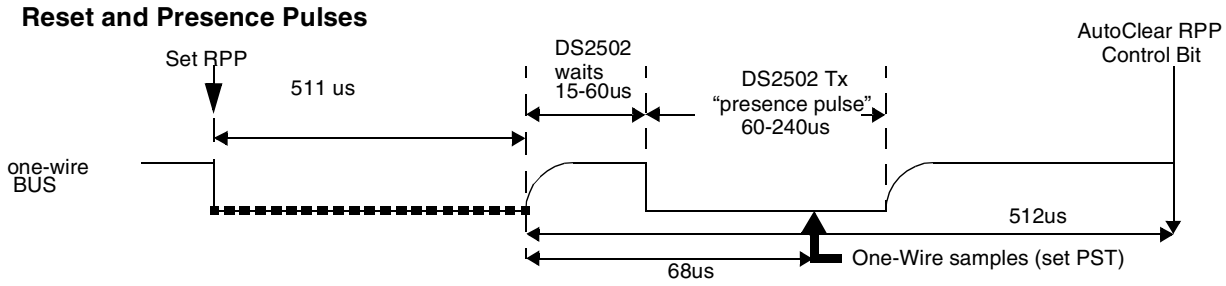


Figure 38. 1-Wire Initialization

The reset pulse begins the initialization sequence and it is initiated when the RPP control register bit is set. When the presence pulse is detected, this bit will be cleared. The presence pulse is used by the bus master to determine if at least one DS2502 is connected. Software will determine if more than one DS2502 exists. The one-wire will sample for the DS2502 presence pulse. The presence pulse is latched in the one-wire

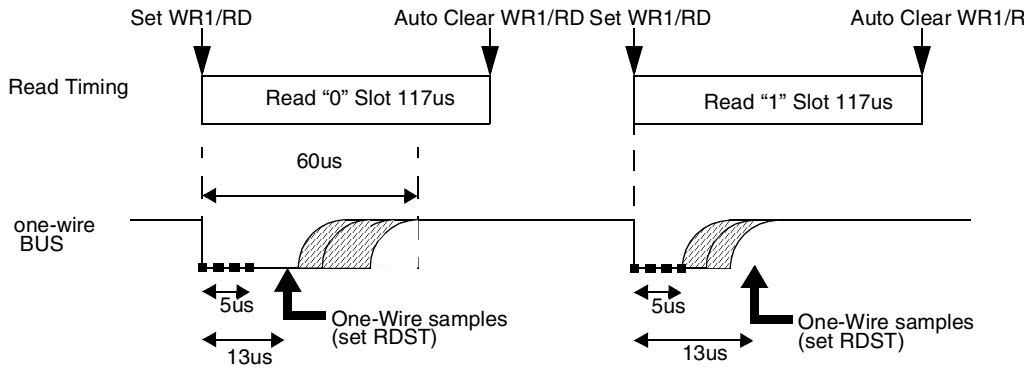


Figure 41. Read Timing

The precision of the generated clock is very important to get a proper behavior of the one-wire module. This module is based on a state machine which undertakes actions at defined times.

Table 33. System Timing Requirements

Times	Values (Microsec)	Minimum (Microsec)	Maximum (microsec)	Absolute Precision	Relative Precision
RSTL	511	480	–	31	0.0645
PST	68	60	75	7	0.1
RSTH	512	480	–	32	0.0645
LOW0	100	60	120	20	0.2
LOWR	5	1	15	4	0.8
READ_sample	13	–	15	2	0.15

The most stringent constraint is 0.0645 as a relative time imprecision.

The time relative precision is directly derived from the frequency of the derivative clock (f):

Time relative precision = 1/f -1 = divider/clock (MHz) - 1

The Figure 34 gathers relative time precision for different main clock frequencies.

Table 34. System Clock Requirements

Main Clock Frequency (MHz)	13	16.8	19.44
Clock divide ratio	13	17	19
Generated frequency (MHz)	1	0.9882	1.023
Relative time imprecision	0	0.0117	0.023

This shows that the user should take care of the main clock frequency when using the one-wire module. If the main clock is an exact integer multiple of 1 MHz, then the generated frequency will be exactly 1 MHz.

NOTE:

A main clock frequency below 10 MHz might cause a misbehavior of the module.

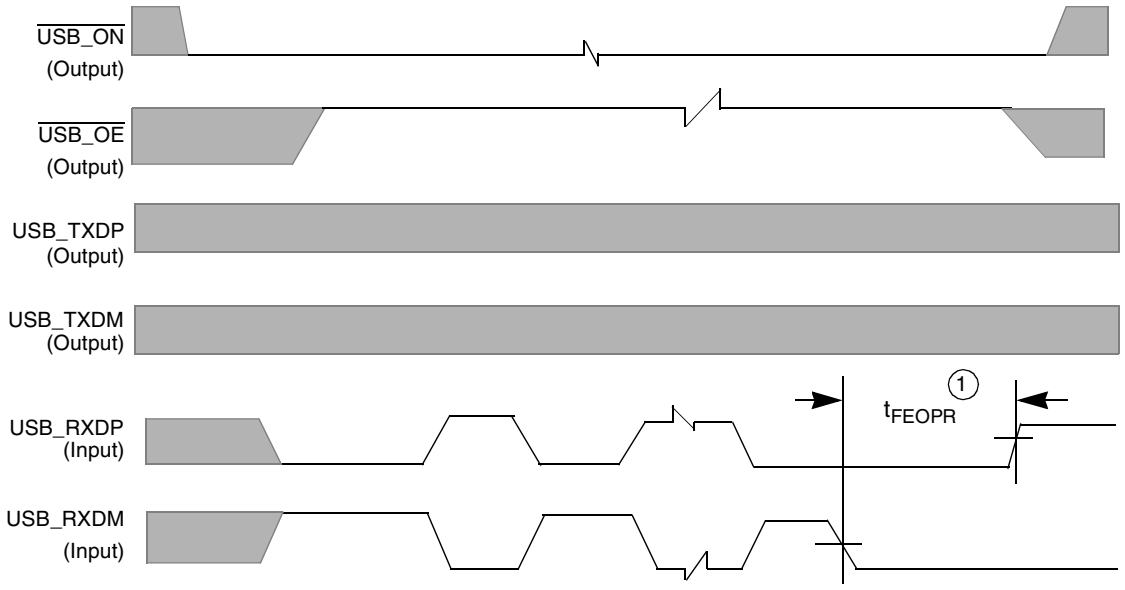


Figure 43. USB Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 36. USB Timing Parameters for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{FEOPR}; Receiver SE0 interval of EOP	82	–	ns

The USBOTG I^2C communication protocol consists of six components: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

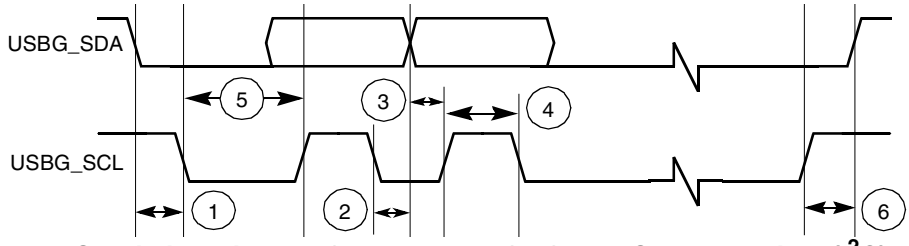


Figure 44. USB Timing Diagram for Data Transfer from USB Transceiver (I^2C)

Table 37. USB Timing Parameters for Data Transfer from USB Transceiver (I^2C)

Ref No.	Parameter	1.8 V ± 0.1 V		Unit
		Minimum	Maximum	
1	Hold time (repeated) START condition	188	–	ns
2	$\overline{\text{Data hold time}}$	0	188	ns
3	Data setup time	88	–	ns
4	HIGH period of the SCL clock	500	–	ns
5	LOW period of the SCL clock	500	–	ns
6	Setup time for STOP condition	185	–	ns

Note: Signals listed with lower case letters are internal to the device.

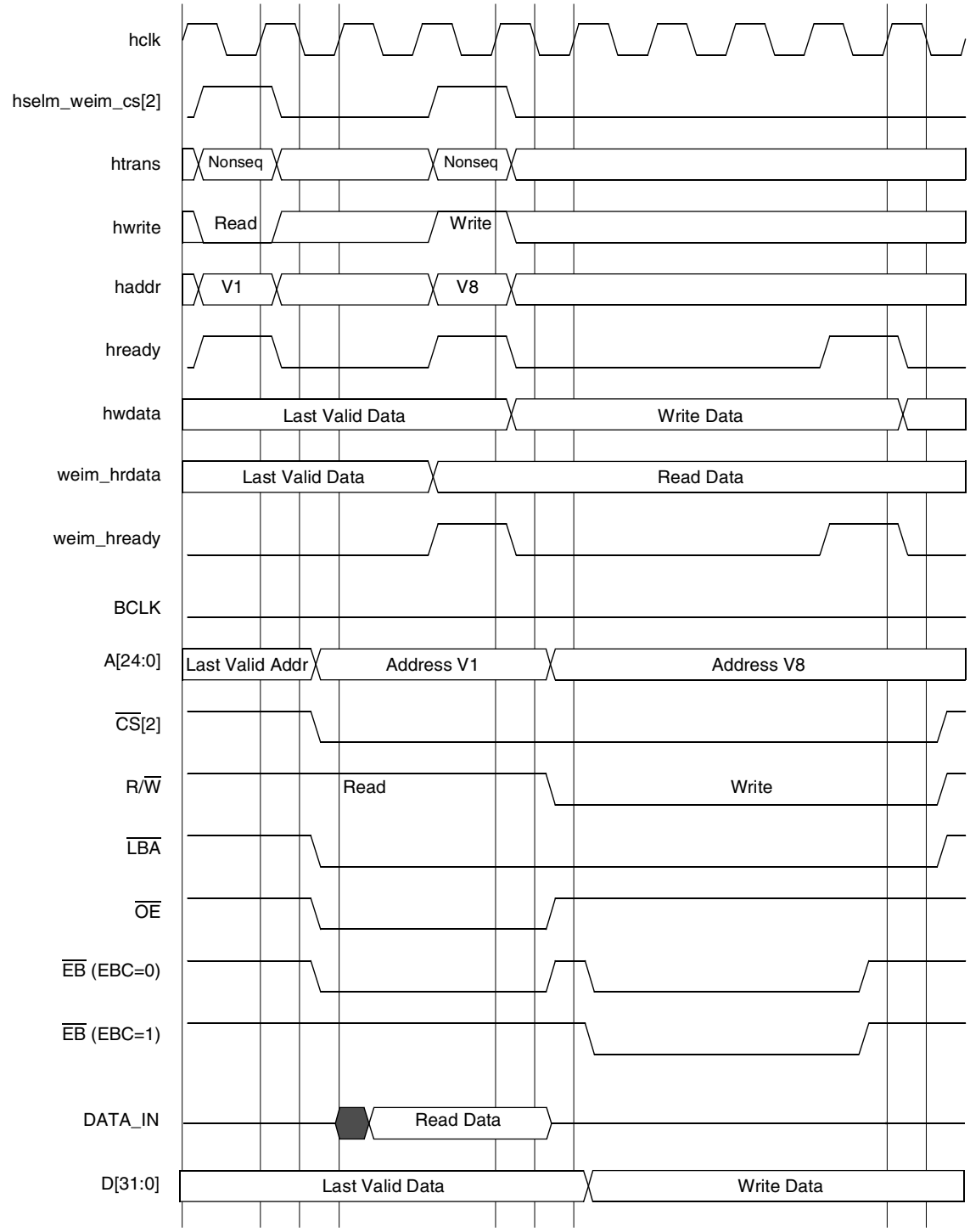


Figure 58. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

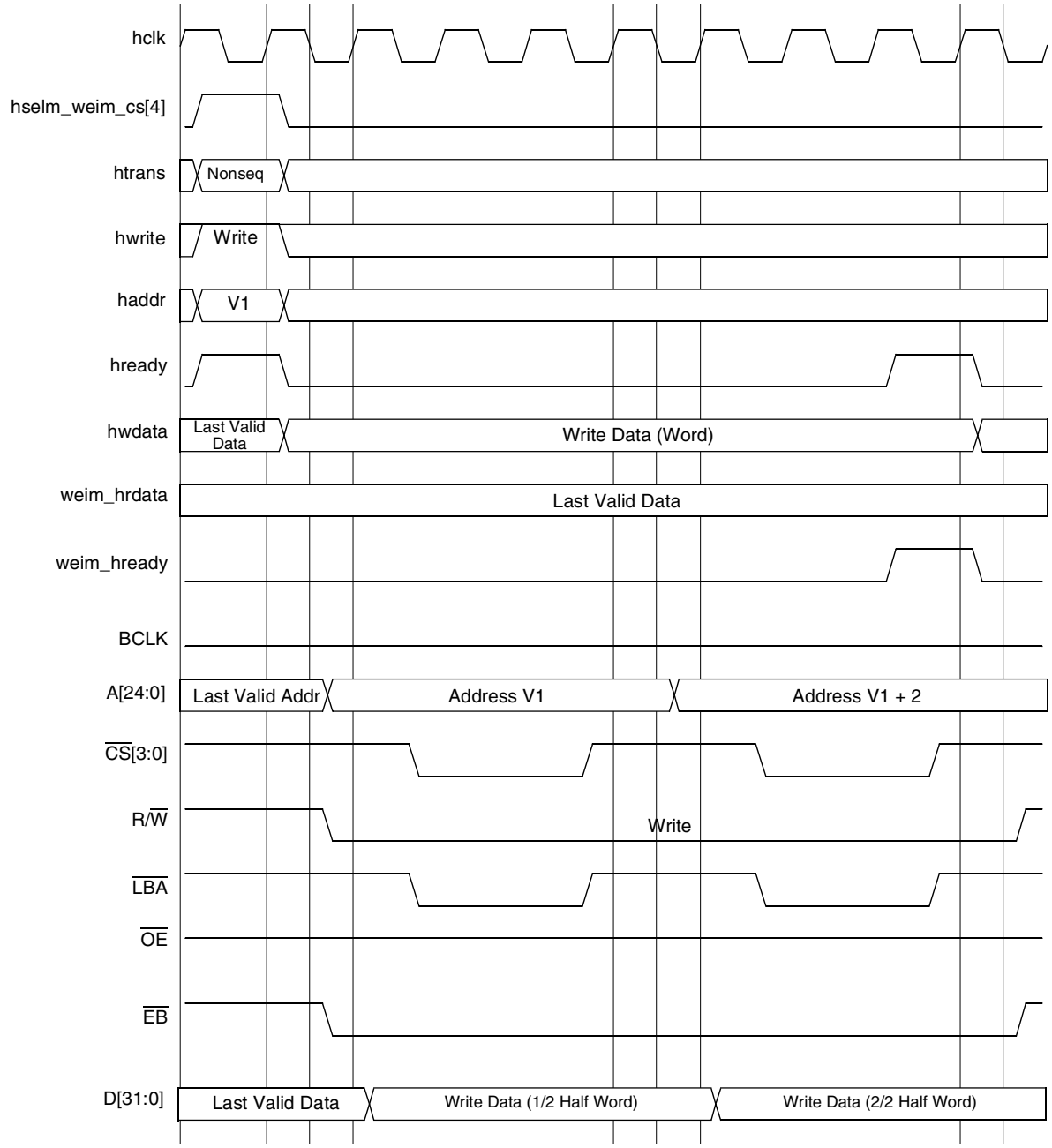


Figure 60. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

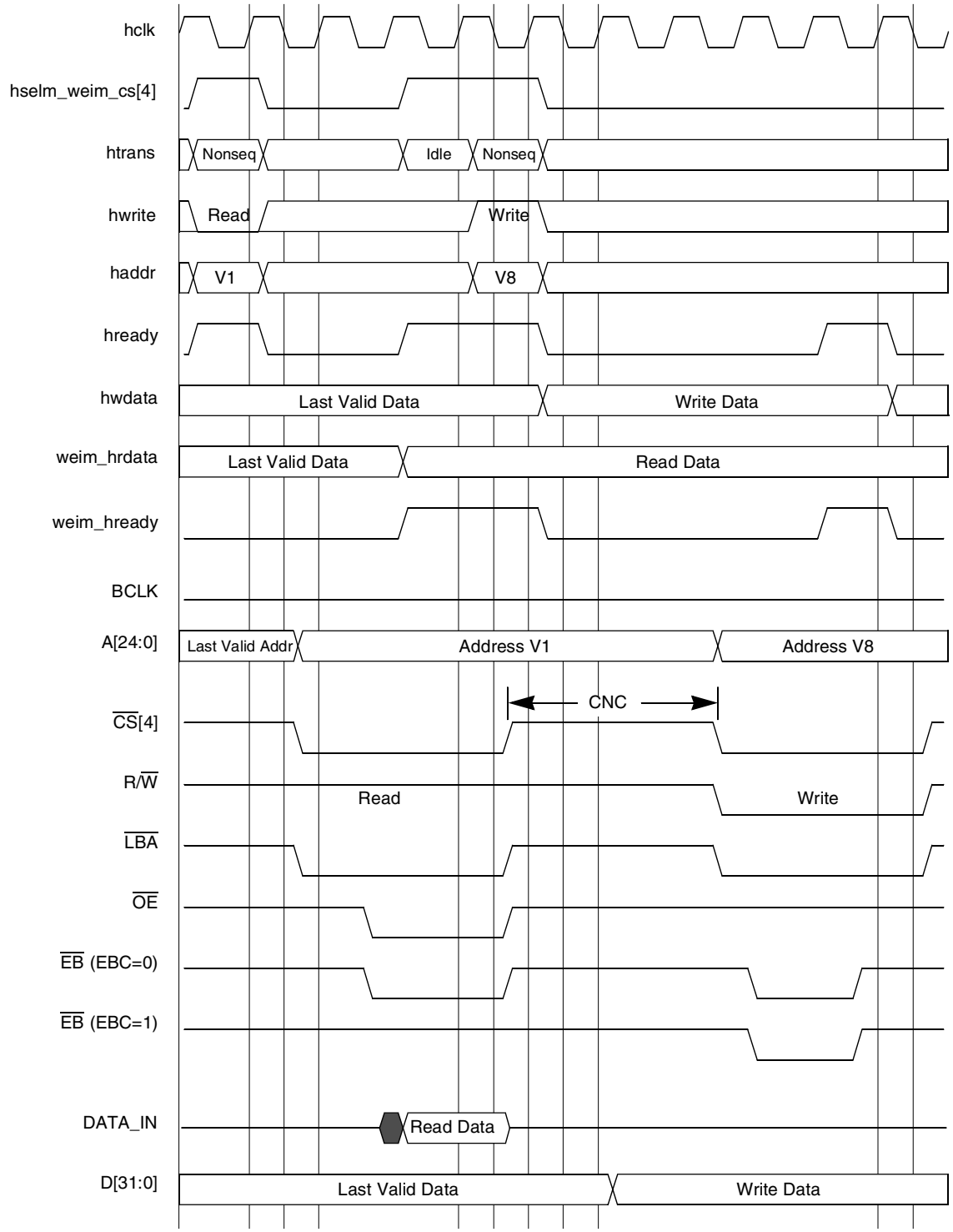


Figure 63. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

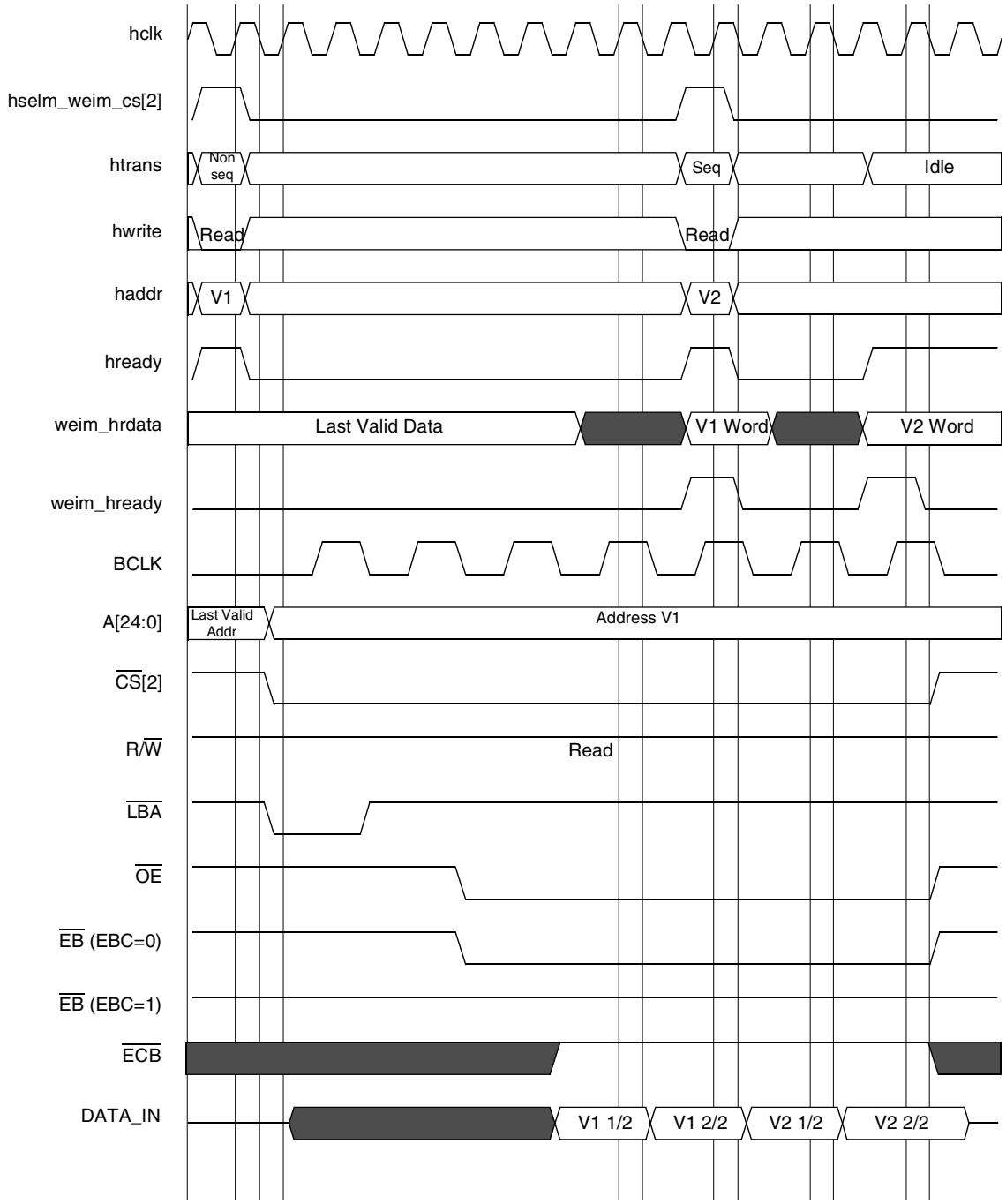
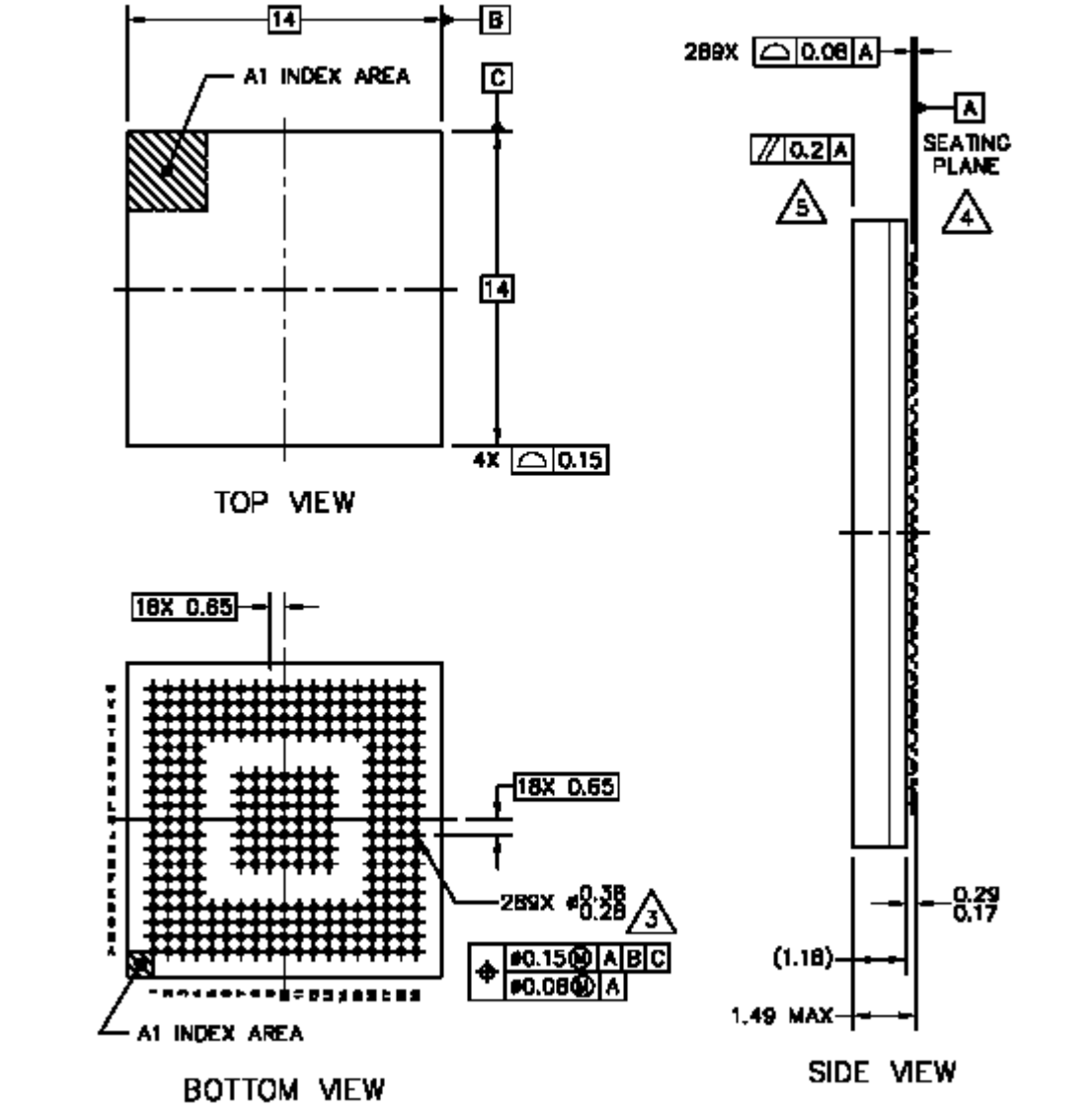


Figure 68. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

4.1 MAPBGA Package Dimensions

Figure 73 illustrates the MAPBGA 14 mm × 14 mm × 1.41 mm package, which has 0.65 mm ball pitch.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 73. i.MX21 MAPBGA Mechanical Drawing