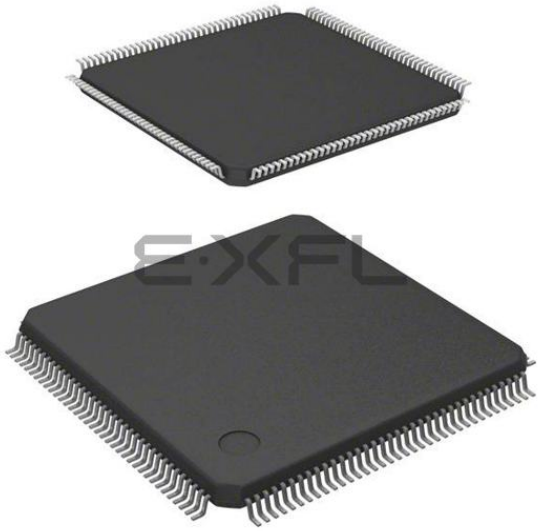

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f271z1t3

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4 Memory organization

The memory space of the ST10F271Z1 is configured in a unified memory architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16 Mbytes. The entire memory space can be accessed Byte wise or Word wise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

IFlash: 128 Kbytes of on-chip Flash memory. It is divided in 6 blocks (B0F0...B0F5) that constitute the Bank 0. When Bootstrap mode is selected, the Test-Flash Block B0TF (8 Kbyte) appears at address 00'0000h: refer to *Chapter 5: Internal Flash memory on page 24* for more details on memory mapping in boot mode. The summary of address range for IFlash is the following:

Table 2. Summary of IFlash address range

Blocks	User mode	Size
B0TF	Not visible	8K
B0F0	00'0000h - 00'1FFFh	8K
B0F1	00'2000h - 00'3FFFh	8K
B0F2	00'4000h - 00'5FFFh	8K
B0F3	00'6000h - 00'7FFFh	8K
B0F4	01'8000h - 01'FFFFh	32K
B0F5	02'0000h - 02'FFFFh	64K
Reserved (1)	*03'0000h - 03'FFFFh / RESERVED*	*64K*
Reserved (1)	*04'0000h - 04'FFFFh / RESERVED*	*64K*

(1) This area must be reserved by the application mapping.

IRAM: 2 Kbytes of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 Wordwide (R0 to R15) and / or Bytewide (RL0, RH0, …, RL7, RH7) general purpose registers group.

XRAM: 8K+2 Kbytes of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.

The XRAM is divided into 2 areas, the first 2 Kbytes named XRAM1 and the second 8 Kbytes named XRAM2, connected to the internal XBUS and are accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read/write delay (31.25ns access at 64MHz CPU clock). Byte and Word accesses are allowed.

The XRAM1 address range is 00'E000h - 00'E7FFh if XPEN (bit 2 of SYSCON register), and XRAM1EN (bit 2 of XPERCON register) are set. If XRAM1EN or XPEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.

The XRAM2 address range is the one selected programming XADRS3 register, if XPEN (bit 2 of SYSCON register), and XRAM2EN (bit 3 of XPERCON register) are set. If bit XPEN is cleared, then any access in the address range programmed for XRAM2 will be directed to

5.4.4 Flash control register 1 high

The Flash Control Register 1 High (FCR1H), together with Flash Control Register 1 Low (FCR1L), is used to select the Sectors to Erase, or during any write operation to monitor the status of each Sector and Bank.

FCR1H (0x08 0006) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved							B0S	reserved							
							RS								

Table 10. Flash control register 1 high

Bit	Function
B0S	Bank 0 Status (IFlash) During any erase operation, this bit is automatically modified and gives the status of the Bank 0. The meaning of B0S bit is given in the next Table 4 Banks (BxS) and Sectors (BxFy) Status bits meaning. This bit is automatically reset at the end of a erase operation if no errors are detected.

During any erase operation, this bit is automatically set and gives the status of the Bank 0. The meaning of B0Fy bit for Sector y of Bank 0 is given by the next Table 4 Banks (BxS) and Sectors (BxFy) Status bits meaning. These bits are automatically reset at the end of an erase operation if no errors are detected.

Table 11. Banks (BxS) and sectors (BxFy) status bits meaning

ERR	SUSP	B0S = 1 meaning	B0Fy = 1 meaning
1	-	Erase error in Bank 0	Erase error in sector y of Bank 0
0	1	Erase suspended in Bank 0	Erase suspended in sector y of Bank 0
0	0	Don't care	Don't care

5.4.5 Flash data register 0 low

The Flash Address Registers (FARH/L) and the Flash Data Registers (FDR1H/L-FDR0H/L) are used during the program operations to store Flash Address in which to program and Data to program.

FDR0L (0x08 0008) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 24. Flash write operations

Operation	Select bit	Address and data	Start bit
Word program (32-bit)	WPG	FARL/FARH FDR0L/FDR0H	WMS
Double word program (64-bit)	DWPG	FARL/FARH FDR0L/FDR0H FDR1L/FDR1H	WMS
Sector erase	SER	FCR1L/FCR1H	WMS
Set protection	SPR	FDR0L/FDR0H	WMS
Program/erase suspend	SUSP	None	None

Table 26. Standard instruction set summary (continued)

Mnemonic	Description	Bytes
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software reset	4
IDLE	Enter Idle mode	4
PWRDN	Enter power-down mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service watchdog timer	4
DISWDT	Disable watchdog timer	4
EINIT	Signify end-of-initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended register sequence	2
EXTP(R)	Begin EXTended page (and register) sequence	2 / 4
EXTS(R)	Begin EXTended segment (and register) sequence	2 / 4
NOP	Null operation	2

7.3 MAC co-processor specific instructions

The *Table 27* lists the MAC instructions of the ST10F271Z1. The detailed description of each instruction can be found in the “ST10 Family Programming Manual”. Note that all MAC instructions are encoded on 4 Bytes.

Table 27. MAC instruction set summary

Mnemonic	Description
CoABS	Absolute value of the accumulator
CoADD(2)	Addition
CoASHR(rnd)	Accumulator arithmetic shift right & optional round
CoCMP	Compare accumulator with operands

Table 28. Interrupt sources (continued)

Source of interrupt or PEC service request	Request flag	Enable flag	Interrupt vector	Vector location	Trap number
CAPCOM register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h
CAPCOM register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 timer 5	T5IR	T5IE	T5INT	00'0094h	25h

20 System reset

System reset initializes the MCU in a predefined state. There are six ways to activate a reset state. The system start-up configuration is different for each case as shown in *Table 48*.

Table 48. Reset event definition

Reset source	Flag	RPD status	Conditions
Power-on reset	PONR	Low	Power-on
Asynchronous hardware reset	LHWR	Low	$t_{\overline{RSTIN}}$ > [1]
Synchronous long hardware reset		High	$t_{\overline{RSTIN}}$ > (1032 + 12) TCL + max(4 TCL, 500 ns)
Synchronous short hardware reset	SHWR	High	$t_{\overline{RSTIN}}$ > max(4 TCL, 500 ns) $t_{\overline{RSTIN}}$ ≤ (1032 + 12) TCL + max(4 TCL, 500 ns)
Watchdog timer reset	WDTR	[3]	WDT overflow
Software reset	SWR	[3]	SRST instruction execution

1) $\overline{RSTIN}$ pulse should be longer than 500ns (Filter) and than settling time for configuration of Port0.

2) See next *Section 20.1* for more details on minimum reset pulse duration.

3) The RPD status has no influence unless Bidirectional Reset is activated (bit BDRSTEN in SYSCON): RPD low inhibits the Bidirectional reset on SW and WDT reset events, that is $\overline{RSTIN}$ is not activated (refer to Sections *20.4*, *20.5* and *20.6*).

20.1 Input filter

On $\overline{RSTIN}$ input pin an on-chip RC filter is implemented. It is sized to filter all the spikes shorter than 50 ns. On the other side, a valid pulse shall be longer than 500 ns to grant that ST10 recognizes a reset command. In between 50 ns and 500 ns a pulse can either be filtered or recognized as valid, depending on the operating conditions and process variations.

For this reason all minimum durations mentioned in this Chapter for the different kind of reset events shall be carefully evaluated taking into account of the above requirements.

In particular, for Short Hardware Reset, where only 4 TCL is specified as minimum input reset pulse duration, the operating frequency is a key factor. Examples:

- For a CPU clock of 64 MHz, 4 TCL is 31.25 ns, so it would be filtered. In this case the minimum becomes the one imposed by the filter (that is 500 ns).
- For a CPU clock of 4 MHz, 4 TCL is 500 ns. In this case the minimum from the formula is coherent with the limit imposed by the filter.

20.2 Asynchronous reset

An asynchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while RPD pin is at low level. Then the ST10F271Z1 is immediately (after the input filter delay) forced in reset default state. It pulls low $\overline{RSTOUT}$ pin, it cancels pending internal hold states if any, it aborts

V_{18} and ground: the internal 1.8V drivers are sized to drive currents of several tens of Ampere, so the current shall be limited by the external hardware. The limit of current is imposed by power dissipation considerations (Refer to Electrical Characteristics Section).

In next Figures *17* and *18* Asynchronous Power-on timing diagrams are reported, respectively with boot from internal or external memory, highlighting the reset phase extension introduced by the embedded Flash module when selected.

Note: Never power the device without keeping $\overline{RSTIN}$ pin grounded: the device could enter in unpredictable states, risking also permanent damages.

Figure 17. Asynchronous power-on RESET ($\overline{EA}$ = 1)

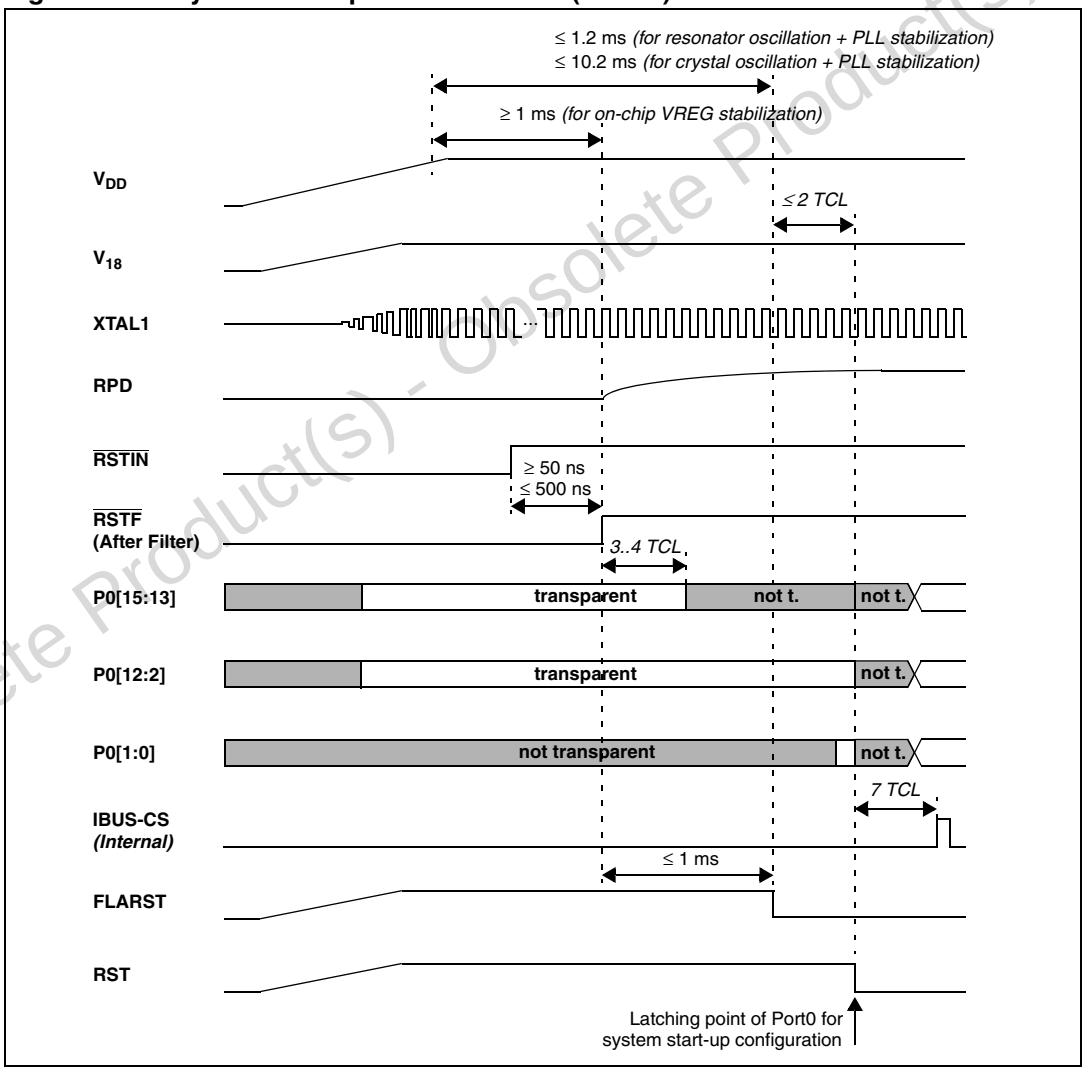


Table 51. Power reduction modes summary

Mode	V_{DD}	V_{STBY}	CPU	Peripherals	RTC	Main OSC	32 kHz OSC	STBY XRAM	XRAM
Idle	on	on	off	on	off	run	off	biased	biased
	on	on	off	on	on	run	on	biased	biased
Power-down	on	on	off	off	off	off	off	biased	biased
	on	on	off	off	on	on	off	biased	biased
	on	on	off	off	on	off	on	biased	biased
Stand-by	off	on	off	off	off	off	off	biased	off
	off	on	off	off	on	off	on	biased	off

Table 52. List of special function registers (continued)

Name		Physical address		8-bit address	Description	Reset value
ODP7	b	F1D2h	E	E9h	Port 7 open drain control register	- - 00h
ODP8	b	F1D6h	E	EBh	Port 8 open drain control register	- - 00h
ONES	b	FF1Eh		8Fh	Constant value 1's register (read only)	FFFFh
P0L	b	FF00h		80h	PORT0 low register (lower half of PORT0)	- - 00h
P0H	b	FF02h		81h	PORT0 high register (upper half of PORT0)	- - 00h
P1L	b	FF04h		82h	PORT1 low register (lower half of PORT1)	- - 00h
P1H	b	FF06h		83h	PORT1 high register (upper half of PORT1)	- - 00h
P2	b	FFC0h		E0h	Port 2 register	0000h
P3	b	FFC4h		E2h	Port 3 register	0000h
P4	b	FFC8h		E4h	Port 4 register (8-bit)	- - 00h
P5	b	FFA2h		D1h	Port 5 register (read only)	XXXXh
P6	b	FFCCh		E6h	Port 6 register (8-bit)	- - 00h
P7	b	FFD0h		E8h	Port 7 register (8-bit)	- - 00h
P8	b	FFD4h		EAh	Port 8 register (8-bit)	- - 00h
P5DIDIS	b	FFA4h		D2h	Port 5 digital disable register	0000h
PECC0		FEC0h		60h	PEC channel 0 control register	0000h
PECC1		FEC2h		61h	PEC channel 1 control register	0000h
PECC2		FEC4h		62h	PEC channel 2 control register	0000h
PECC3		FEC6h		63h	PEC channel 3 control register	0000h
PECC4		FEC8h		64h	PEC channel 4 control register	0000h
PECC5		FECAh		65h	PEC channel 5 control register	0000h
PECC6		FECCh		66h	PEC channel 6 control register	0000h
PECC7		FECEh		67h	PEC channel 7 control register	0000h
PICON	b	F1C4h	E	E2h	Port input threshold control register	- - 00h
PP0		F038h	E	1Ch	PWM module period register 0	0000h
PP1		F03Ah	E	1Dh	PWM module period register 1	0000h
PP2		F03Ch	E	1Eh	PWM module period register 2	0000h
PP3		F03Eh	E	1Fh	PWM module period register 3	0000h
PSW	b	FF10h		88h	CPU program status word	0000h
PT0		F030h	E	18h	PWM module up/down counter 0	0000h
PT1		F032h	E	19h	PWM module up/down counter 1	0000h
PT2		F034h	E	1Ah	PWM module up/down counter 2	0000h
PT3		F036h	E	1Bh	PWM module up/down counter 3	0000h
PW0		FE30h		18h	PWM module pulse width register 0	0000h

Table 52. List of special function registers (continued)

Name		Physical address		8-bit address	Description	Reset value
T1		FE52h		29h	CAPCOM timer 1 register	0000h
T1IC	b	FF9Eh		CFh	CAPCOM timer 1 interrupt control register	- - 00h
T1REL		FE56h		2Bh	CAPCOM timer 1 reload register	0000h
T2		FE40h		20h	GPT1 timer 2 register	0000h
T2CON	b	FF40h		A0h	GPT1 timer 2 control register	0000h
T2IC	b	FF60h		B0h	GPT1 timer 2 interrupt control register	- - 00h
T3		FE42h		21h	GPT1 timer 3 register	0000h
T3CON	b	FF42h		A1h	GPT1 timer 3 control register	0000h
T3IC	b	FF62h		B1h	GPT1 timer 3 interrupt control register	- - 00h
T4		FE44h		22h	GPT1 timer 4 register	0000h
T4CON	b	FF44h		A2h	GPT1 timer 4 control register	0000h
T4IC	b	FF64h		B2h	GPT1 timer 4 interrupt control register	- - 00h
T5		FE46h		23h	GPT2 timer 5 register	0000h
T5CON	b	FF46h		A3h	GPT2 timer 5 control register	0000h
T5IC	b	FF66h		B3h	GPT2 timer 5 interrupt control register	- - 00h
T6		FE48h		24h	GPT2 timer 6 register	0000h
T6CON	b	FF48h		A4h	GPT2 timer 6 control register	0000h
T6IC	b	FF68h		B4h	GPT2 timer 6 interrupt control register	- - 00h
T7		F050h	E	28h	CAPCOM timer 7 register	0000h
T78CON	b	FF20h		90h	CAPCOM timer 7 and 8 control register	0000h
T7IC	b	F17Ah	E	BDh	CAPCOM timer 7 interrupt control register	- - 00h
T7REL		F054h	E	2Ah	CAPCOM timer 7 reload register	0000h
T8		F052h	E	29h	CAPCOM timer 8 register	0000h
T8IC	b	F17Ch	E	BEh	CAPCOM timer 8 interrupt control register	- - 00h
T8REL		F056h	E	2Bh	CAPCOM timer 8 reload register	0000h
TFR	b	FFACh		D6h	Trap Flag register	0000h
WDT		FEAEh		57h	Watchdog timer register (read only)	0000h
WDTCON	b	FFAEh		D7h	Watchdog timer control register	00xxh [2]
XADRS3		F01Ch	E	0Eh	XPER address select register 3	800Bh
XP0IC	b	F186h	E	C3h	See *Section 9.1*	- - 00h [3]
XP1IC	b	F18Eh	E	C7h	See *Section 9.1*	- - 00h [3]
XP2IC	b	F196h	E	CBh	See *Section 9.1*	- - 00h [3]
XP3IC	b	F19Eh	E	CFh	See *Section 9.1*	- - 00h [3]

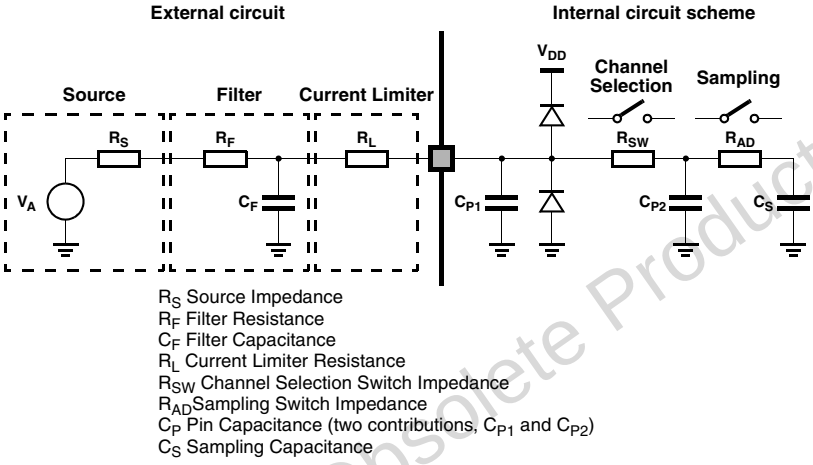
Table 64. DC characteristics (continued)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage READY (TTL only)	V_{IL3} **SR**	– 0.3	0.8	V	–
Input high voltage (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1)	V_{IH} **SR**	2.0	V_{DD} + 0.3	V	–
Input high voltage (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1)	V_{IHS} **SR**	0.7 V_{DD}	V_{DD} + 0.3	V	–
Input high voltage $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD	V_{IH1} **SR**	0.7 V_{DD}	V_{DD} + 0.3	V	–
Input high voltage XTAL1 (CMOS only)	V_{IH2} **SR**	0.7 V_{DD}	V_{DD} + 0.3	V	Direct Drive mode
Input high voltage READY (TTL only)	V_{IH3} **SR**	2.0	V_{DD} + 0.3	V	–
Input Hysteresis (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, XTAL1, RPD)	V_{HYS} **CC**	400	700	mV	(1)
Input Hysteresis (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, XTAL1, RPD)	V_{HYSS} **CC**	750	1400	mV	(1)
Input Hysteresis $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$	V_{HYS1} **CC**	750	1400	mV	(1)
Input Hysteresis XTAL1	V_{HYS2} **CC**	0	50	mV	(1)
Input Hysteresis READY (TTL only)	V_{HYS3} **CC**	400	700	mV	(1)
Input Hysteresis RPD	V_{HYS4} **CC**	500	1500	mV	(1)
Output low voltage (P6[7:0], ALE, $\overline{RD}$, $\overline{WR}$/$\overline{WRL}$, $\overline{BHE}$/$\overline{WRH}$, CLKOUT, $\overline{RSTIN}$, $\overline{RSTOUT}$)	V_{OL} **CC**	–	0.4 0.05	V	I_{OL} = 8 mA I_{OL} = 1 mA
Output low voltage (P0[15:0], P1[15:0], P2[15:0], P3[15,13:0], P4[7:0], P7[7:0], P8[7:0])	V_{OL1} **CC**	–	0.4 0.05	V	I_{OL1} = 4 mA I_{OL1} = 0.5 mA
Output low voltage RPD	V_{OL2} **CC**	–	V_{DD} 0.5 V_{DD} 0.3 V_{DD}	V	I_{OL2} = 85 µA I_{OL2} = 80 µA I_{OL2} = 60 µA
Output high voltage (P6[7:0], ALE, $\overline{RD}$, $\overline{WR}$/$\overline{WRL}$, $\overline{BHE}$/$\overline{WRH}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} **CC**	V_{DD} – 0.8 V_{DD} – 0.08	–	V	I_{OH} = – 8 mA I_{OH} = – 1 mA
Output high voltage (2) (P0[15:0], P1[15:0], P2[15:0], P3[15,13:0], P4[7:0], P7[7:0], P8[7:0])	V_{OH1} **CC**	V_{DD} – 0.8 V_{DD} – 0.08	–	V	I_{OH1} = – 4 mA I_{OH1} = – 0.5 mA
Output high voltage RPD	V_{OH2} **CC**	0 0.3 V_{DD} 0.5 V_{DD}	–	V	I_{OH2} = – 2 mA I_{OH2} = – 750 µA I_{OH2} = – 150 µA
Input leakage current (P5[15:0]) (3)	$\|I_{OZ1}\|$ **CC**	–	±0.2	µA	–
Input leakage current (all except P5[15:0], P2[0], RPD, P3[12], P3[15])	$\|I_{OZ2}\|$ **CC**	–	±0.5	µA	–

besides, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth).

Figure 43. A/D converter input pins scheme



Input leakage and external circuit

The series resistor utilized to limit the current to a pin (see R_L in *Figure 43*), in combination with a large source impedance can lead to a degradation of A/D converter accuracy when input leakage is present.

Data about maximum input leakage current at each pin are provided in the Data Sheet (Electrical Characteristics section). Input leakage is greatest at high operating temperatures, and in general it decreases by one half for each 10 °C decrease in temperature.

Considering that, for a 10-bit A/D converter one count is about 5mV (assuming V_{AREF} = 5 V), an input leakage of 100 nA acting though an R_L = 50 kΩ of external resistance leads to an error of exactly one count (5 mV); if the resistance were 100 kΩ the error would become two counts.

Eventual additional leakage due to external clamping diodes must also be taken into account in computing the total leakage affecting the A/D converter measurements. Another contribution to the total leakage is represented by the charge sharing effects with the sampling capacitance: being C_S substantially a switched capacitance, with a frequency equal to the conversion rate of a single channel (maximum when fixed channel continuous conversion mode is selected), it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 250 kHz, with C_S equal to 4 pF, a resistance of 1 MΩ is obtained ($R_{EQ} = 1 / f_C C_S$, where f_C represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the following relation:

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

R_L sizing is obtained:

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) \leq T_S$$

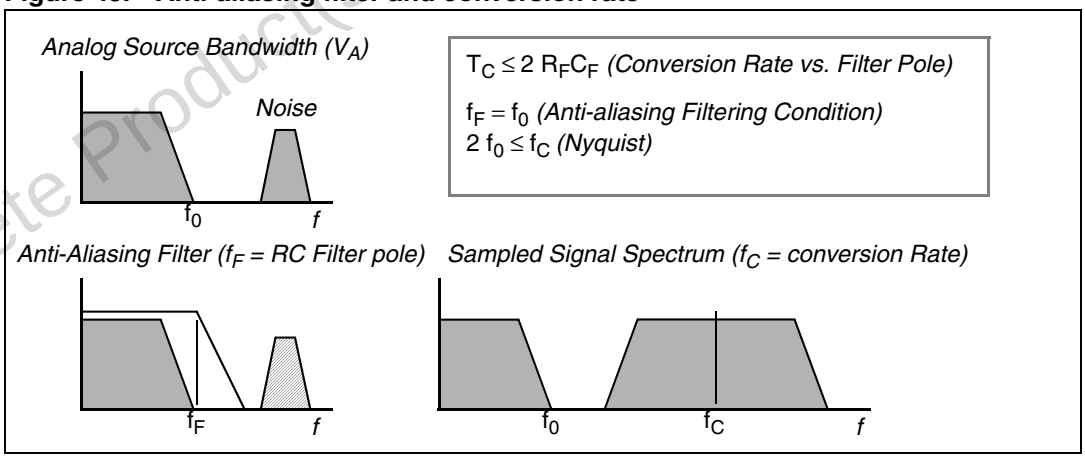
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. The following equation must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2}(C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1}(C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing (see *Figure 45*).

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

Figure 45. Anti-aliasing filter and conversion rate



The considerations above lead to impose new constraints to the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive the following relation between the ideal and real sampled voltage on C_S:

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

Figure 60. External memory cycle: demultiplexed bus, without r/w delay, extended ALE, r/w CS

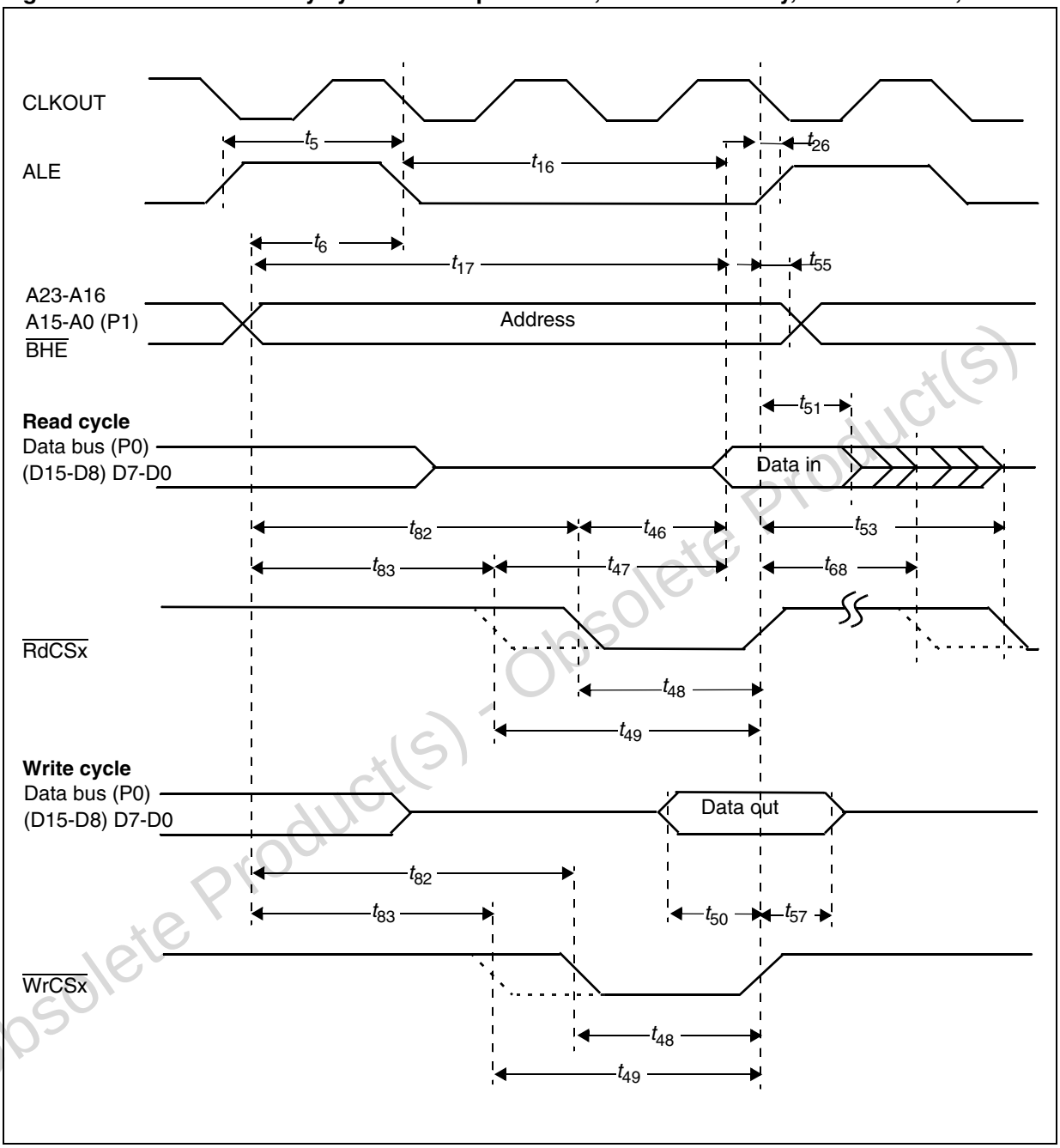
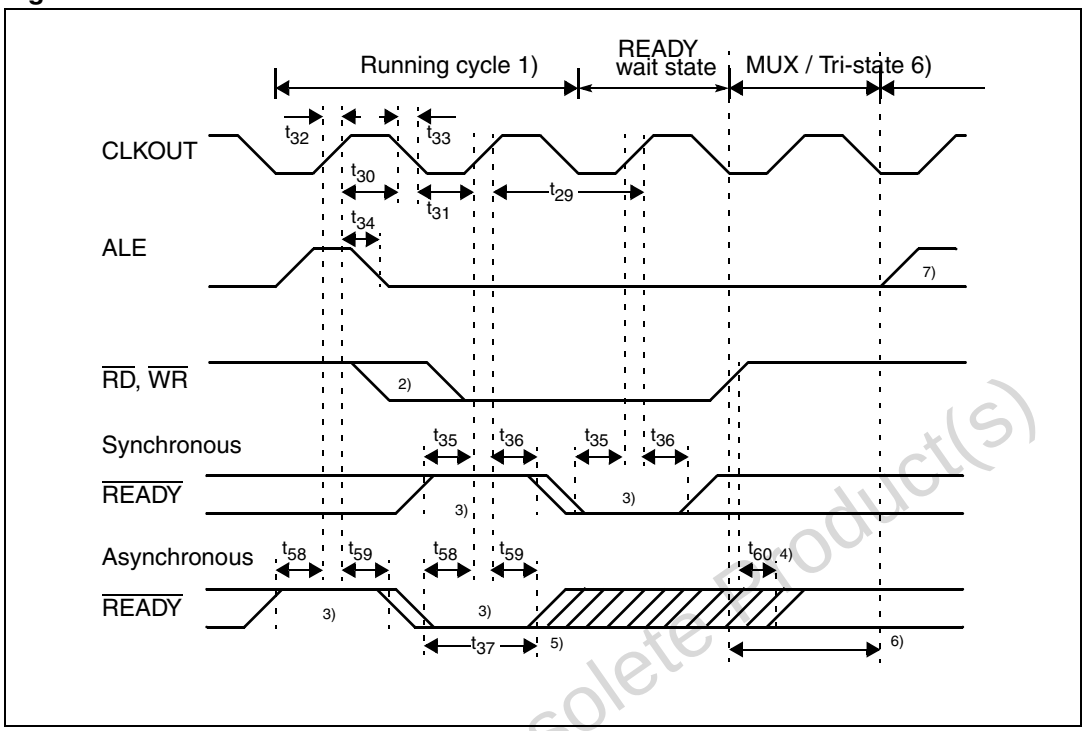


Figure 61. CLKOUT and $\overline{\text{READY}}$



1. Cycle as programmed, including MCTC wait states (Example shows 0 MCTC WS).
2. The leading edge of the respective command depends on RW-delay.
3. $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled wait state, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
4. $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
5. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4).
6. Multiplexed bus modes have a MUX wait state added after a bus cycle, and an additional MTTC wait state may be inserted here.
   For a multiplexed bus with MTTC wait state this delay is two CLKOUT cycles, for a demultiplexed bus without MTTC wait state this delay is zero.
7. The next external bus cycle may start here.

25.8.19 External bus arbitration

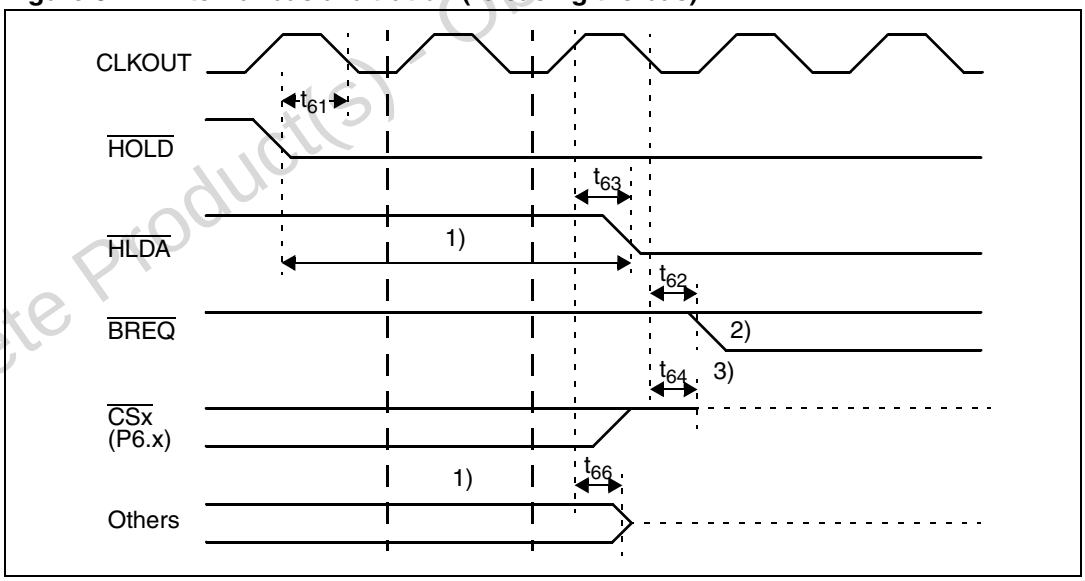
V_{DD} = 5 V ± 10 %, V_{SS} = 0 V, T_A = -40 to +125 °C, C_L = 50 pF

Table 81. External bus arbitration timings

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU clock 1/2 TCL = 1 to 64 MHz		Unit
			min.	max.	min.	max.	
t_{61}	SR	$\overline{HOLD}$ input setup time to CLKOUT	18.5	–	18.5	–	ns
t_{62}	CC	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	–	12.5	–	12.5	ns
t_{63}	CC	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	–	12.5	–	12.5	ns
t_{64}	CC	$\overline{CSx}$ release [1]	–	20	–	20	ns
t_{65}	CC	$\overline{CSx}$ drive	– 4	15	– 4	15	ns
t_{66}	CC	Other signals release [1]	–	20	–	20	ns
t_{67}	CC	Other signals drive	– 4	15	– 4	15	ns

1. Partially tested, guaranteed by design characterization.

Figure 62. External bus arbitration (releasing the bus)



1. The ST10F271Z1 will complete the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.

25.8.20 High-speed synchronous serial interface (SSC) timing

Master mode

V_{DD} = 5 V ±10%, V_{SS} = 0 V, T_A = -40 to +125 °C, C_L = 50 pF

Table 82. SSC master mode timings

Symbol		Parameter	Max. baudrate 6.6 MBd (1)@f_{CPU} = 40 MHz (<SSCBR> = 0002h)		Variable baudrate (<SSCBR> = 0001h - FFFFh)		Unit
			min.	max.	min.	max.	
t_{300}	CC	SSC clock cycle time(2))	150	150	8TCL	262144 TCL	ns
t_{301}	CC	SSC clock high time	63	–	t_{300} / 2 – 12	–	ns
t_{302}	CC	SSC clock low time	63	–	t_{300} / 2 – 12	–	ns
t_{303}	CC	SSC clock rise time	–	10	–	10	ns
t_{304}	CC	SSC clock fall time	–	10	–	10	ns
t_{305}	CC	Write data valid after shift edge	–	15	–	15	ns
t_{306}	CC	Write data hold after shift edge(3)	– 2	–	– 2	–	ns
t_{307p}	SR	Read data setup time before latch edge, phase error detection on (SSCPEN = 1)	37.5	–	2TCL + 12.5	–	ns
t_{308p}	SR	Read data hold time after latch edge, phase error detection on (SSCPEN = 1)	50	–	4TCL	–	ns
t_{307}	SR	Read data setup time before latch edge, phase error detection off (SSCPEN = 0)	25	–	2TCL	–	ns
t_{308}	SR	Read data hold time after latch edge, phase error detection off (SSCPEN = 0)	0	–	0	–	ns

1. Maximum Baudrate is in reality 8Mbaud, that can be reached with 64 MHz CPU clock and <SSCBR> set to '3h', or with 48 MHz CPU clock and <SSCBR> set to '2h'. When 40 MHz CPU clock is used the maximum baudrate cannot be higher than 6.6 Mbaud (<SSCBR> = '2h') due to the limited granularity of <SSCBR>. Value '1h' for <SSCBR> can be used only with CPU clock equal to (or lower than) 32 MHz.
2. Formula for SSC clock cycle time: t_{300} = 4 TCL x (<SSCBR> + 1) Where <SSCBR> represents the content of the SSC Baudrate register, taken as unsigned 16-bit integer. Minimum limit allowed for t_{300} is 125 ns (corresponding to 8Mbaud).
3. Partially tested, guaranteed by design characterization.

Figure 66. PQFP144 - 144-pin plastic quad flatpack 28 x 28 mm, 0.65 mm pitch, package outline

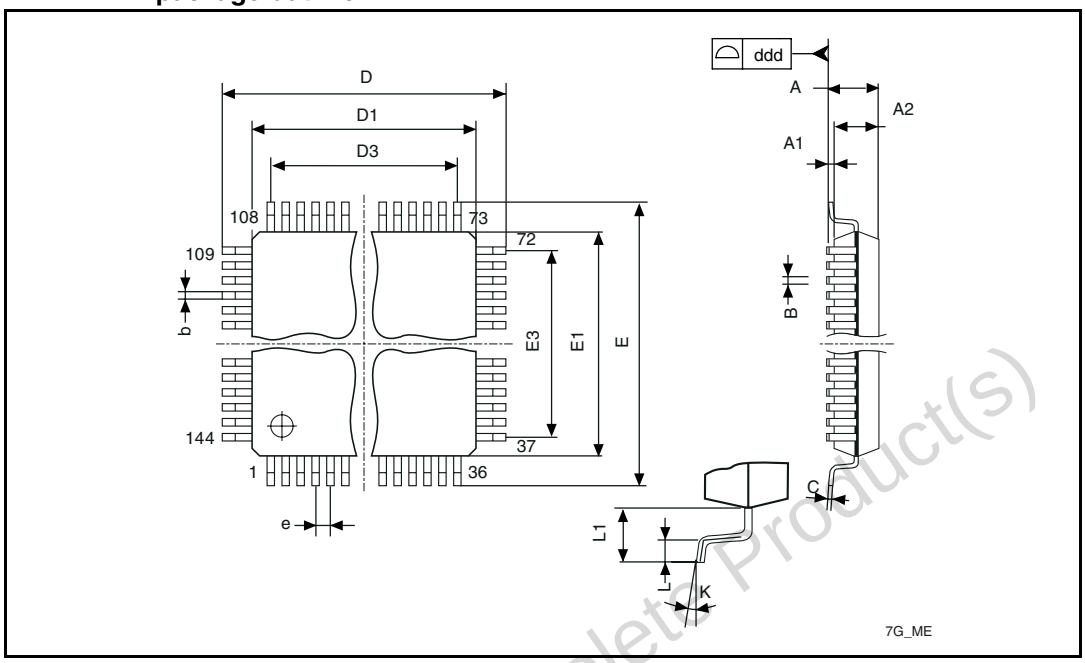


Table 84. PQFP144 - 144-pin plastic quad flatpack 28 x 28 mm, 0.65 mm pitch, package mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			4.070			0.1602
A1		0.250			0.0098	
A2	3.420	3.170	3.670	0.1346	0.1248	0.1445
b		0.220	0.380		0.0087	0.0150
C		0.130	0.230		0.0051	0.0091
D	31.200	30.950	31.450	1.2283	1.2185	1.2382
D1	28.000	27.900	28.100	1.1024	1.0984	1.1063
D3	22.750			0.8957		
e	0.650			0.0256		
E	31.200	30.950	31.450	1.2283	1.2185	1.2382
E1	28.000	27.900	28.100	1.1024	1.0984	1.1063
E3	22.750			0.8957		
L	0.800	0.650	0.950	0.0315	0.0256	0.0374
L1	1.600			0.0630		
K		0°	7°		0°	7°
ddd	0.101	0.0040				

1. Values in inches are converted from mm and rounded up to 4 decimal places.