**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 14 |
| Program Memory Size | 1KB (1K x 8) |
| Program Memory Type | ROM |
| EEPROM Size | - |
| RAM Size | 125 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 18-DIP (0.300", 7.62mm) |
| Supplier Device Package | 18-DIP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86c0412pecr5036 |

## GENERAL DESCRIPTION (Continued)

**Note:** All signals with a preceding front slash, "/", are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

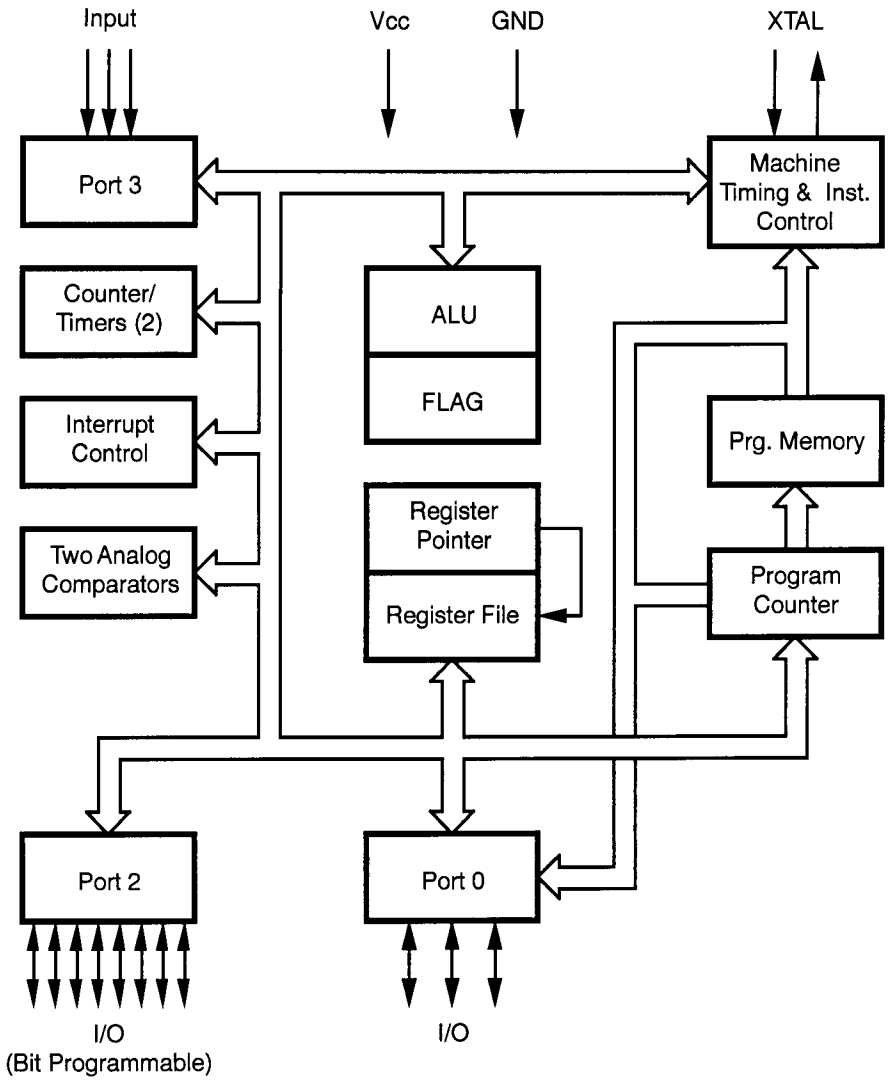



**Figure 1. Z86C04/C08 Functional Block Diagram**

| Symbol | Parameter | $V_{CC}$ | $T_A$= 0°C to +70°C Min | $T_A$= 0°C to +70°C Max | $T_A$= –40°C to +105°C Min | $T_A$= –40°C to +105°C Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CH}$ | Clock Input High Voltage | 3.0V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 3.0V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 0.8 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 3.0V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 1.8 | V | | 1 |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | 1 |
| $V_{IL}$ | Input Low Voltage | 3.0V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 0.8 | V | | 1 |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | 1 |
| $V_{OH}$ | Output High Voltage | 3.0V | $V_{CC}$–0.4 | | $V_{CC}$–0.4 | | 3.0 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 5.5V | $V_{CC}$–0.4 | | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 3.0V | $V_{CC}$–0.4 | | $V_{CC}$–0.4 | | 3.0 | V | Low Noise @ $I_{OH}$ = –0.5 mA | 6 |
| | | 5.5V | $V_{CC}$–0.4 | | $V_{CC}$–0.4 | | 4.8 | V | Low Noise @ $I_{OH}$ = –0.5 mA | 6 |
| $V_{OL1}$ | Output Low Voltage | 3.0V | | 0.8 | | 0.8 | 0.2 | V | $I_{OL}$= +4.0 mA | 5 |
| | | 5.5V | | 0.4 | | 0.4 | 0.1 | V | $I_{OL}$= +4.0 mA | 5 |
| | | 3.0V | | 0.4 | | 0.4 | 0.2 | V | Low Noise @ $I_{OL}$ = 1.0 mA | 6 |
| | | 5.5V | | 0.4 | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | 6 |
| $V_{OL2}$ | Output Low Voltage | 3.0V | | 1.0 | | 1.0 | 0.8 | V | $I_{OL}$ = +12 mA | 5 |
| | | 5.5V | | 0.8 | | 0.8 | 0.3 | V | $I_{OL}$ = +12 mA | 5 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 3.0V | | 25 | | 25 | 10 | mV | | |
| | | 5.5V | | 25 | | 25 | 10 | mV | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Auto Reset | | 2.0 | 2.8 | | | 2.6 | V | Int. CLK Freq @ 6 MHz Max. | |
| | | | | | 1.8 | 3.0 | 2.6 | V | Int. CLK Freq @ 4 MHz Max. | |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 3.0V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 3.0V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | | 0 | $V_{CC}$–1.0 | 0 | $V_{CC}$–1.5 | | V | | |
| $I_{CC}$ | Supply Current | 3.0V | | 3.5 | | 3.5 | 1.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 5.5V | | 7.0 | | 7.0 | 3.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| Symbol | Parameter | $V_{CC}$ | $T_A$= 0°C to +70°C Min | Max | $T_A$= –40°C to +105°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current | 3.0V | | 8.0 | | 8.0 | 3.0 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 5.5V | | 11.0 | | 11.0 | 4.4 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 3.0V | | 10 | | 10 | 3.6 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| | | 5.5V | | 15 | | 15 | 9.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| $I_{CC1}$ | Standby Current | 3.0V | | 2.5 | | 2.5 | 0.7 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 5.5V | | 4.0 | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 3.0V | | 4.0 | | 4.0 | 1.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | 5,7 |
| | | 5.5V | | 5.0 | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | 5,7 |
| | | 3.0V | | 4.5 | | 4.5 | 1.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | 5,7 |
| | | 5.5V | | 7.0 | | 7.0 | 4.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | 5,7 |
| $I_{CC}$ | Supply Current (Low Noise) | 3.0V | | 3.5 | | 3.5 | 1.5 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 5.5V | | 7.0 | | 7.0 | 3.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 3.0V | | 5.8 | | 5.8 | 2.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 5.5V | | 9.0 | | 9.0 | 4.0 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 3.0V | | 8.0 | | 8.0 | 3.0 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |
| | | 5.5V | | 11.0 | | 11.0 | 4.4 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |

| Symbol | Parameter | $V_{CC}$ | $T_A$= 0°C to +70°C Min | Max | $T_A$= –40°C to +105°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (Low Noise Mode) | 3.0V | | 2.5 | | 2.5 | 0.7 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 5.5V | | 4.0 | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 3.0V | | 3.5 | | 5.0 | 0.9 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 5,7 |
| | | 5.5V | | 5.0 | | 5.0 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4MHz | 5,7 |
| $I_{CC2}$ | Standby Current | 3.0V | | 10 | | 20 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V,Vcc WDT is not Running | 7 |
| | | 5.5V | | 10 | | 20 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V,Vcc WDT is not Running | 7 |
| $I_{ALL}$ | Auto Latch Low Current | 3.0V | | 12 | | 8.0 | 3.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | 30 | | 32 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| $I_{ALH}$ | Auto Latch High Current | 3.0V | | –8 | | –5.0 | –1.5 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | –16 | | –20 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |

**Notes:**

1. Port 0, 2, and 3 only
2. $V_{SS}$ = 0V = GND
3. The device operates down to $V_{LV}$. The minimum operational $V_{CC}$ is determined on the value of the voltage $V_{LV}$ at the ambient temperature. The $V_{LV}$ increases as the temperature decreases.
4. $V_{CC}$ = 3.0V to 5.5V, typical values measured at $V_{CC}$ = 3.3V and $V_{CC}$ = 5.0V.
5. Standard Mode (not Low EMI Mode).
6. Z86C08 only
7. Inputs at power rail and outputs are unloaded.

## AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

| | | | | $T_A$ = -40C to +125C | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 8 MHz | | 12 MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 3.0V | 125 | DC | 83 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | 83 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 3.0V | | 25 | | 15 | ns | 1 |
| | | | 5.5V | | 25 | | 15 | ns | 1 |
| 3 | TwC | Input Clock Width | 3.0V | | 62 | | 41 | ns | 1 |
| | | | 5.5V | | 62 | | 41 | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 3.0V | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 3.0V | 8TpC | | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 3.0V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 3.0V | 100 | | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time Before Timeout | 3.0V | 25 | | 25 | | ms | |
| | | | 5.5V | 8 | | 8 | | ms | |
| 11 | Tpor | Power-On Reset Time | 3.0V | 50 | 180 | 50 | 180 | ms | 3 |
| | | | 5.5V | 18 | 100 | 18 | 100 | ms | 3 |
| | | | 3.0V | 4 | 30 | 4 | 30 | ms | 4 |
| | | | 5.5V | 2 | 15 | 2 | 15 | ms | 4 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Z86C08
4. Z86C04

## AC ELECTRICAL CHARACTERISTICS (Continued)

| | | | | $T_A$= 0°C to +70°C | | | | $T_A$= -40°C to +105°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 8 MHz | | 12 MHz | | 8 MHz | | 12 MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 3.0V | 125 | DC | 83 | DC | 125 | DC | 83 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | 83 | DC | 125 | DC | 83 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 3.0V | | 25 | | 15 | | 25 | | 15 | ns | 1 |
| | | | 5.5V | | 25 | | 15 | | 25 | | 15 | ns | 1 |
| 3 | TwC | Input Clock Width | 3.0V | 62 | | 41 | | | 62 | | 41 | ns | 1 |
| | | | 5.5V | 62 | | 41 | | | 62 | | 41 | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 3.0V | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 3.0V | | 100 | | 100 | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time Before Timeout | 3.0V | 25 | | 25 | | 25 | | 25 | | ms | |
| | | | 5.5V | 10 | | 10 | | 8 | | 8 | | ms | 3 |
| | | | 5.5V | 12 | | 12 | | 12 | | 12 | | ms | 4 |
| 11 | Tpor | Power-On Reset Time | 3.0V | 50 | 160 | 50 | 160 | 50 | 160 | 50 | 160 | ms | 3 |
| | | | 5.5V | 24 | 80 | 24 | 80 | 18 | 80 | 18 | 80 | ms | 3 |
| | | | 3.0V | 6 | 30 | 6 | 30 | 4 | 30 | 4 | 30 | ms | 4 |
| | | | 5.5V | 3 | 15 | 3 | 15 | 2 | 15 | 2 | 15 | ms | 4 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31)
3. Z86C08
4. Z86C04

## AC ELECTRICAL CHARACTERISTICS

Low Noise Mode (SCLK/TCLK = XTAL)

| | | | | $T_A$= –40°C to +125°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 2 MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 3.0V | 1000 | DC | 500 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 500 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 3.0V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 3.0V | 500 | | 250 | | ns | 1 |
| | | | 5.5V | 500 | | 250 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 3.0V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 3.0V | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 3.0V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 3.0V | 100 | | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time Before Timeout | 3.0V | 25 | | 25 | | ms | 3 |
| | | | 5.5V | 8 | | 8 | | ms | 3 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.

## AC ELECTRICAL CHARACTERISTICS (Continued)

| | | | | $T_A$= 0°C to 70°C | | | | $T_A$= –40°C to +105°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 4 MHz | | 1 MHz | | 4 MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 3.0V | 1000 | DC | 250 | DC | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 3.0V | | 25 | | 25 | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 3.0V | 500 | | 125 | | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | 500 | | 125 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 3.0V | 2.5TpC | | 2.5TpC | | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 3.0V | 4TpC | | 4TpC | | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | 4TpC | | 4TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Timer | 3.0V | | 100 | | 100 | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 2.5TpC | | 2.5TpC | | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time Before Timeout | 3.0V | 25 | | 25 | | 25 | | 25 | | ms | 3 |
| | | | 5.5V | 10 | | 10 | | 8 | | 8 | | ms | 3,5 |
| | | | 5.5V | 12 | | 12 | | 12 | | 12 | | ms | 3,4 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.
4. Z86C04
5. Z86C08

# LOW NOISE VERSION

## Low EMI Emission

The Z8® MCU can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted

## APPLICATION PRECAUTIONS:

1. Emulator does not support the 32 kHz operation.
2. For the Z86C04, the WDT only runs in STOP Mode if the permanent WDT option is selected and if the on-board RC oscillator is selected as the clock source for the WDT.
3. For the Z86C08, the WDT only runs in Stop Mode if the permanent WDT option is selected.
4. The registers %FE (GPR) and %FF (SPL) are reset to 00Hex after Stop Mode recovery or any reset.
5. Emulator does not support the system clock driving the WDT mask option.
6. Must wait two NOPS before analog comparitor outputs are valid after enabling analog mode.
7. Must disable interrupts, enable the analog comparitor, and then clear IRQ3 to IRQ0 when switching from digital to analog mode.

## PIN DESCRIPTION

**XTAL1, XTAL2** *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a RC, parallel-resonant crystal, LC, or an external single-phase clock to the on-chip clock oscillator and buffer.

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. After Power-On Reset, this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. To change the Auto Latch state, the auto latches must be over driven with current greater than $I_{ALH}$ (high to low) or $I_{ALL}$ (low to high).

**Port 0** (P02-P00). Port 0 is a 3-bit I/O, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be configured under software control to be all inputs or all outputs (Figure 6).

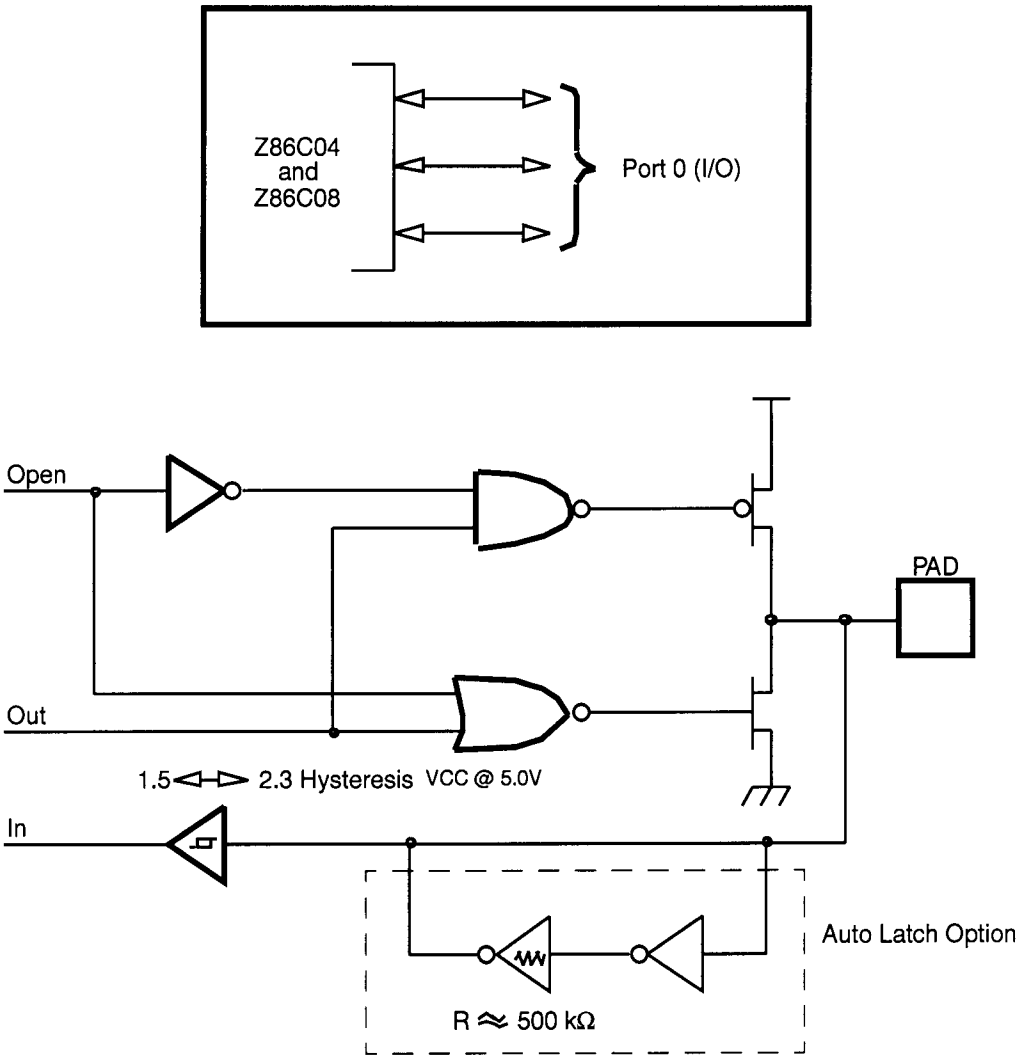



**Figure 6. Port 0 Configuration**

**Port 2** (P27-P20). Port 2 is an 8-bit I/O, bit-programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 7).

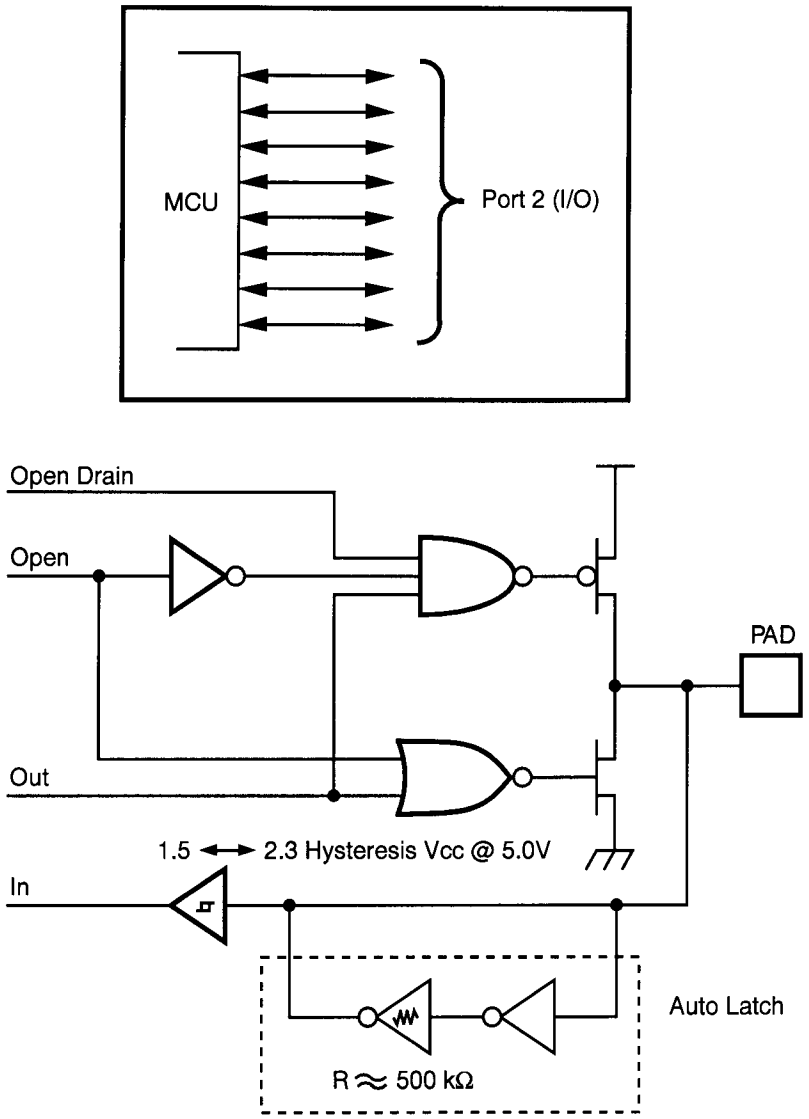



**Figure 7. Port 2 Configuration**

## PIN DESCRIPTION (Continued)

**Port 3** (P33-P31). Port 3 is a 3-bit, Schmitt-triggered CMOS-compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal ($T_{IN}$) (Figure 8).

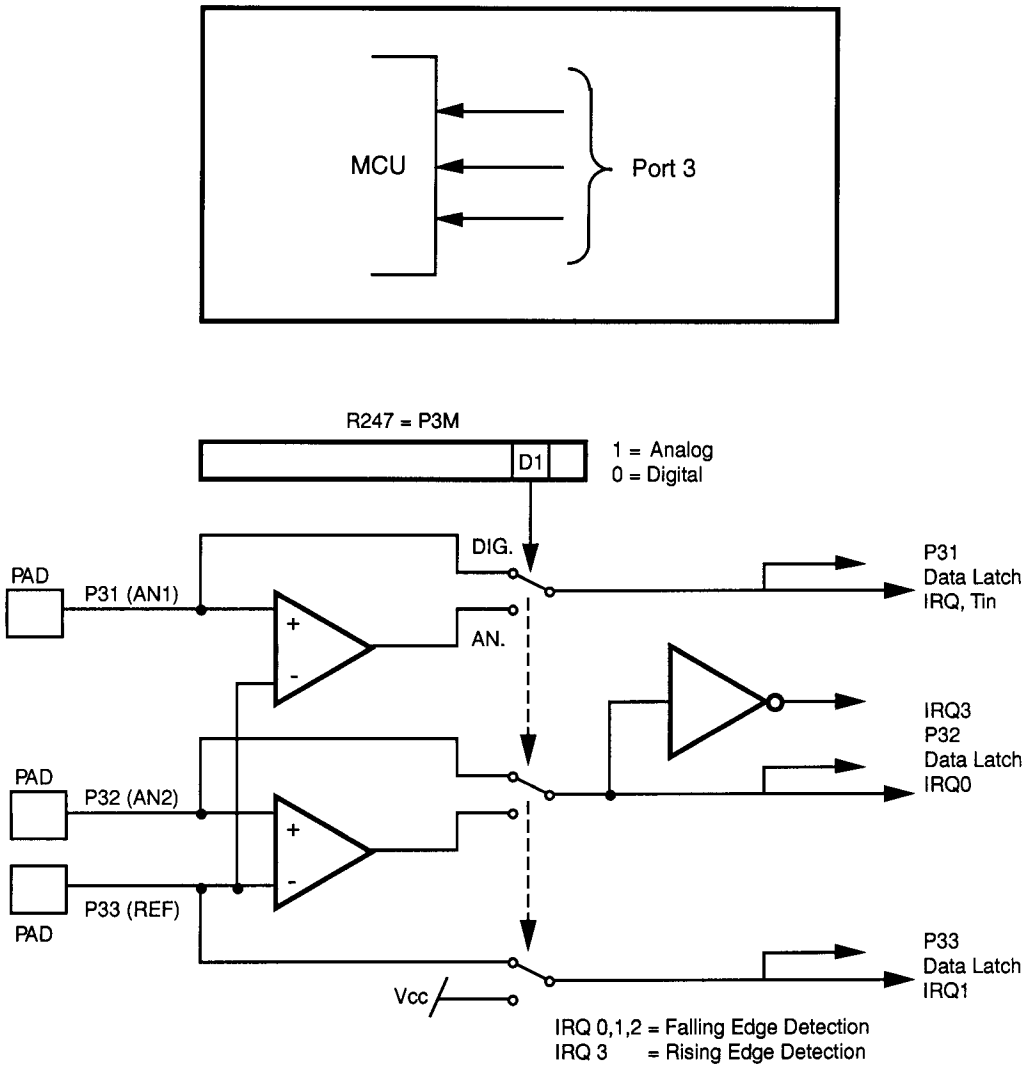



**Figure 8. Port 3 Configuration**

**Comparator Inputs.** Two analog comparators are added to Port 3 inputs for interface flexibility. Typical applications for these on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply that discontinues power in STOP Mode. The common voltage range is 0-4V when the $V_{CC}$ is 5.0V. Before the comparitor outputs are valid, two NOP delays are required after enabling the analog comparitors.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or $T_{IN}$ through P31. Alternately, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

## FUNCTIONAL DESCRIPTION

**RESET.** Upon power-up, the Power-On Reset circuit waits for $T_{POR}$ ms, plus 18 clock cycles, and then starts program execution at address %000C (Hex) (Figure 9). The device control registers' reset value is shown in Table 1.

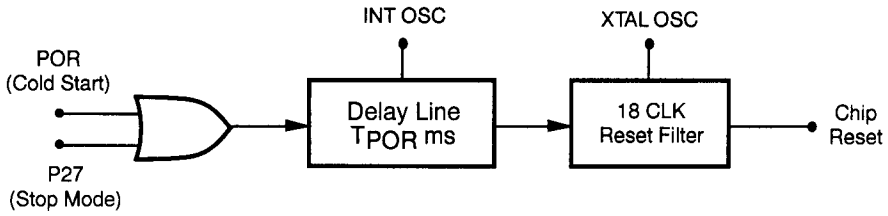



**Figure 9. Internal Reset Configuration**

**Table 1. Z86C04/C08 & C05/C07 Control Registers**

| | | Reset Condition | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Addr.** | **Reg.** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Comments** |
| 03H (3)* | Port 3 | U | U | U | U | U | U | U | U | |
| 02H (2)* | Port 2 | U | U | U | U | U | U | U | U | |
| 00H (0)* | Port 0 | U | U | U | U | U | U | U | U | |
| FFH(255) | SPL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FEH (254) | GPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FDH (253) | RP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FCH (252) | FLAGS | U | U | U | U | U | U | U | U | |
| FBH (251) | IMR | 0 | U | U | U | U | U | U | U | |
| FAH (250) | IRQ | U | U | 0 | 0 | 0 | 0 | 0 | 0 | IRQ3 is used for positive edge detection |
| F9H (249) | IPR | U | U | U | U | U | U | U | U | |
| F8H (248)* | P01M | U | U | U | 0 | U | U | 0 | 1 | |
| F7H (247)* | P3M | U | U | U | U | U | U | 0 | 0 | |
| F6H (246)* | P2M | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Inputs after reset |
| F5H (245) | PRE0 | U | U | U | U | U | U | U | 0 | |
| F4H (244) | T0 | U | U | U | U | U | U | U | U | |
| F3H (243) | PRE1 | U | U | U | U | U | U | 0 | 0 | |
| F2H (242) | T1 | U | U | U | U | U | U | U | U | |
| F1H (241) | TMR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Note:** *Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be re-configured as shown in Table 1 and the user must avoid bus contention on the port pins or it may affect device reliability.

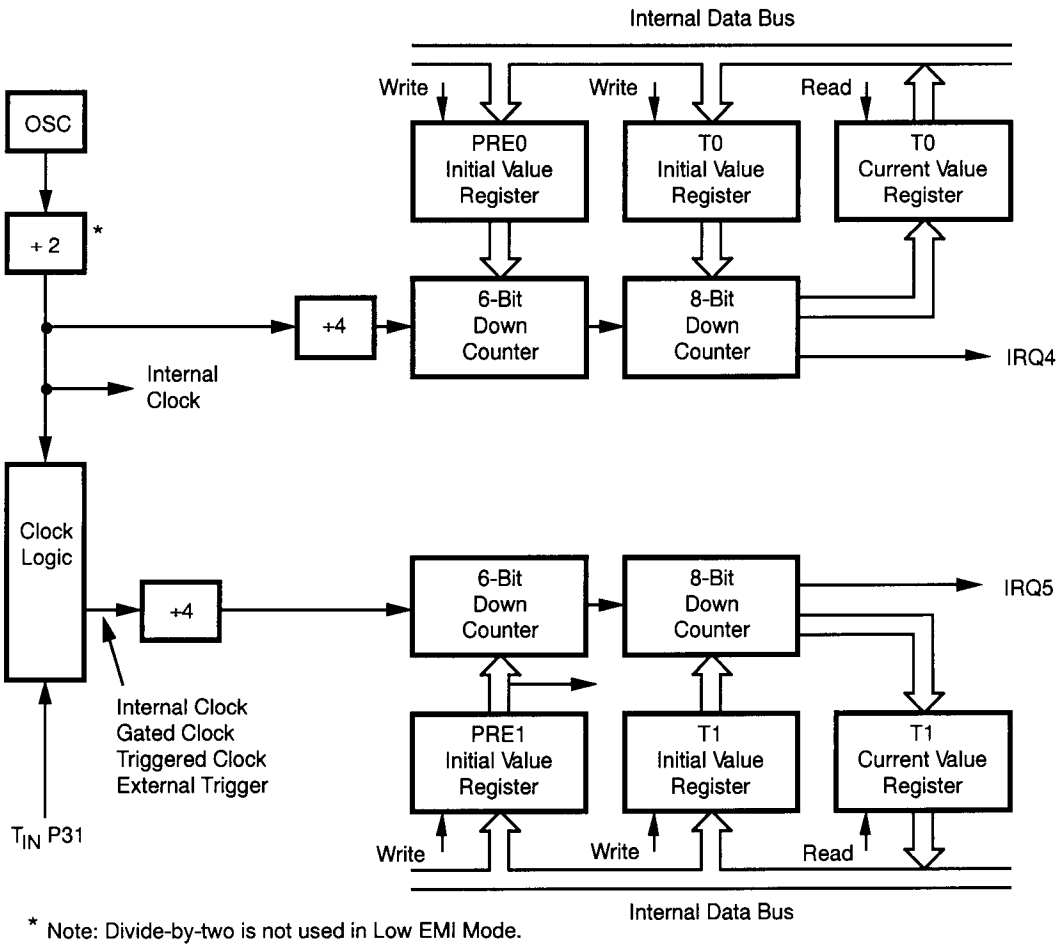
## FUNCTIONAL DESCRIPTION (Continued)

**Counter/Timer.** There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 13).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock.




* Note: Divide-by-two is not used in Low EMI Mode.

**Figure 13. Counter/Timers Block Diagram**

**Opcode WDT** (5FH). The first time Opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done within the maximum $T_{WDT}$ period; otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of $T_{POR}$ plus 18 XTAL clock cycles. The WDT does not work (run) in STOP Mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

**Opcode WDH** (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it facilitates running the WDT function during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

**Permanent WDT Mask Option.** Only when the Permanent WDT Mask Option is selected, then the WDT is hardwired to be enabled after reset. The WDT will operate in Run Mode, HALT Mode, and STOP Mode. The Opcode 5FH is used to refresh or clear the WDT counter. The WDT instruction (4FH) has no effect The WDT will not run in STOP Mode if the system clock driving the WDT is selected (Z86C04 only).

**System Clock Driving WDT Mask Option (Z86C04 only)** When this option is selected, the Z8's system clock drives the WDT instead of the on-board RC oscillator driving the WDT. The WDT time-out will be SCLK x 32,512.The WDT will not run in STOP Mode.

**Low-Voltage Protection** ($V_{LV}$). Maximum ($V_{LV}$) Conditions:

Case 1: $T_A$= –40°C, +85°C, Internal Clock Frequency equal or less than 6 MHz

Case 2: $T_A$= –40°C, +105°C, Internal Clock Frequency equal or less than 4 MHz

**Note:** The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low-Voltage Protection trip point ($V_{LV}$) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Cases 1 and 2. The actual low voltage trip point is a function of temperature and process parameters (Figure 16).

**1 MHz (Typical)**

| Temp | –40C° | 0°C | +25°C | +70°C | +105°C | +125°C |
|---|---|---|---|---|---|---|
| $V_{LV}$ | 3.0 | 2.75 | 2.6 | 2.3 | 2.1 | 1.9 |

**ROM Protect.** ROM Protect fully protects the Z86C04/C08 ROM code from being read internally. **When ROM Protect is selected, ROM look-up tables can be used in this mode.**

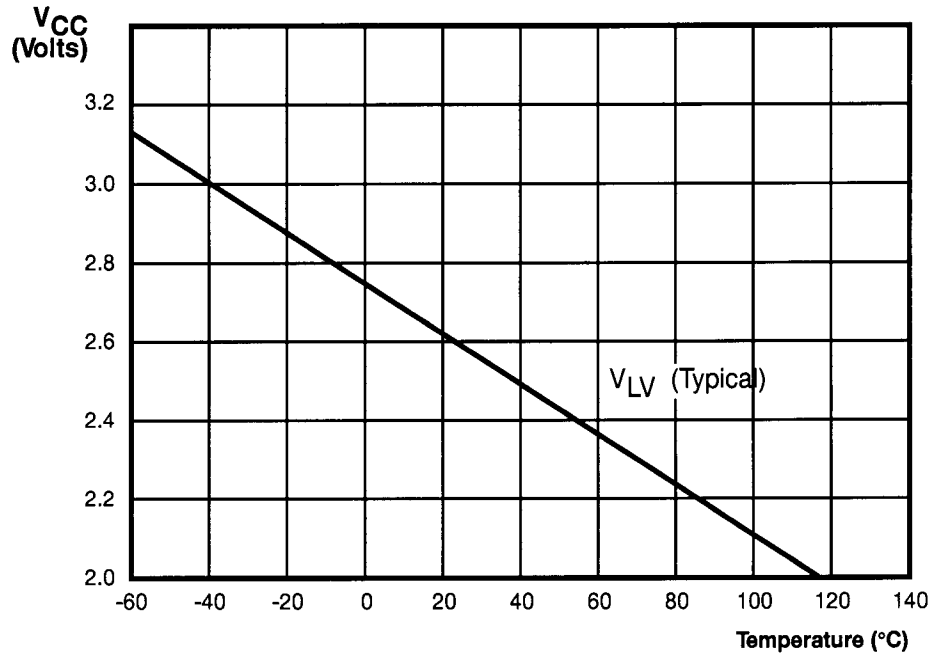



**Figure 16. Typical Z86C04/C08 $V_{LV}$ vs. Temperature**

# Z8 CONTROL REGISTER DIAGRAMS

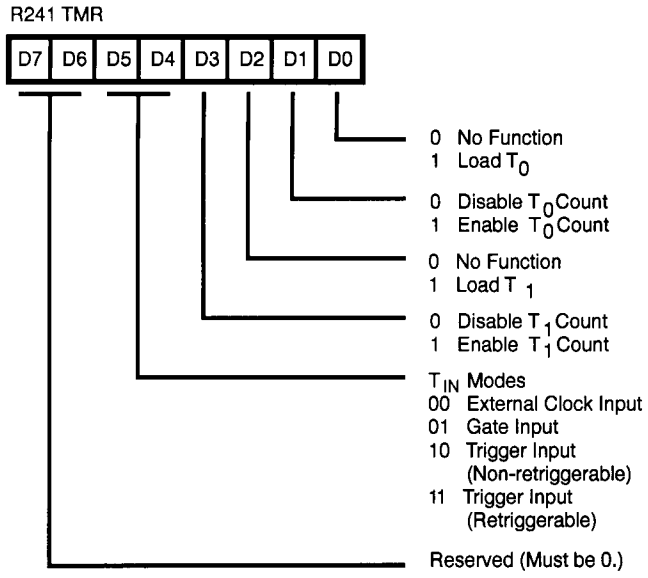



**Figure 17. Timer Mode Register ($F1_H$: Read/Write)**

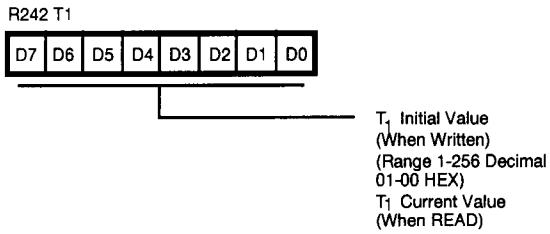



**Figure 18. Counter Time 1 Register ($F2_H$: Read/Write)**

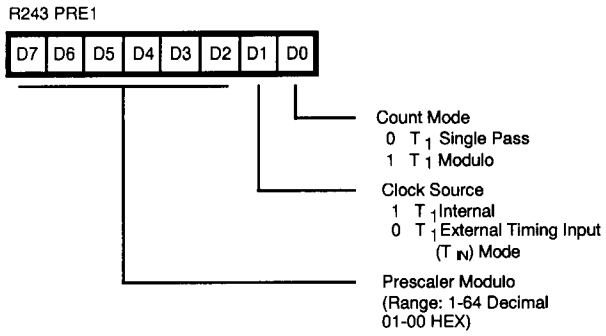



**Figure 19. Prescaler 1 Register ($F3_H$: Write Only)**

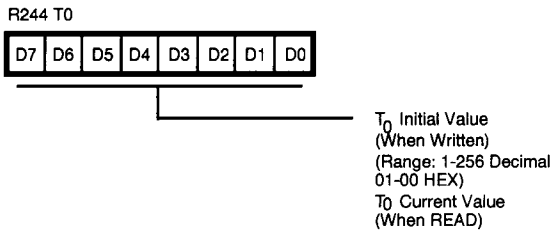



**Figure 20. Counter/Timer 0 Register ($F4_H$: Read/Write)**

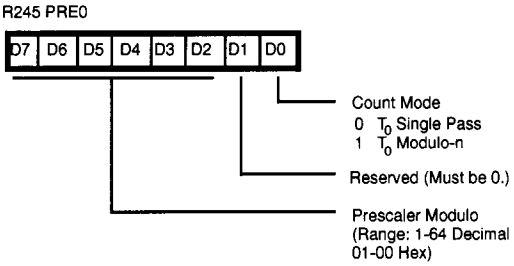



**Figure 21. Prescaler 0 Register ($F5_H$: Write Only)**

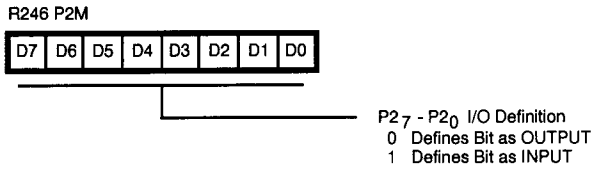



**Figure 22. Port 2 Mode Register ($F6_H$: Write Only)**

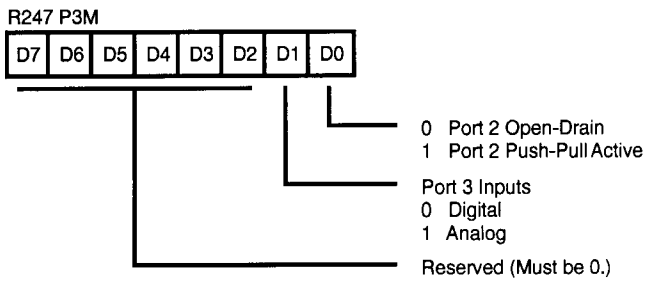



**Figure 23. Port 3 Mode Register ($F7_H$: Write Only)**

Standard Mode

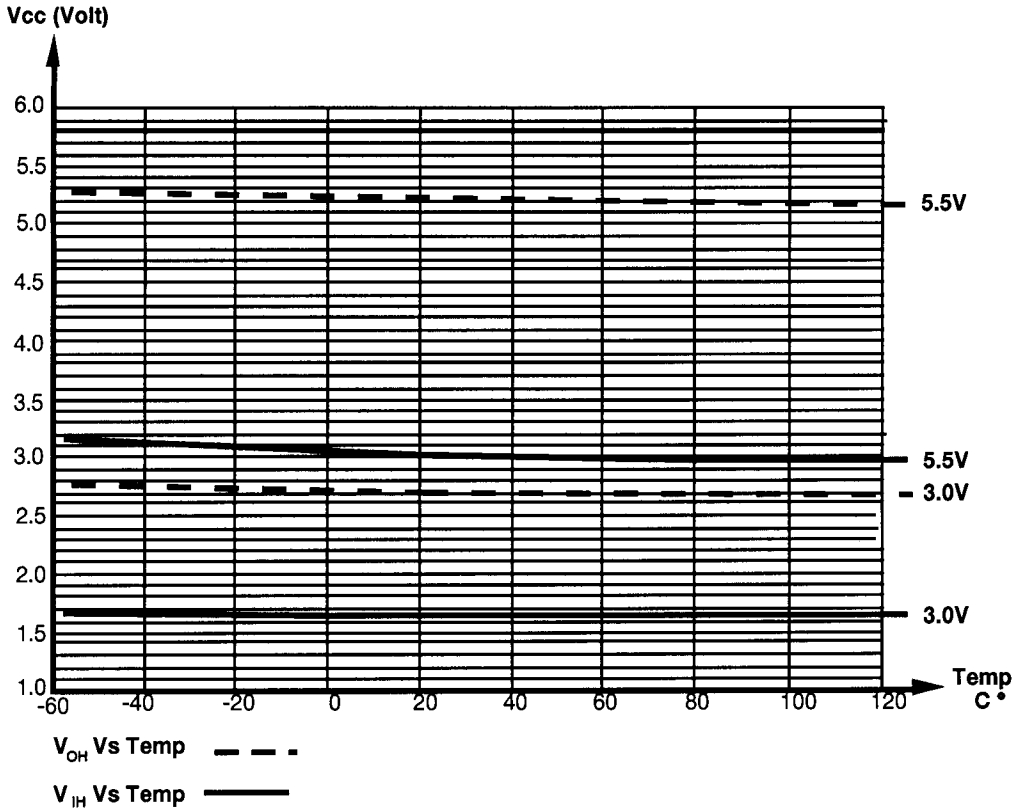



Figure 32. $V_{IH}$, $V_{OH}$ vs. Temperature

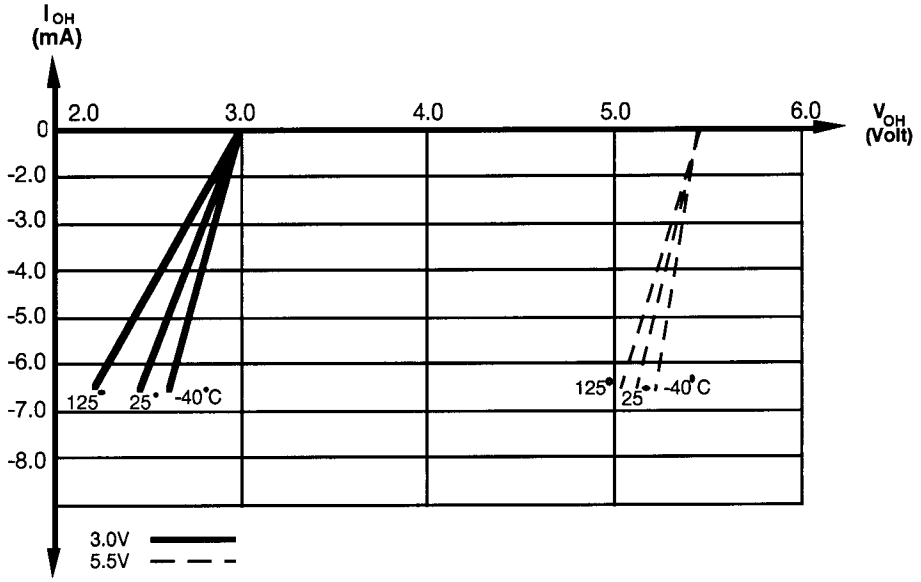



Figure 33. Typical $I_{OH}$ vs. $V_{OH}$

## Z8 CONTROL REGISTER DIAGRAMS (Continued)

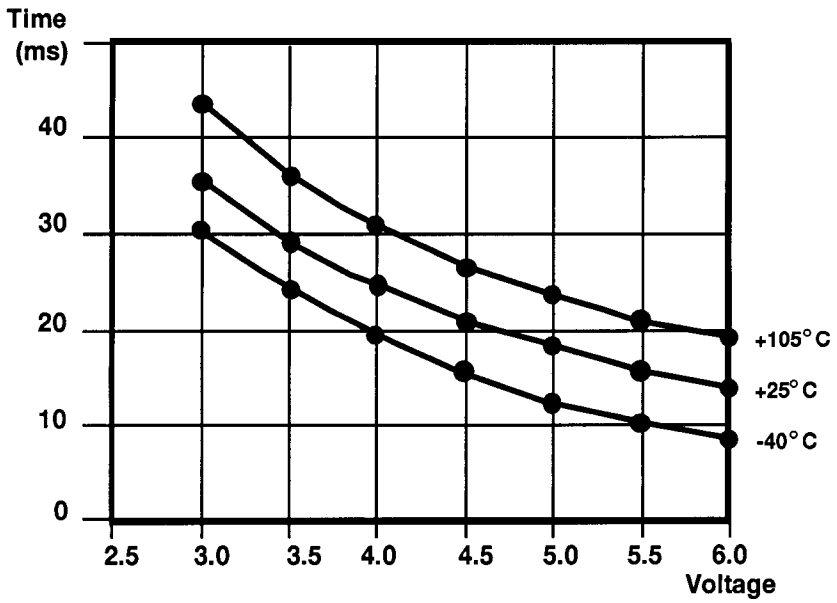



**Figure 34. Typical WDT Time Out Period vs. $V_{cc}$ Over Temperature**

## ORDERING INFORMATION

| Z86C04 (12 MHz) Standard Temperature | | Z86C08 (12 MHz) Standard Temperature | |
|---|---|---|---|
| 18-Pin DIP | 18-Pin SOIC | 18-Pin DIP | 18-Pin SOIC |
| Z86C0412PSC | Z86C0412SSC | Z86C0812PSC | Z86C0812SSC |
| Extended Temperature | | Extended Temperature | |
| 18-Pin DIP | 18-Pin SOIC | 18-Pin DIP | 18-Pin SOIC |
| Z86C0412PEC | Z86C0412SEC | Z86C0812PEC | Z86C0812SEC |
| Z86C0412PAC | Z86C0412SAC | Z86C0812PAC | Z86C0812SAC |

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

## CODES

**Preferred Package**
P = DIP
S = SOIC

**Preferred Temperature**
S = 0°C to +70°C

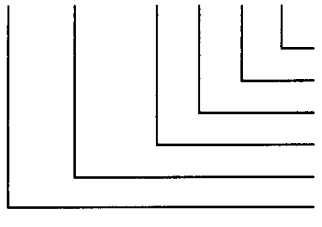
**Longer Lead Time**
E = –40°C to +105°C
A = -40°C to +125°C

**Speeds**
12 = 12 MHz

**Environmental**
C = Plastic Standard

**Example:**

**Z 86C04 12 P S C** is a Z86C04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



**Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.



Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com