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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c0412pscr4265

DC ELECTRICAL CHARACTERISTICS (Continued)

I_{CC}	Supply Current	5.5V	15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	3.0V	2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V	4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		3.0V	4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V	5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		3.0V	4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V	7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	3.0V	3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V	7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		3.0V	5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V	9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz	7
I_{CC1}	Standby Current (Low Noise Mode)	3.0V	2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1MHz	7
		5.5V	4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1MHz	7
		3.0V	3.0	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V	4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
I_{CC2}	Standby Current	3.0V	20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC};WDT is not Running	7
		5.5V	20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC};WDT is not Running	7
I_{ALL}	Auto Latch Low Current	3.0V	8.0	3.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V	36	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.0V	–5.0	–1.5	µA	$0V < V_{IN} < V_{CC}$	
		5.5V	–22	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 0, 2, and 3 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86C08 only
7. Inputs at power rail and outputs are unloaded.
8. Low EMI Mode

Symbol	Parameter	V_{CC}	T_A= 0°C to +70°C Min	T_A= 0°C to +70°C Max	T_A= –40°C to +105°C Min	T_A= –40°C to +105°C Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		1
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		1
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V		1
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V		1
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	5
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	Low Noise @ I_{OH} = –0.5 mA	6
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	6
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL}= +4.0 mA	5
		5.5V		0.4		0.4	0.1	V	I_{OL}= +4.0 mA	5
		3.0V		0.4		0.4	0.2	V	Low Noise @ I_{OL} = 1.0 mA	6
		5.5V		0.4		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	6
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA	5
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA	5
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.0	2.8			2.6	V	Int. CLK Freq @ 6 MHz Max.	
					1.8	3.0	2.6	V	Int. CLK Freq @ 4 MHz Max.	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0	0	V_{CC}–1.5		V		
I_{CC}	Supply Current	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	T_A= 0°C to +70°C Min	Max	T_A= –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		4.0		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		3.0V		4.0		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		3.0V		4.5		4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		7.0		7.0	3.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		3.0V		5.8		5.8	2.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		9.0		9.0	4.0	mA	All Output and I/O Pins Floating @ 2 MHz	7
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		11.0		11.0	4.4	mA	All Output and I/O Pins Floating @ 4 MHz	7

Symbol	Parameter	V_{CC}	T_A= 0°C to +70°C Min	Max	T_A= –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		4.0		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		3.0V		3.5		5.0	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	5,7
		5.5V		5.0		5.0	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4MHz	5,7
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V,Vcc WDT is not Running	7
		5.5V		10		20	1.0	µA	STOP Mode V_{IN} = 0V,Vcc WDT is not Running	7
I_{ALL}	Auto Latch Low Current	3.0V		12		8.0	3.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		30		32	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.0V		–8		–5.0	–1.5	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–16		–20	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 0, 2, and 3 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode).
6. Z86C08 only
7. Inputs at power rail and outputs are unloaded.

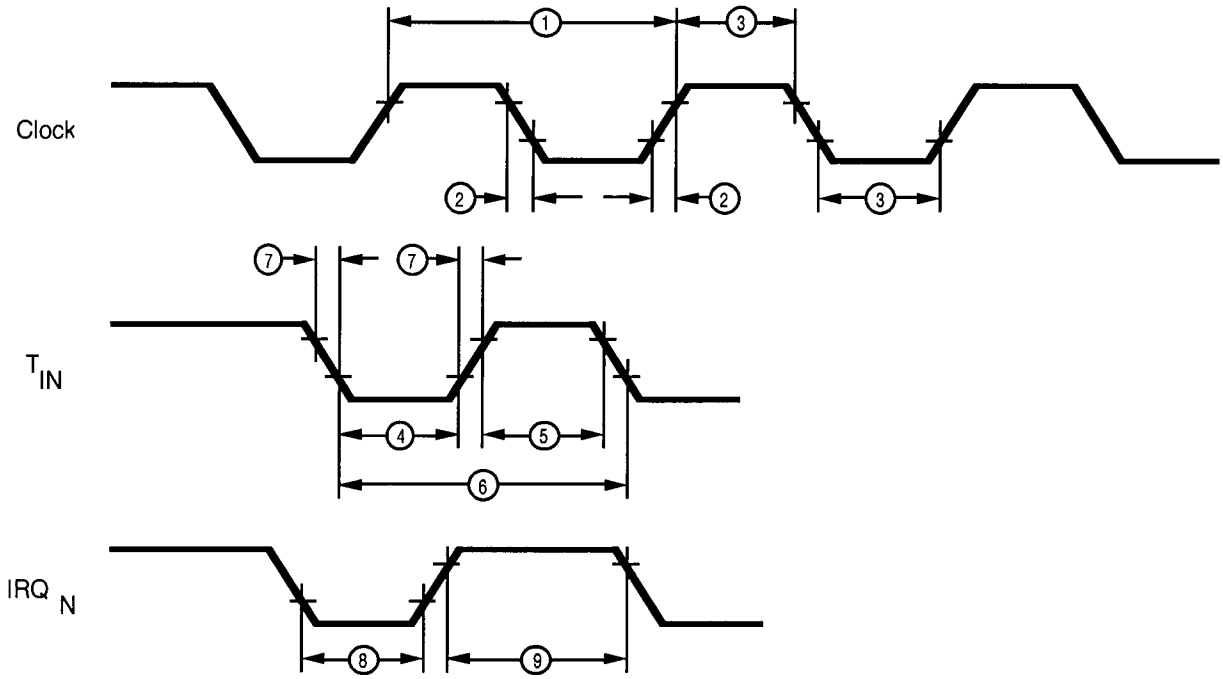


Figure 5. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A = -40C to +125C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	3.0V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		ms	
			5.5V	8		8		ms	
11	Tpor	Power-On Reset Time	3.0V	50	180	50	180	ms	3
			5.5V	18	100	18	100	ms	3
			3.0V	4	30	4	30	ms	4
			5.5V	2	15	2	15	ms	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Z86C08
4. Z86C04

AC ELECTRICAL CHARACTERISTICS (Continued)

				T_A= 0°C to +70°C				T_A= -40°C to +105°C					
				8 MHz		12 MHz		8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	1
			5.5V		25		15		25		15	ns	1
3	TwC	Input Clock Width	3.0V	62		41			62		41	ns	1
			5.5V	62		41			62		41	ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		25		25		ms	
			5.5V	10		10		8		8		ms	3
			5.5V	12		12		12		12		ms	4
11	Tpor	Power-On Reset Time	3.0V	50	160	50	160	50	160	50	160	ms	3
			5.5V	24	80	24	80	18	80	18	80	ms	3
			3.0V	6	30	6	30	4	30	4	30	ms	4
			5.5V	3	15	3	15	2	15	2	15	ms	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31)
3. Z86C08
4. Z86C04

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode (SCLK/TCLK = XTAL)

				T_A= –40°C to +125°C					
				1 MHz		2 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	1000	DC	500	DC	ns	1
			5.5V	1000	DC	500	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	3.0V	500		250		ns	1
			5.5V	500		250		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		ms	3
			5.5V	8		8		ms	3

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.

PIN DESCRIPTION

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a RC, parallel-resonant crystal, LC, or an external single-phase clock to the on-chip clock oscillator and buffer.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. After Power-On Reset, this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. To change the Auto Latch state, the auto latches must be over driven with current greater than I_{ALH} (high to low) or I_{ALL} (low to high).

Port 0 (P02-P00). Port 0 is a 3-bit I/O, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be configured under software control to be all inputs or all outputs (Figure 6).

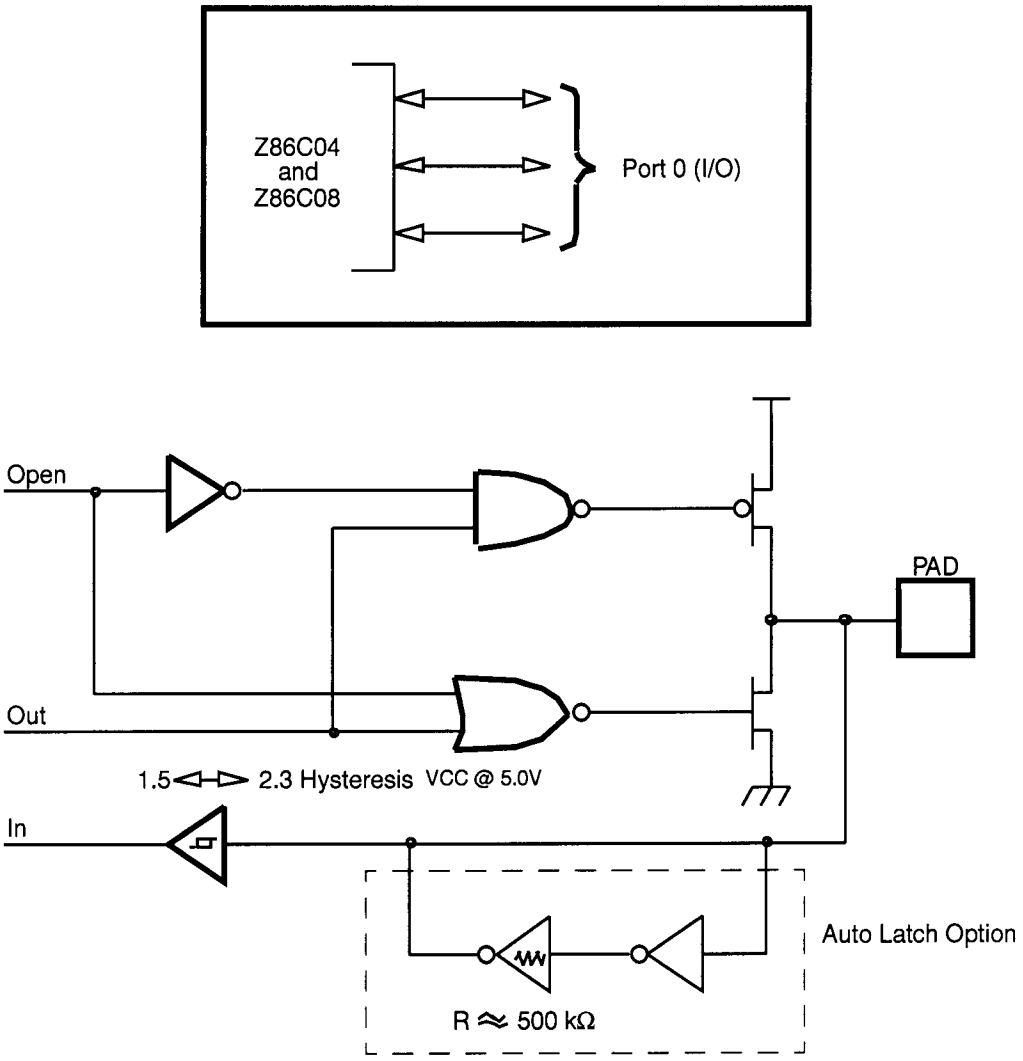


Figure 6. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit-programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 7).

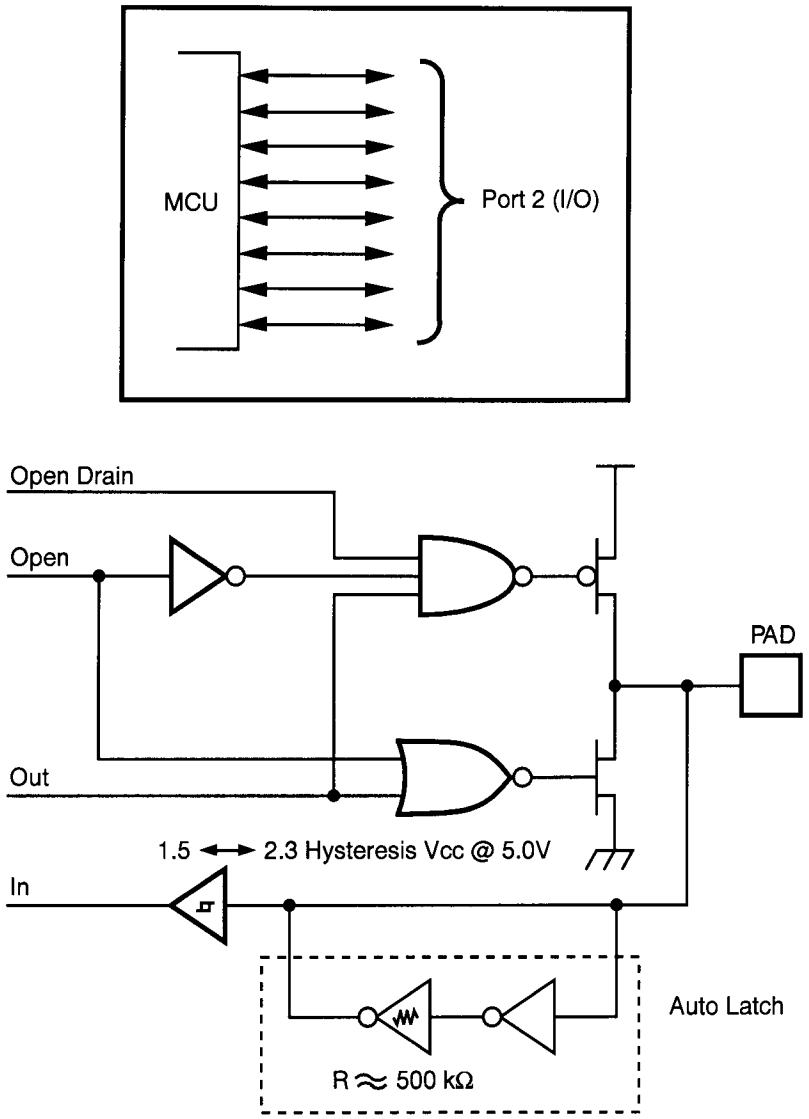


Figure 7. Port 2 Configuration

FUNCTIONAL DESCRIPTION

RESET. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, and then starts program execution at address %000C (Hex) (Figure 9). The device control registers' reset value is shown in Table 1.

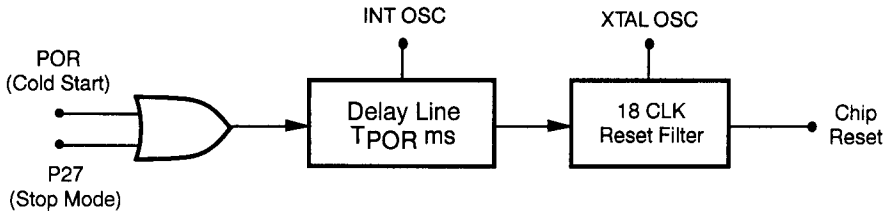


Figure 9. Internal Reset Configuration

Table 1. Z86C04/C08 & C05/C07 Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
03H (3)*	Port 3	U	U	U	U	U	U	U	U	
02H (2)*	Port 2	U	U	U	U	U	U	U	U	
00H (0)*	Port 0	U	U	U	U	U	U	U	U	
FFH(255)	SPL	0	0	0	0	0	0	0	0	
FEH (254)	GPR	0	0	0	0	0	0	0	0	
FDH (253)	RP	0	0	0	0	0	0	0	0	
FCH (252)	FLAGS	U	U	U	U	U	U	U	U	
FBH (251)	IMR	0	U	U	U	U	U	U	U	
FAH (250)	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9H (249)	IPR	U	U	U	U	U	U	U	U	
F8H (248)*	P01M	U	U	U	0	U	U	0	1	
F7H (247)*	P3M	U	U	U	U	U	U	0	0	
F6H (246)*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5H (245)	PRE0	U	U	U	U	U	U	U	0	
F4H (244)	T0	U	U	U	U	U	U	U	U	
F3H (243)	PRE1	U	U	U	U	U	U	0	0	
F2H (242)	T1	U	U	U	U	U	U	U	U	
F1H (241)	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be re-configured as shown in Table 1 and the user must avoid bus contention on the port pins or it may affect device reliability.

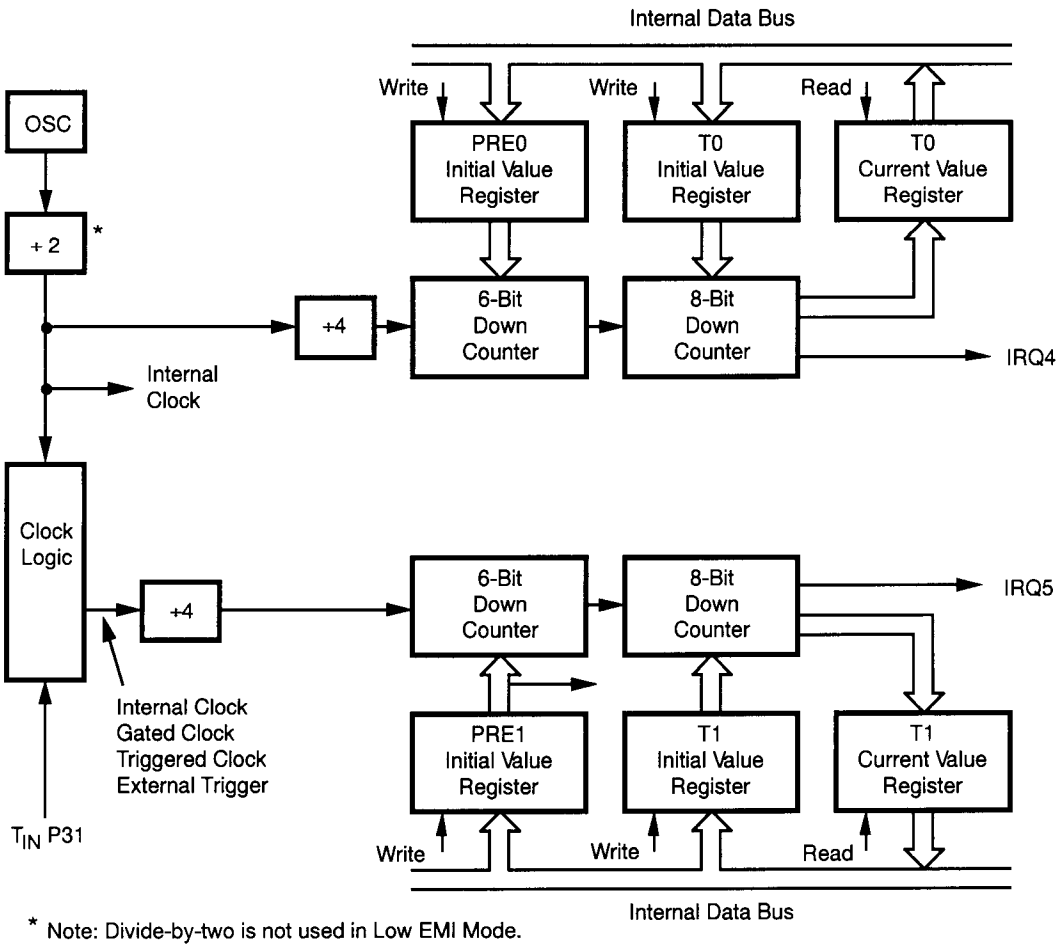
FUNCTIONAL DESCRIPTION (Continued)

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 13).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock.



* Note: Divide-by-two is not used in Low EMI Mode.

Figure 13. Counter/Timers Block Diagram

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 14). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 2).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86C08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1(P31)	4,5	External (F) Edge
IRQ3	AN2(P32)	6,7	External (R) Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

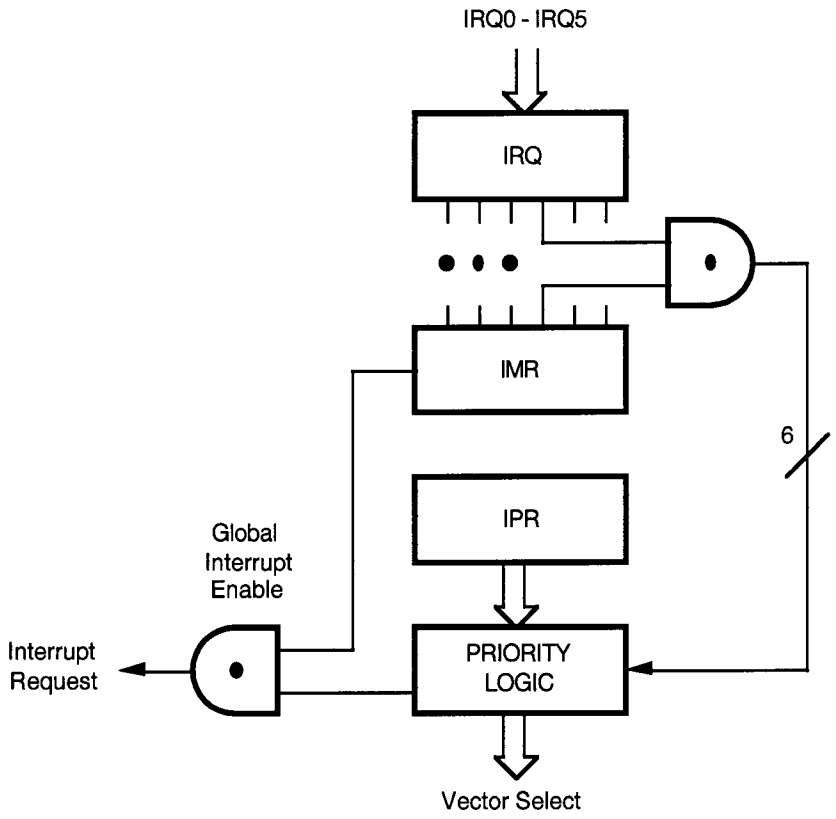


Figure 14. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a RC, crystal, ceramic resonator, LC, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors (which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device Ground pin 14 (Figure 15).

Note that the crystal capacitor loads should be connected to V_{SS} pin 14 to reduce ground noise injection.

To use 32 kHz crystal, the 32 kHz operational mask option must be selected, and an external resistor R must be connected across XTAL1 and XTAL2.To use RC oscillator, the RC oscillator option must be selected.

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC} or dropping the V_{CC} below V_{LV}. The second method is if P27 is at a low level when the device executes the STOP instruction. A low condition on P27 releases the STOP Mode regardless if configured for input or output.

Program execution under both conditions begins at location 000C (Hex). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Note: (X = dependent upon user's application.)
In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, that is, as follows:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
            or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT should be refreshed once the WDT is enabled within every Twdt period; otherwise, the Z8 resets itself. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

WDT = 5F (Hex)

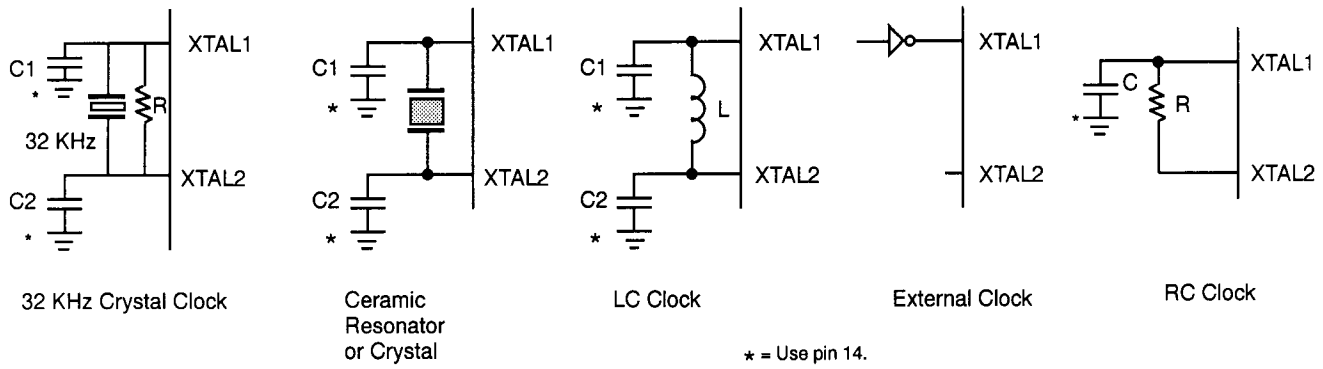


Figure 15. Oscillator Configuration

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done within the maximum T_{WDT} period; otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 XTAL clock cycles. The WDT does not work (run) in STOP Mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

Opcode WDH (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it facilitates running the WDT function during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT Mask Option. Only when the Permanent WDT Mask Option is selected, then the WDT is hardwired to be enabled after reset. The WDT will operate in Run Mode, HALT Mode, and STOP Mode. The Opcode 5FH is used to refresh or clear the WDT counter. The WDT instruction (4FH) has no effect The WDT will not run in STOP Mode if the system clock driving the WDT is selected (Z86C04 only).

System Clock Driving WDT Mask Option (Z86C04 only) When this option is selected, the Z8's system clock drives the WDT instead of the on-board RC oscillator driving the WDT. The WDT time-out will be SCLK x 32,512.The WDT will not run in STOP Mode.

Low-Voltage Protection (V_{LV}). Maximum (V_{LV}) Conditions:

Case 1: T_A= –40°C, +85°C, Internal Clock Frequency equal or less than 6 MHz

Case 2: T_A= –40°C, +105°C, Internal Clock Frequency equal or less than 4 MHz

Note: The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low-Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Cases 1 and 2. The actual low voltage trip point is a function of temperature and process parameters (Figure 16).

1 MHz (Typical)

Temp	–40C°	0°C	+25°C	+70°C	+105°C	+125°C
V_{LV}	3.0	2.75	2.6	2.3	2.1	1.9

ROM Protect. ROM Protect fully protects the Z86C04/C08 ROM code from being read internally. **When ROM Protect is selected, ROM look-up tables can be used in this mode.**

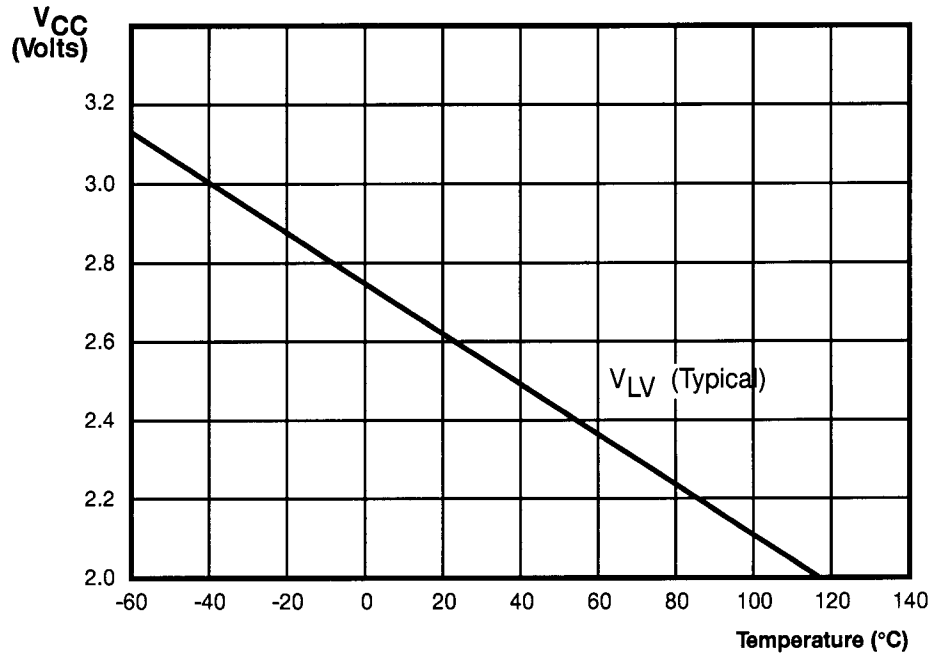


Figure 16. Typical Z86C04/C08 V_{LV} vs. Temperature

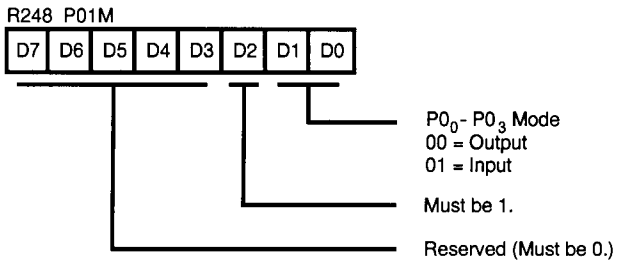


Figure 24. Port 0 and 1 Mode Register ($F8_H$: Write Only)

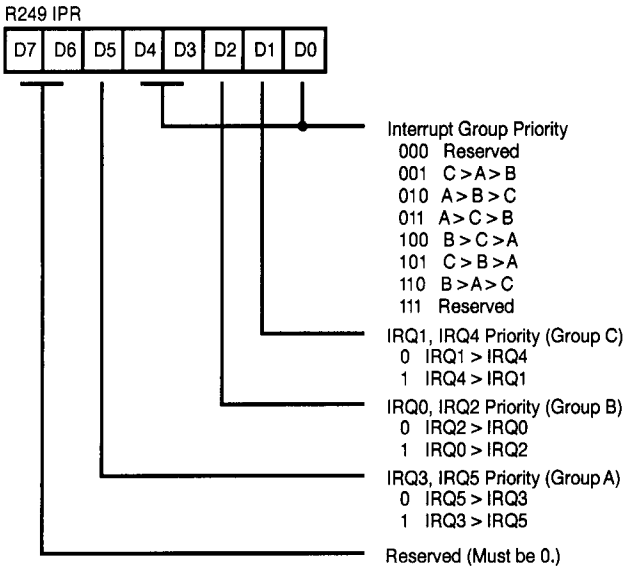


Figure 25. Interrupt Priority Register ($F9_H$: Write Only)

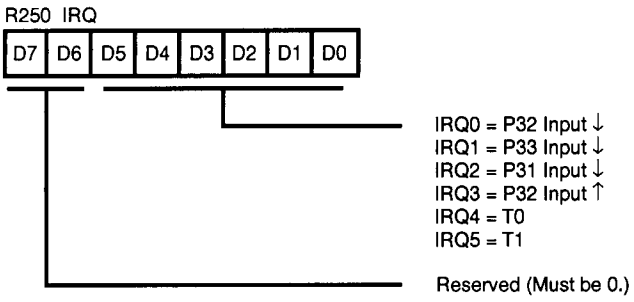


Figure 26. Interrupt Request Register (FA_H: Read/Write)

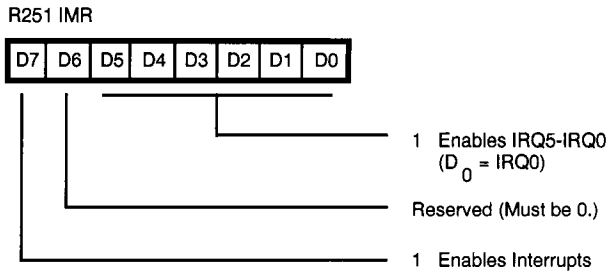


Figure 27. Interrupt Mask Register (FB_H: Read/Write)

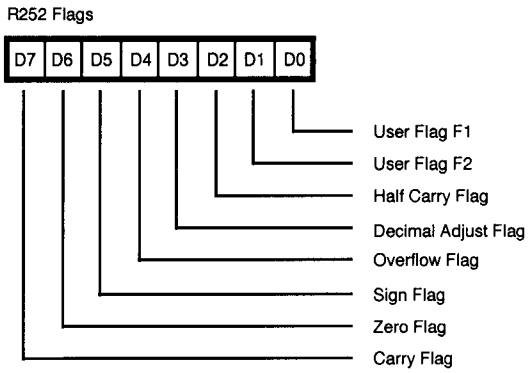


Figure 28. Flag Register (FC_H: Read/Write)

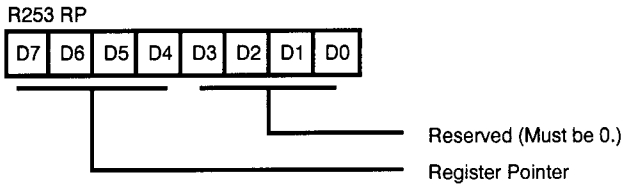


Figure 29. Register Pointer (FD_H: Read/Write)

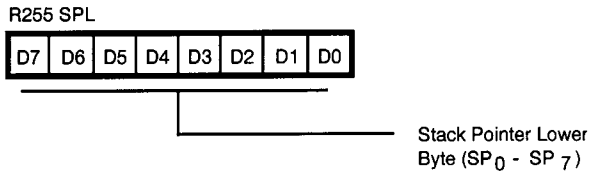


Figure 30. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS

Standard Mode

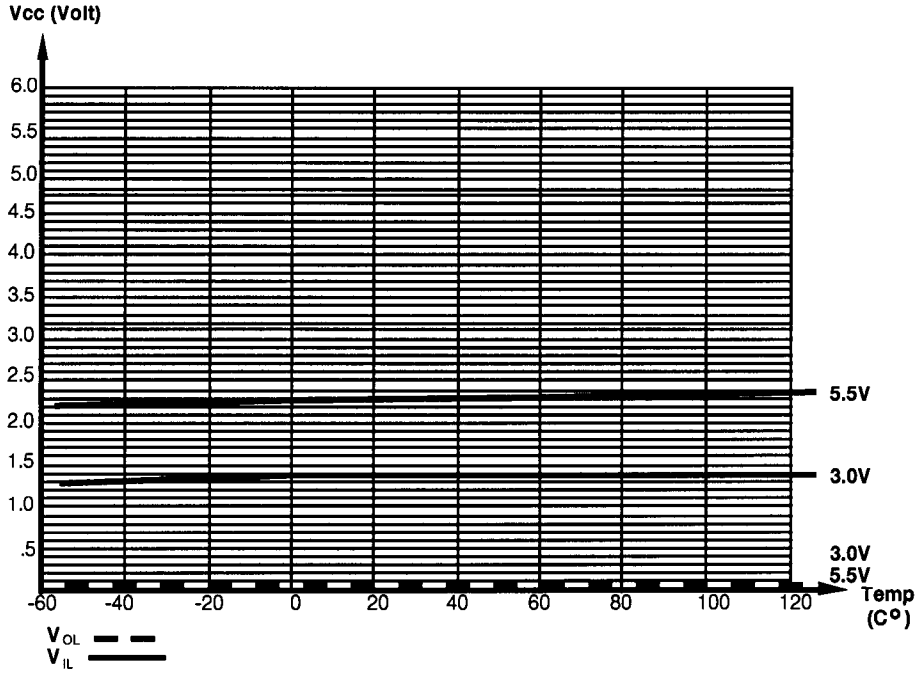


Figure 31. V_{IL}, V_{OL} vs. Temperature

Z8 CONTROL REGISTER DIAGRAMS (Continued)

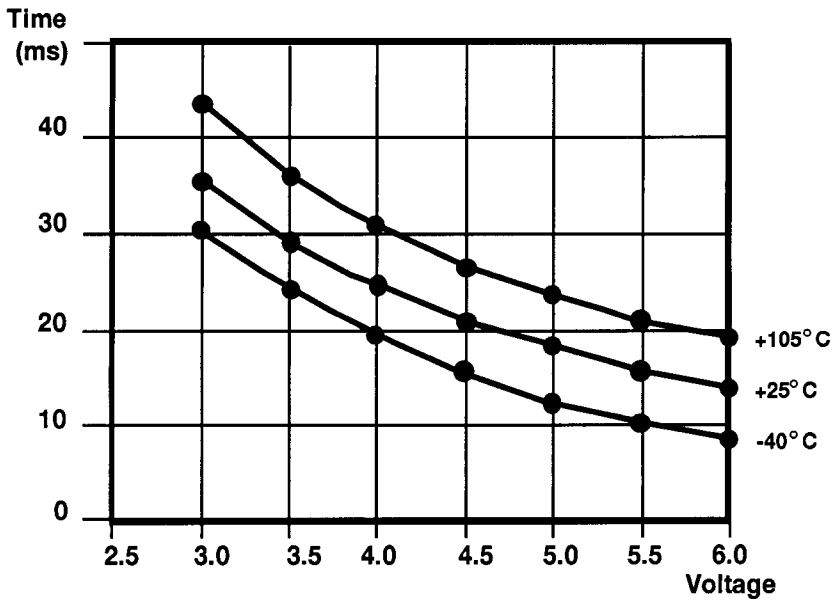
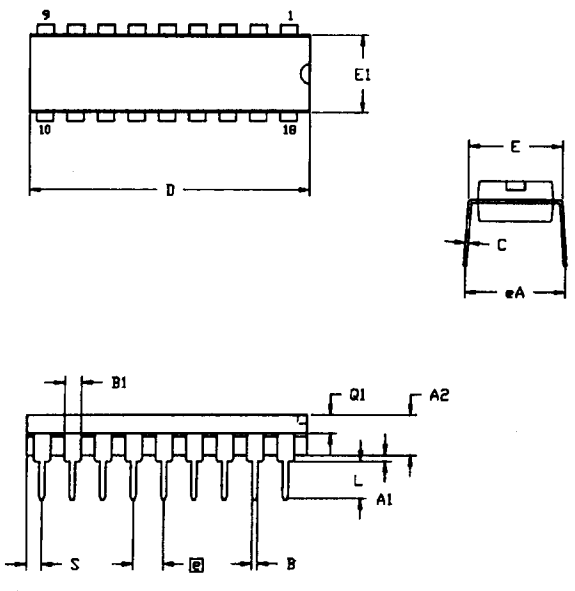


Figure 34. Typical WDT Time Out Period vs. V_{cc} Over Temperature

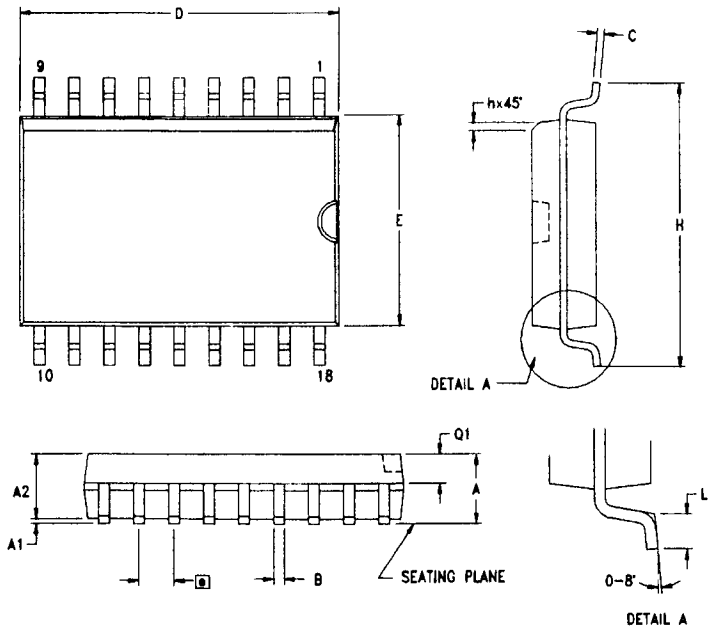
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 35. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 36. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C04 (12 MHz) Standard Temperature		Z86C08 (12 MHz) Standard Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0412PSC	Z86C0412SSC	Z86C0812PSC	Z86C0812SSC
Extended Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0412PEC	Z86C0412SEC	Z86C0812PEC	Z86C0812SEC
Z86C0412PAC	Z86C0412SAC	Z86C0812PAC	Z86C0812SAC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = DIP
S = SOIC

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C
A = -40°C to +125°C

Speeds
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C04 12 P S C is a Z86C04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow