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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c0812pecr5302

GENERAL DESCRIPTION (Continued)

Note: All signals with a preceding front slash, "/", are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

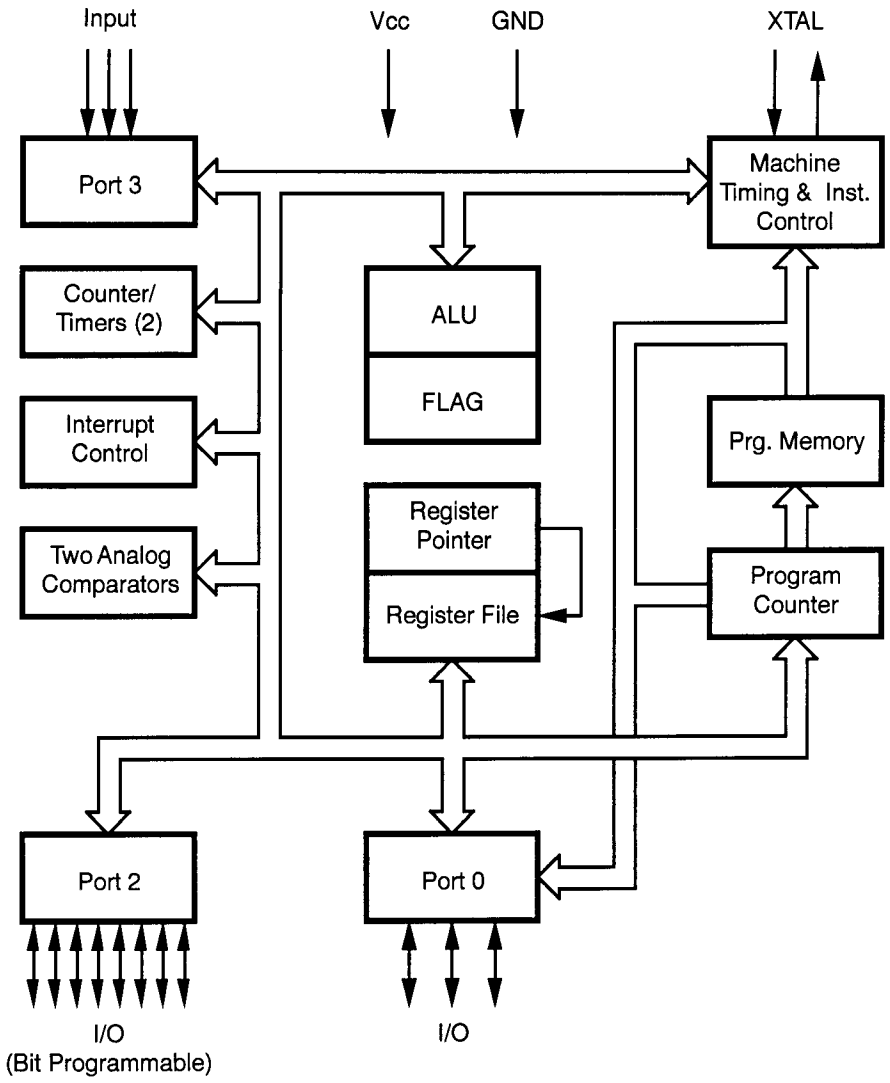


Figure 1. Z86C04/C08 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on Pin 7 with Respect to V_{SS}	–0.7	V_{DD}+1	V	2
Total Power Dissipation		462	mW	
Maximum Current out of V_{SS}		84	mA	
Maximum Current into V_{DD}		84	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		12	mA	
Maximum Output Current Sourced by Any I/O Pin		12	mA	
Total Maximum Output Current Sinked by Port 2		70	mA	
Total Maximum Output Current Sourced by Port 2		70	mA	

Notes:
1. This applies to all pins except where otherwise noted. Maximum current into pin must be ±600µA.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:
Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{OL} x I_{OL}).

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 4).

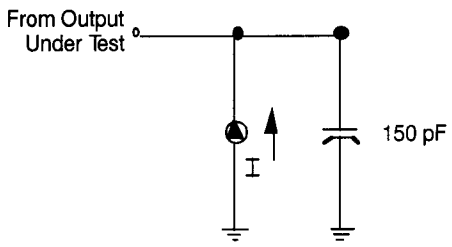


Figure 4. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +125°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	Vss–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		1
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		1
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	0.8	V		1
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		1
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	5
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		3.0V	V_{CC}–0.4		3.0	V	Low Noise @ I_{OH} = –0.5 mA	6
		5.5V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	6
V_{OL1}	Output Low Voltage	3.0V		0.8	0.2	V	I_{OL} = +4.0 mA	5
		5.5V		0.6	0.1	V	I_{OL} = +4.0 mA	5
		3.0V		0.6	0.2	V	Low Noise @ I_{OL} = 1.0 mA	6
		5.5V		0.6	0.1	V	Low Noise @ I_{OL} = 1.0 mA	6
V_{OL2}	Output Low Voltage	3.0V		1.2	0.8	V	I_{OL} = +12 mA	5
		5.5V		1.0	0.3	V	I_{OL} = +12 mA	5
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25	10	mV		
		5.5V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.6	3.0	2.6	V	Int. CLK Freq @ 2 MHz Max.	5
			1.6	3.0	2.6	V	Int. CLK Freq @ 1 MHz Max.	8
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, Vcc	
V_{VICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} –1.5		V		
I_{CC}	Supply Current	3.0V		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		7.0	3.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		3.0V		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		11.0	4.4	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		3.0V		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz	5,7

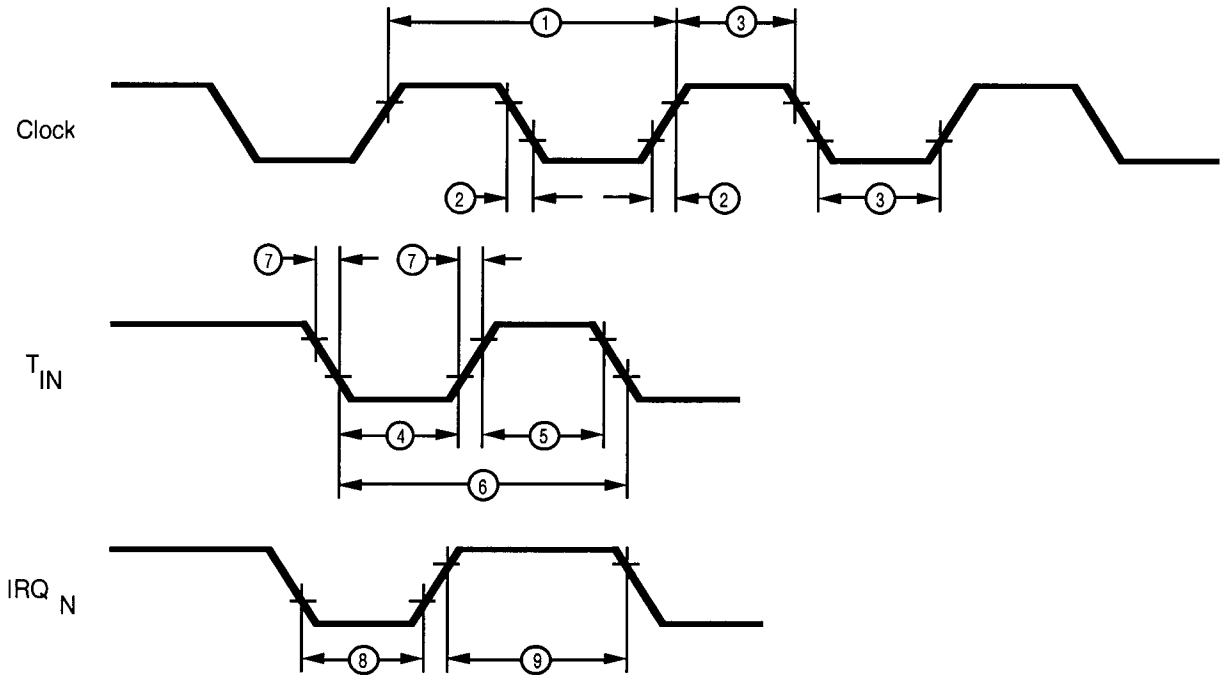


Figure 5. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A = -40C to +125C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	3.0V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		ms	
			5.5V	8		8		ms	
11	Tpor	Power-On Reset Time	3.0V	50	180	50	180	ms	3
			5.5V	18	100	18	100	ms	3
			3.0V	4	30	4	30	ms	4
			5.5V	2	15	2	15	ms	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Z86C08
4. Z86C04

AC ELECTRICAL CHARACTERISTICS (Continued)

				T_A= 0°C to +70°C				T_A= -40°C to +105°C					
				8 MHz		12 MHz		8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	1
			5.5V		25		15		25		15	ns	1
3	TwC	Input Clock Width	3.0V	62		41			62		41	ns	1
			5.5V	62		41			62		41	ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		25		25		ms	
			5.5V	10		10		8		8		ms	3
			5.5V	12		12		12		12		ms	4
11	Tpor	Power-On Reset Time	3.0V	50	160	50	160	50	160	50	160	ms	3
			5.5V	24	80	24	80	18	80	18	80	ms	3
			3.0V	6	30	6	30	4	30	4	30	ms	4
			5.5V	3	15	3	15	2	15	2	15	ms	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31)
3. Z86C08
4. Z86C04

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode (SCLK/TCLK = XTAL)

				T_A= –40°C to +125°C					
				1 MHz		2 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	1000	DC	500	DC	ns	1
			5.5V	1000	DC	500	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	3.0V	500		250		ns	1
			5.5V	500		250		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	3.0V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		ms	3
			5.5V	8		8		ms	3

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.

AC ELECTRICAL CHARACTERISTICS (Continued)

				T_A= 0°C to 70°C				T_A= –40°C to +105°C					
				1 MHz		4 MHz		1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	1000	DC	250	DC	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	1000	DC	250	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25		25		25	ns	1
			5.5V		25		25		25		25	ns	1
3	TwC	Input Clock Width	3.0V	500		125		500		125		ns	1
			5.5V	500		125		500		125		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			1
			5.5V	4TpC		4TpC		4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.0V	25		25		25		25		ms	3
			5.5V	10		10		8		8		ms	3,5
			5.5V	12		12		12		12		ms	3,4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Internal RC Oscillator driving WDT.
4. Z86C04
5. Z86C08

PIN DESCRIPTION (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, Schmitt-triggered CMOS-compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 8).

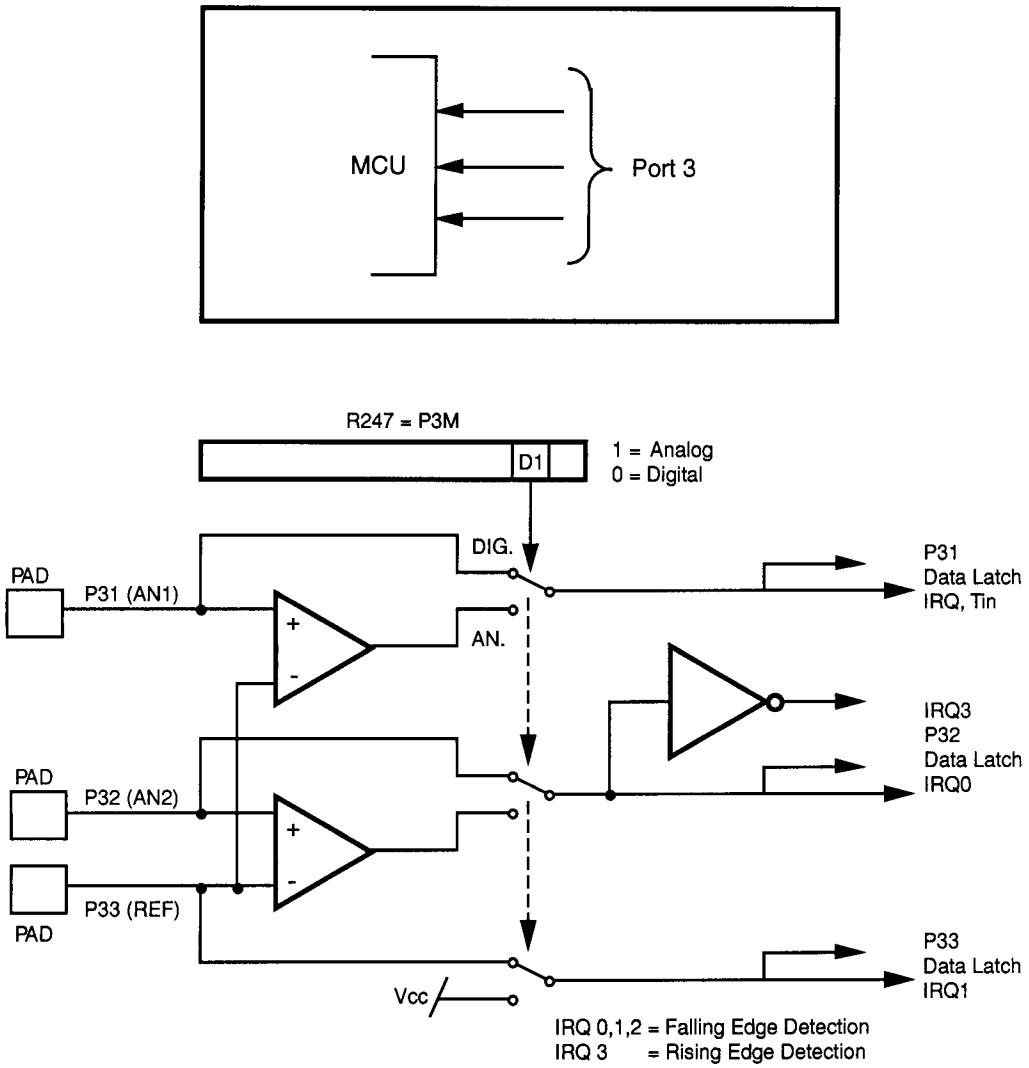


Figure 8. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility. Typical applications for these on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply that discontinues power in STOP Mode. The common voltage range is 0-4V when the V_{CC} is 5.0V. Before the comparitor outputs are valid, two NOP delays are required after enabling the analog comparitors.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternately, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

RESET. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, and then starts program execution at address %000C (Hex) (Figure 9). The device control registers' reset value is shown in Table 1.

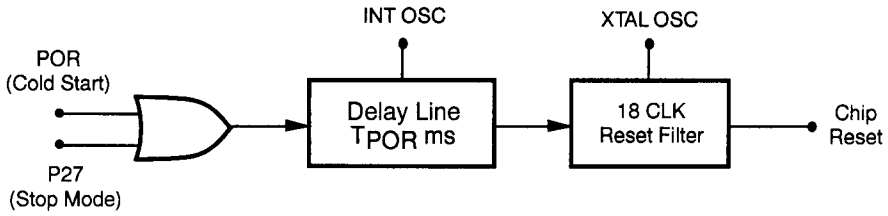


Figure 9. Internal Reset Configuration

Table 1. Z86C04/C08 & C05/C07 Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
03H (3)*	Port 3	U	U	U	U	U	U	U	U	
02H (2)*	Port 2	U	U	U	U	U	U	U	U	
00H (0)*	Port 0	U	U	U	U	U	U	U	U	
FFH(255)	SPL	0	0	0	0	0	0	0	0	
FEH (254)	GPR	0	0	0	0	0	0	0	0	
FDH (253)	RP	0	0	0	0	0	0	0	0	
FCH (252)	FLAGS	U	U	U	U	U	U	U	U	
FBH (251)	IMR	0	U	U	U	U	U	U	U	
FAH (250)	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9H (249)	IPR	U	U	U	U	U	U	U	U	
F8H (248)*	P01M	U	U	U	0	U	U	0	1	
F7H (247)*	P3M	U	U	U	U	U	U	0	0	
F6H (246)*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5H (245)	PRE0	U	U	U	U	U	U	U	0	
F4H (244)	T0	U	U	U	U	U	U	U	U	
F3H (243)	PRE1	U	U	U	U	U	U	0	0	
F2H (242)	T1	U	U	U	U	U	U	U	U	
F1H (241)	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be re-configured as shown in Table 1 and the user must avoid bus contention on the port pins or it may affect device reliability.

FUNCTIONAL DESCRIPTION (Continued)

Program Memory. The Z86C04/C08 can address up to 1K/2K bytes of internal program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1023/2047 are on-chip mask-programmed ROM.

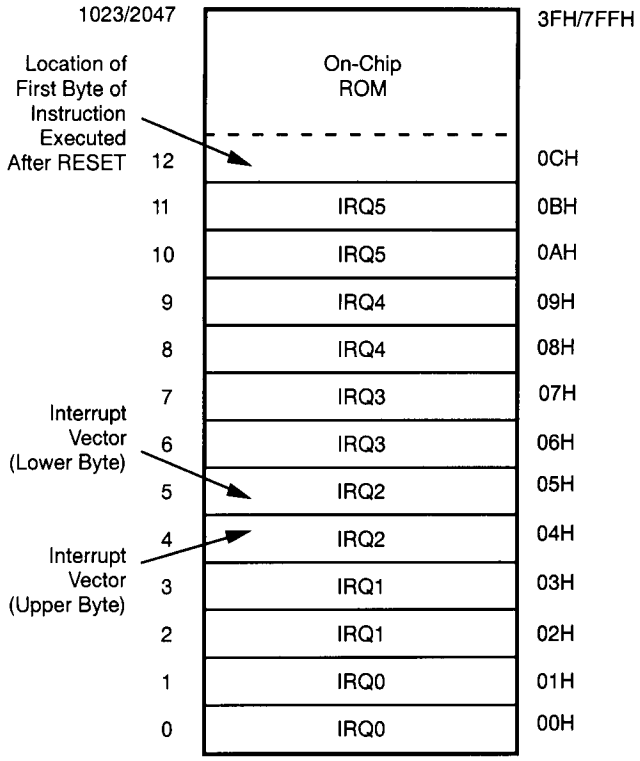


Figure 10. Program Memory Map

Register File. The Register File consists of three I/O port registers, 125 general-purpose registers, and 14 control and status registers (R0, R2-R3, R4-R127, and R241-R255, respectively; see Figure 11). Note that R254 is available for general purpose use.

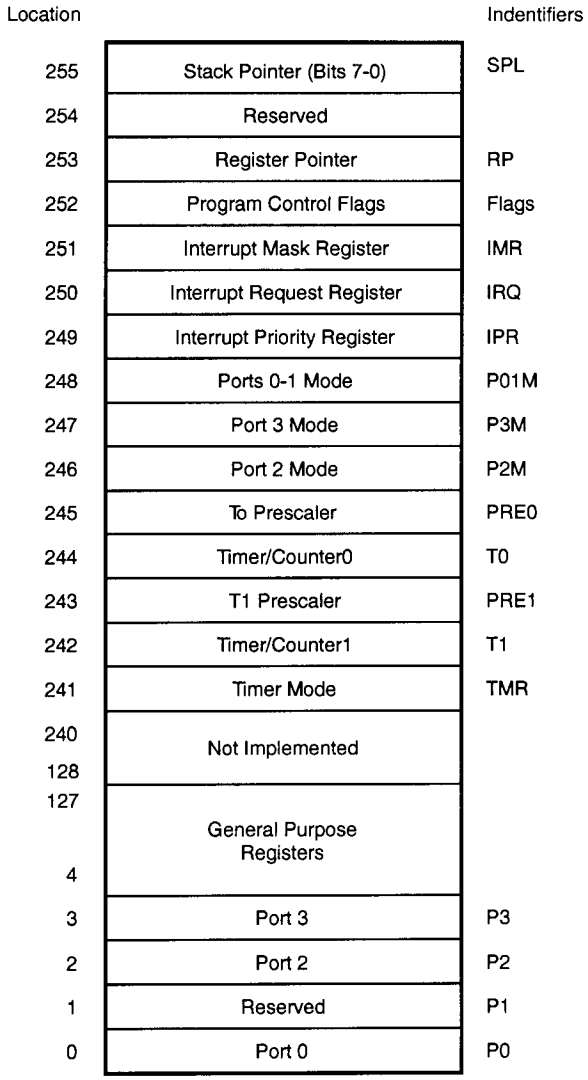


Figure 11. Register File

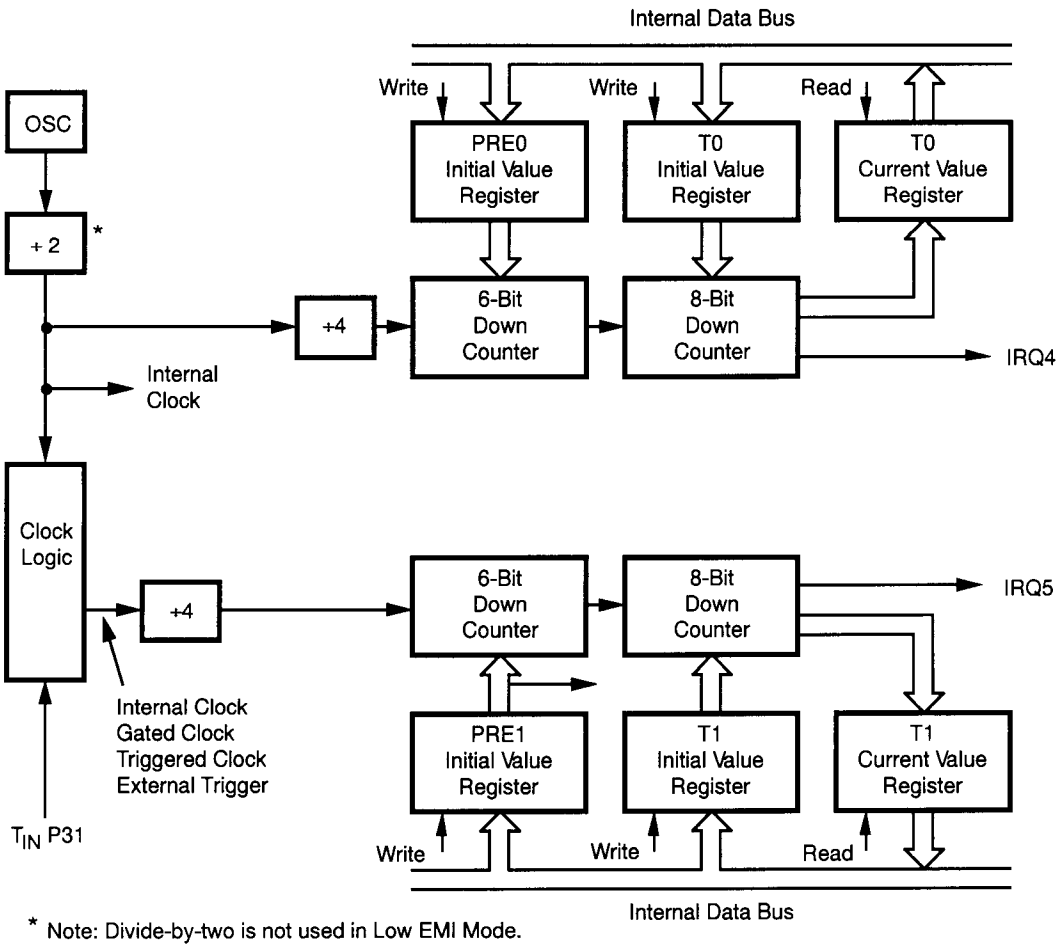
FUNCTIONAL DESCRIPTION (Continued)

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 13).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock.



* Note: Divide-by-two is not used in Low EMI Mode.

Figure 13. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a RC, crystal, ceramic resonator, LC, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitors (which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin directly to device Ground pin 14 (Figure 15).

Note that the crystal capacitor loads should be connected to V_{SS} pin 14 to reduce ground noise injection.

To use 32 kHz crystal, the 32 kHz operational mask option must be selected, and an external resistor R must be connected across XTAL1 and XTAL2.To use RC oscillator, the RC oscillator option must be selected.

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC} or dropping the V_{CC} below V_{LV}. The second method is if P27 is at a low level when the device executes the STOP instruction. A low condition on P27 releases the STOP Mode regardless if configured for input or output.

Program execution under both conditions begins at location 000C (Hex). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Note: (X = dependent upon user's application.)
In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, that is, as follows:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
            or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT should be refreshed once the WDT is enabled within every Twdt period; otherwise, the Z8 resets itself. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

WDT = 5F (Hex)

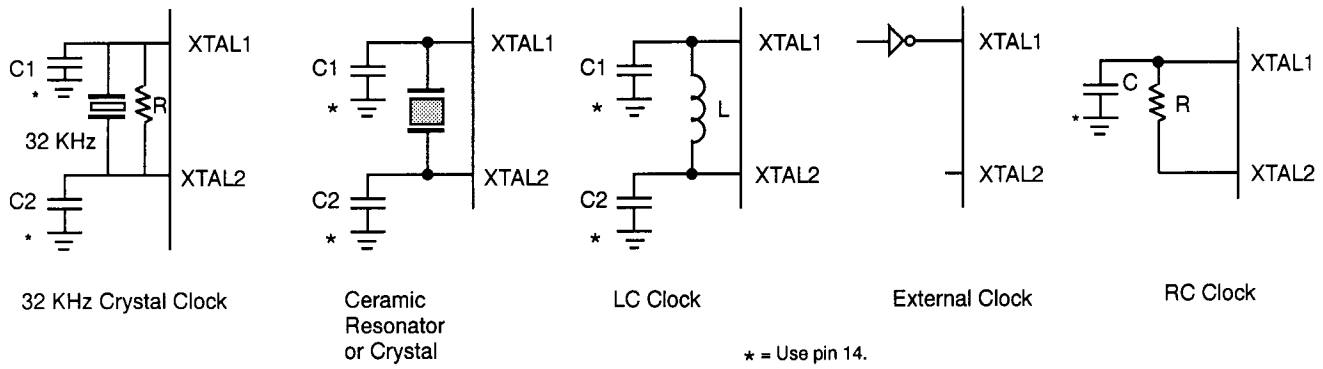


Figure 15. Oscillator Configuration

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done within the maximum T_{WDT} period; otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 XTAL clock cycles. The WDT does not work (run) in STOP Mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

Opcode WDH (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it facilitates running the WDT function during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT Mask Option. Only when the Permanent WDT Mask Option is selected, then the WDT is hardwired to be enabled after reset. The WDT will operate in Run Mode, HALT Mode, and STOP Mode. The Opcode 5FH is used to refresh or clear the WDT counter. The WDT instruction (4FH) has no effect The WDT will not run in STOP Mode if the system clock driving the WDT is selected (Z86C04 only).

System Clock Driving WDT Mask Option (Z86C04 only) When this option is selected, the Z8's system clock drives the WDT instead of the on-board RC oscillator driving the WDT. The WDT time-out will be SCLK x 32,512.The WDT will not run in STOP Mode.

Low-Voltage Protection (V_{LV}). Maximum (V_{LV}) Conditions:

Case 1: T_A= –40°C, +85°C, Internal Clock Frequency equal or less than 6 MHz

Case 2: T_A= –40°C, +105°C, Internal Clock Frequency equal or less than 4 MHz

Note: The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low-Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Cases 1 and 2. The actual low voltage trip point is a function of temperature and process parameters (Figure 16).

1 MHz (Typical)

Temp	–40C°	0°C	+25°C	+70°C	+105°C	+125°C
V_{LV}	3.0	2.75	2.6	2.3	2.1	1.9

ROM Protect. ROM Protect fully protects the Z86C04/C08 ROM code from being read internally. **When ROM Protect is selected, ROM look-up tables can be used in this mode.**

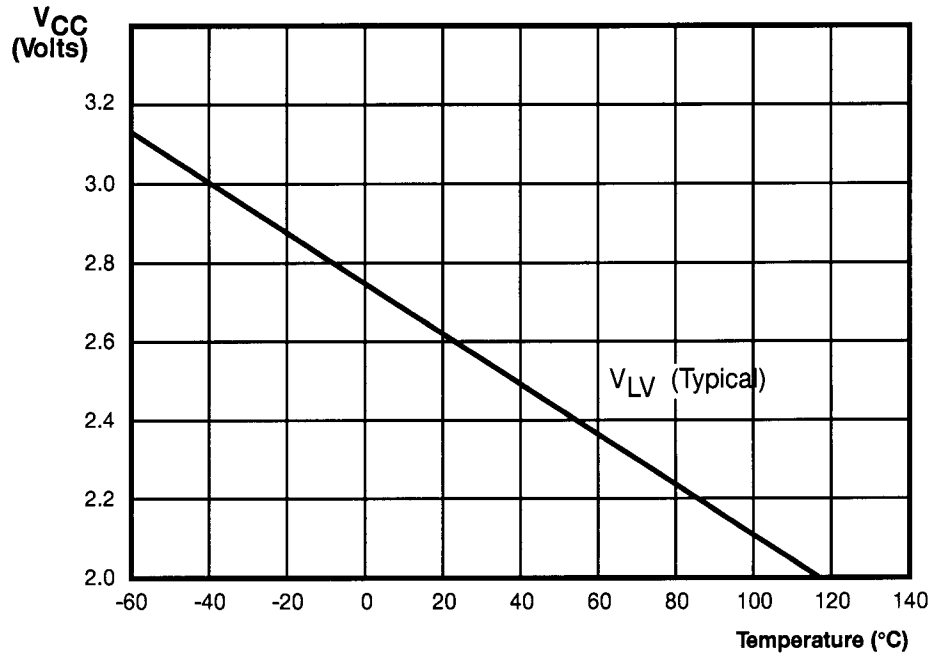


Figure 16. Typical Z86C04/C08 V_{LV} vs. Temperature

Z8 CONTROL REGISTER DIAGRAMS

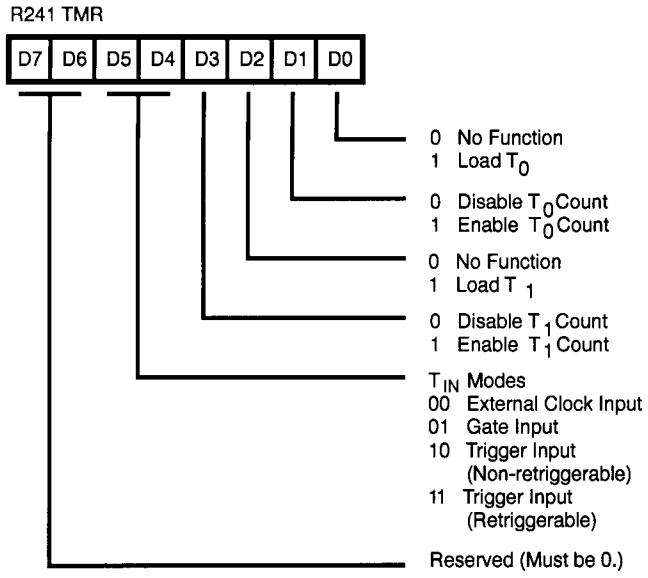


Figure 17. Timer Mode Register ($F1_H$: Read/Write)

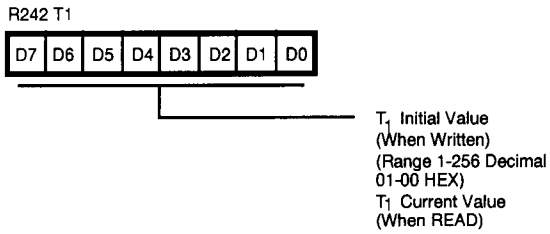


Figure 18. Counter Time 1 Register ($F2_H$: Read/Write)

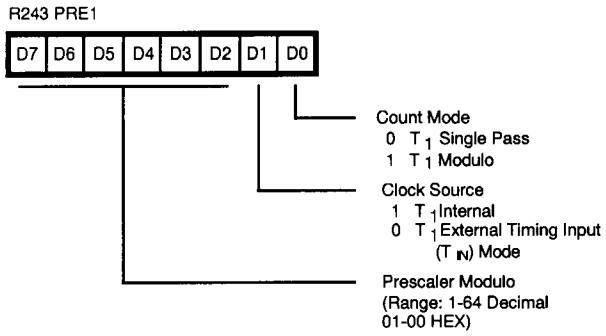


Figure 19. Prescaler 1 Register ($F3_H$: Write Only)

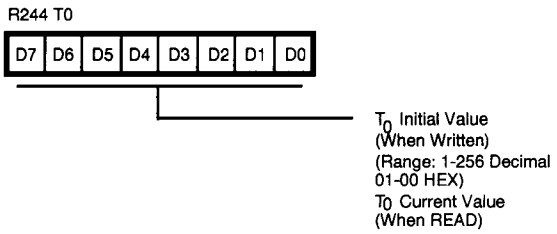


Figure 20. Counter/Timer 0 Register ($F4_H$: Read/Write)

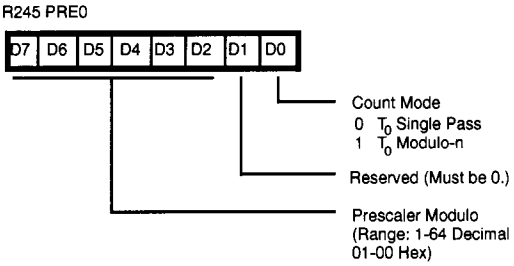


Figure 21. Prescaler 0 Register ($F5_H$: Write Only)

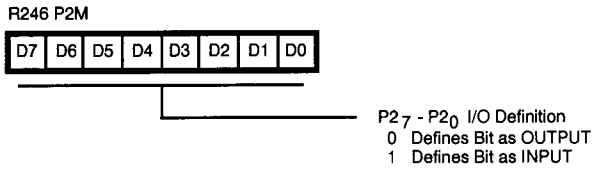


Figure 22. Port 2 Mode Register ($F6_H$: Write Only)

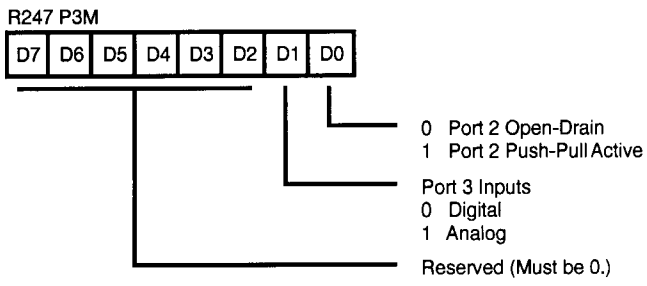


Figure 23. Port 3 Mode Register ($F7_H$: Write Only)

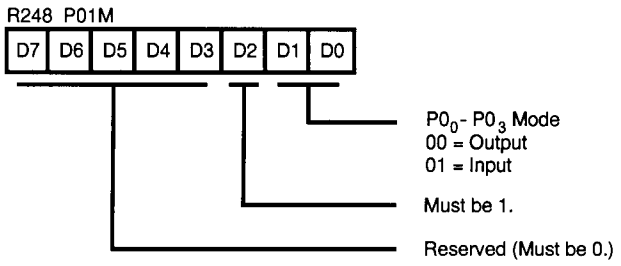


Figure 24. Port 0 and 1 Mode Register ($F8_H$: Write Only)

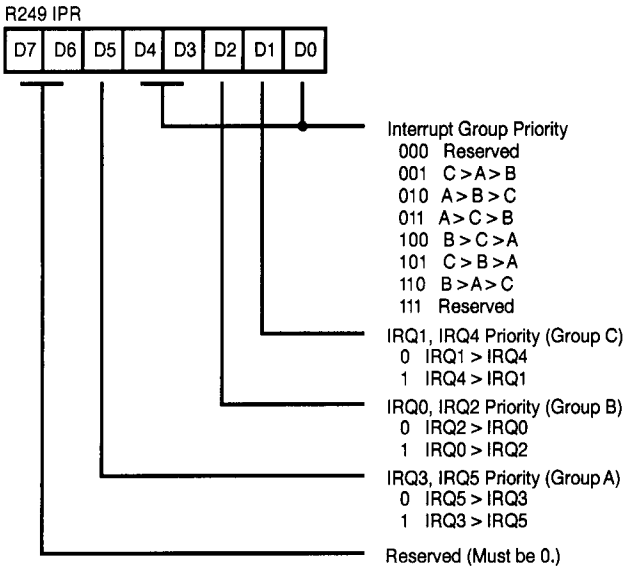


Figure 25. Interrupt Priority Register ($F9_H$: Write Only)

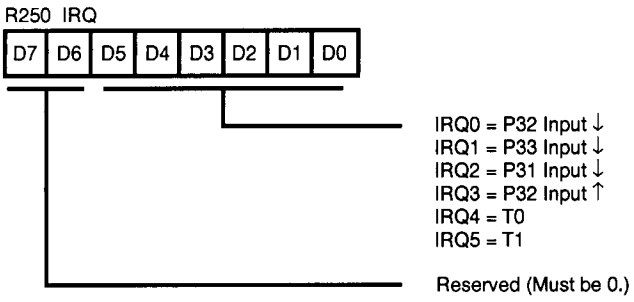


Figure 26. Interrupt Request Register (FA_H: Read/Write)

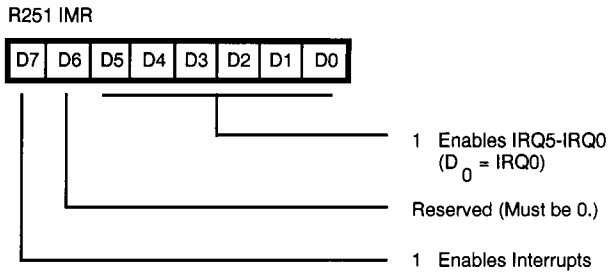


Figure 27. Interrupt Mask Register (FB_H: Read/Write)

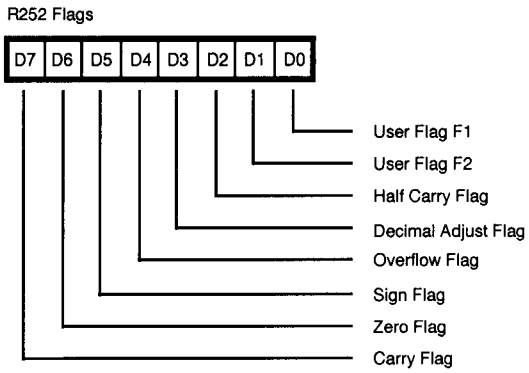


Figure 28. Flag Register (FC_H: Read/Write)

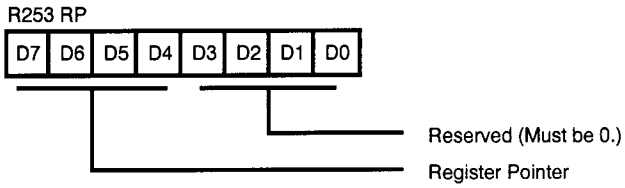


Figure 29. Register Pointer (FD_H: Read/Write)

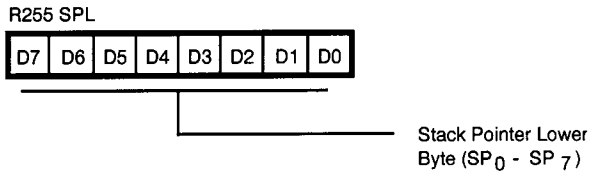


Figure 30. Stack Pointer (FF_H: Read/Write)

Standard Mode

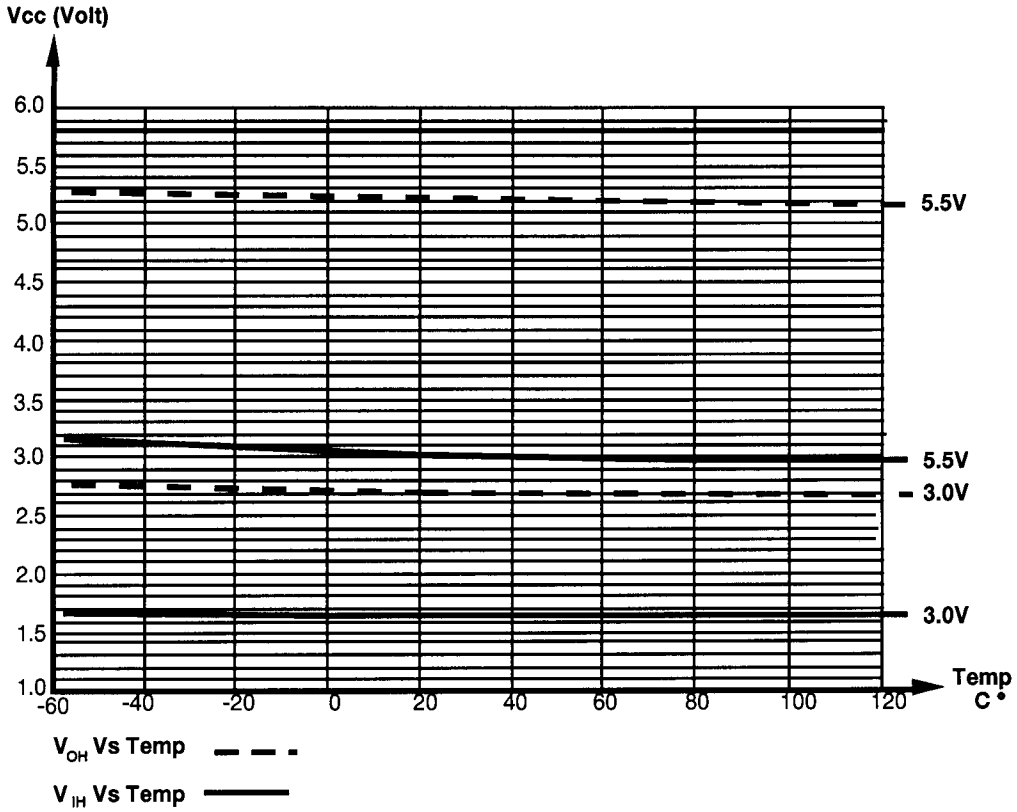


Figure 32. V_{IH}, V_{OH} vs. Temperature

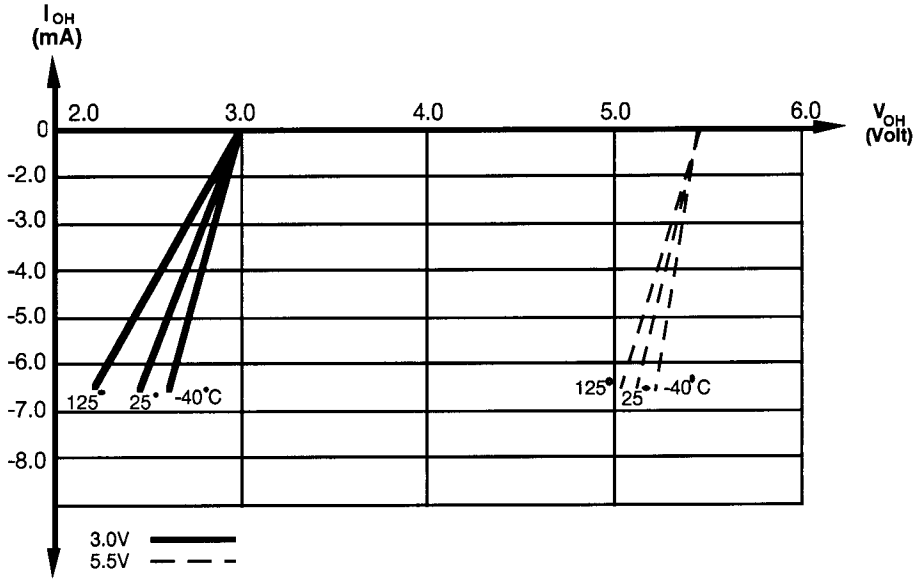


Figure 33. Typical I_{OH} vs. V_{OH}

Z8 CONTROL REGISTER DIAGRAMS (Continued)

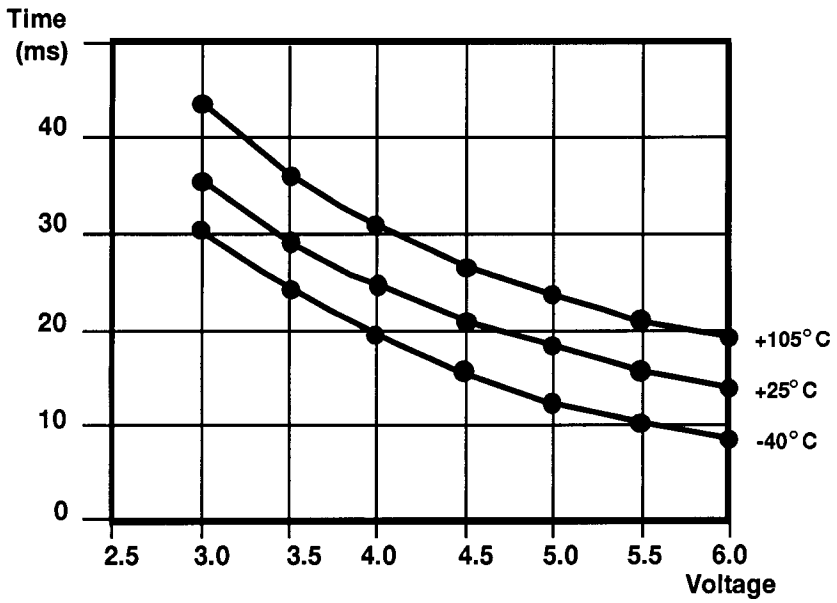
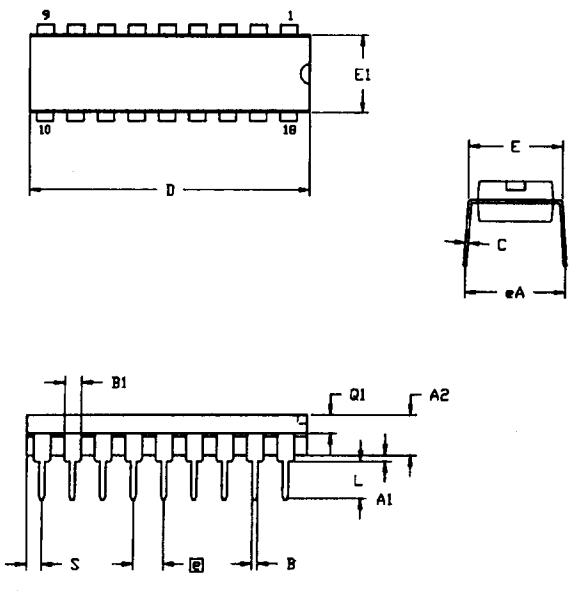


Figure 34. Typical WDT Time Out Period vs. V_{cc} Over Temperature

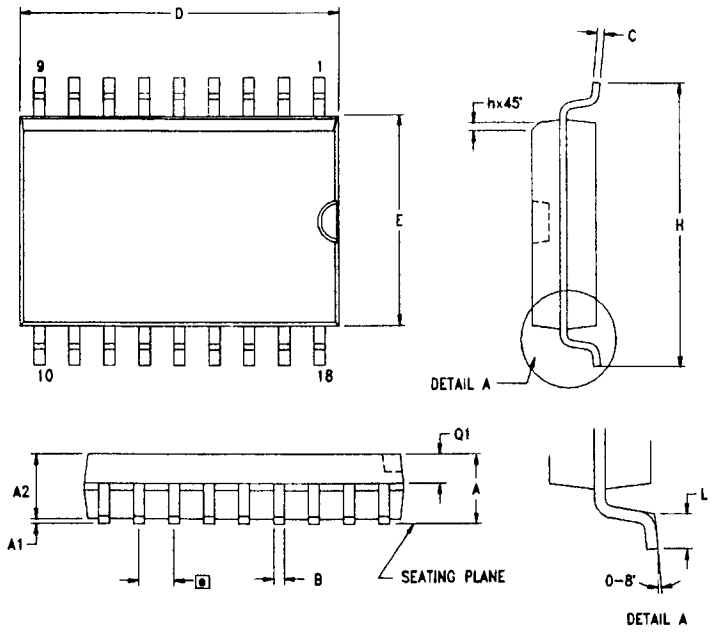
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 35. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 36. 18-Pin SOIC Package Diagram

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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