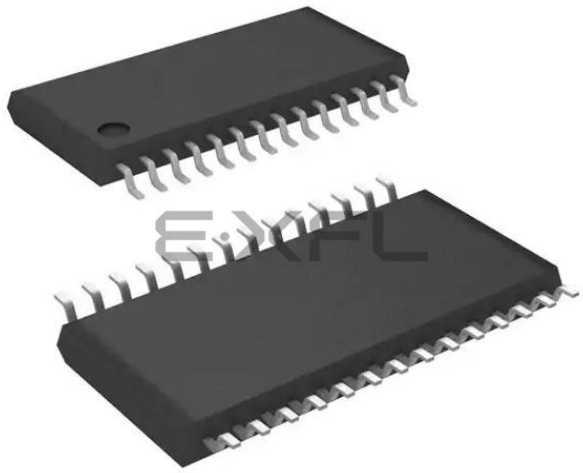

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, KPI, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e715at28

8 General 80C51 System Control

A or ACC – Accumulator (Bit-addressable)

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: E0H Reset value: 0000 0000B

Bit	Name	Description
7:0	ACC[7:0]	**Accumulator** The A or ACC register is the standard 8051 accumulator for arithmetic operation.

B – B Register (Bit-addressable)

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: F0H Reset value: 0000 0000B

Bit	Name	Description
7:0	B[7:0]	**B Register** The B register is the other accumulator of the standard 8051. It is used mainly for MUL and DIV operations.

SP – Stack Pointer

7	6	5	4	3	2	1	0
SP[7:0]							
R/W							

Address: 81H Reset value: 0000 0111B

Bit	Name	Description
7:0	SP[7:0]	**Stack Pointer** The Stack Pointer stores the scratch-pad RAM address where the stack begins. It is incremented before data is stored during PUSH or CALL instructions. Note that the default value of SP is 07H. It causes the stack to begin at location 08H.

Bit	Name	Description
5	F0	**User Flag 0** The general-purpose flag that can be set or cleared by the user.
4	RS1	**Register Bank Selecting Bits** **The two bits select one of four banks in which R0~R7 locate.** RS1 RS0 Register Bank RAM Address 0 0 0 00~07H 0 1 1 08~0FH 1 0 2 10~17H 1 1 3 18~1FH
3	RS0	
2	OV	**Overflow Flag** OV is used for a signed character operands. For an ADD or ADDC instruction, OV will be set if there is a carry out of bit 6 but not out of bit 7, or a carry out of bit 7 but not bit 6. Otherwise, OV is cleared. OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands. For a SUBB, OV is set if a borrow is needed into bit6 but not into bit 7, or into bit7 but not bit 6. Otherwise, OV is cleared. OV indicates a negative number produced when a negative value is subtracted from a positive value or a positive result when a positive number is subtracted from a negative number. For a MUL, if the product is greater than 255 (00FFH), OV will be set. Otherwise, it is cleared. For a DIV, it is normally 0. However, if B had originally contained 00H, the values returned in A and B will be undefined. Meanwhile, the OV will be set.
1	F1	**User Flag 1** The general purpose flag that can be set or cleared by the user via software.
0	P	**Parity Flag** Set to 1 to indicate an odd number of ones in the accumulator. Cleared for an even number of ones. It performs even parity check.

Table 8–1 Instructions that Affect Flag Settings

Instruction	CY	OV	AC	Instruction	CY	OV	AC
ADD	X[1]	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, /bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, /bit	X		
RRC A	X			MOV C, bit	X		

9 I/O Port Structure and Operation

For N79E715, there are **four** I/O ports – port 0, port 1, port2 and port 3. If using HIRC and reset pin configurations, the N79E715 can support up to **25** pins. All I/O pins besides P1.2 and P1.3 can be configured to one of four types by software as shown in the following table.

Table 9–1 Setting Table for I/O Ports Structure

PxM1.y	PxM2.y	Port I/O Mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

Note: P1.2 and P1.3 are not effective in this table.

After reset, these pins are in quasi-bidirectional mode except P1.2 and P1.3 pins.

The P1.2 and P1.3 are dedicating open-drain pin for I2C interface after reset.

Each I/O port of N79E715 may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P3M1 register; where n is 0, 1, 2 or 3. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n).

The P3.0 (XTAL2) can be configured as clock output when used HIRC or external crystal is clock source, and the frequency of clock output is divided by 4 HIRC clock or external crystal.

9.1 Quasi-Bidirectional Output Configuration

The default port configuration for standard N79E715 I/O ports is “Quasi-bidirectional” mode that is common on the 80C51 and most of its derivatives. This type rules as both input and output. When the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a large current. In the quasi bidirectional I/O structure, there are three pull-up transistors. Each of them serves different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch contains logic 1. The “very weak” pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the outside port pin itself is at logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting 1. If a pin that has logic 1 on it is pulled low by an external device, the “weak” pull-up turns off, and only the “very weak” pull-up remains on. To pull the pin low under these conditions, the external device has

TL2 – Timer 2 Low Byte

7	6	5	4	3	2	1	0
TL2[7:0]							
R/W							

Address: CCH Reset value: 0000 0000B

Bit	Name	Description
7:0	TL2[7:0]	**Timer 2 Low Byte** The TL2 register is the low byte of the 16-bit Timer 2.

TH2 – Timer 2 High Byte

7	6	5	4	3	2	1	0
TH2[7:0]							
R/W							

Address: CDH Reset value: 0000 0000B

Bit	Name	Description
7:0	TH2[7:0]	**Timer 2 High Byte** The TH2 register is the high byte of the 16-bit Timer 2.

Timer/Counter 2 provides three operating mode which can be selected by control bits in T2CON and T2MOD as shown in the table below. Note that the TH2 and TL2 are accessed separately. It is strongly recommended that user stop Timer 2 temporally for a reading from or writing to TH2 and TL2. The free-running reading or writing may cause unpredictable situation.

Table 10–1 Timer 2 Operating Modes

Timer 2 Mode	CP/$\overline{RL2}$ (T2CON.0)	LDEN (T2MOD.7)
Input capture	0	0
Auto-reload	0	1
Compare	1	X

10.2.1 Input Capture Mode

The input capture module with Timer 2 implements the input capture mode. Timer 2 should be configured by clearing CP/$\overline{RL2}$ and LDEN bit to enter input capture mode. The input capture module is configured through CAPCON0~2 registers. The input capture module supports 3-channel inputs (IC0, IC1, and IC2 pins) that share I/O pin P1.2, P0.7 and P2.0. Each input channel contains its own Schmitt trigger input. The noise filter for each channel is enabled via setting ENF0~2 (CAPCON2[6:4]). It filters input glitches smaller than 4 CPU clocks. Input capture 0~2 have independent edge detector but share with unique Timer 2. The trigger edge is also configured individually by setting CAPCON1. It supports positive edge capture, negative edge capture, or both edge captures. Each input capture channel has its own enabling bit CAPEN0~2 (CAPCON0[6:4]).

11 Watchdog Timer (WDT)

The N79E715 provides one Watchdog Counter to serve as a system monitor, which improve the reliability of the system. Watchdog Timer is useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. The periodic interrupt of Watchdog Timer can also serve as an event timer or a durational system supervisor in a monitoring system which generally operates in Idle or Power-down mode. The Watchdog Timer is basic a setting of divider that divides an internal low speed clock source. The divider output is selectable and determines the time-out interval. When the time-out interval is fulfilled, it will wake the system up from Idle or Power-down mode and an interrupt event will occur. If Watchdog Timer reset is enabled, a system reset will occur after a period of delay if without any software response.

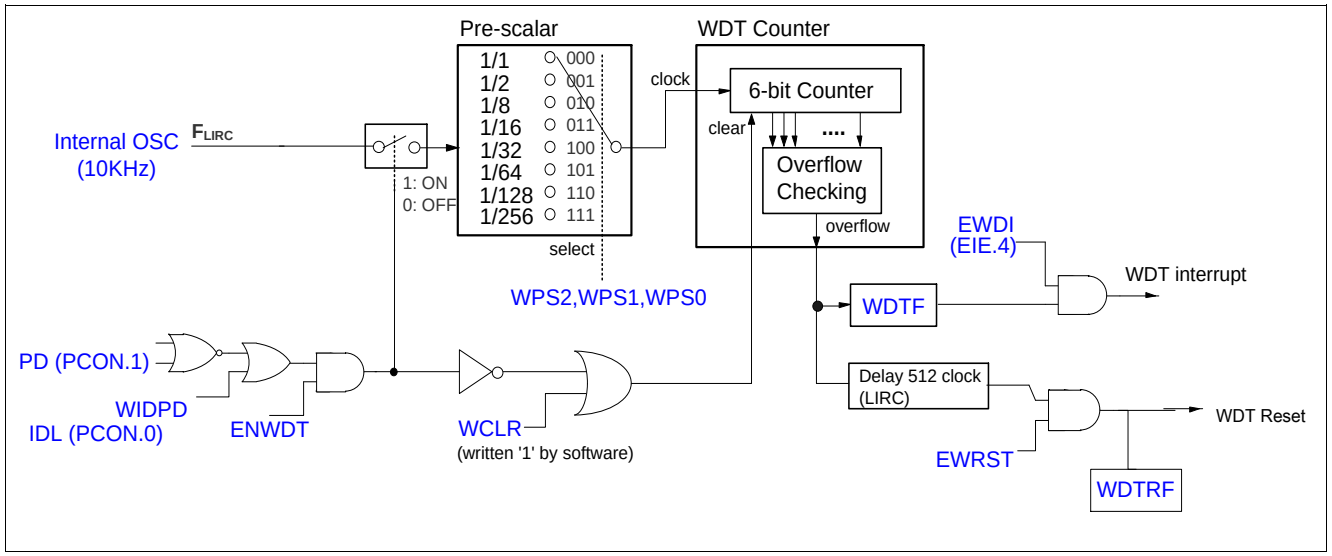


Figure 11-1 Watchdog Timer

11.1 Functional Description

The Watchdog Timer should first be reset 00H by using WDCLR(WDCON0.6) to ensure that the timer starts from a known state. After disable Watchdog Timer through clearing WDTEN (WDCON0.7) will also clear this counter. The WDCLR bit is used to reset the Watchdog Timer. This bit is self-cleared thus the user doesn't need to clear it. After writing 1 to WDCLR, the hardware will automatically clear it. After WDTEN set as 1, the Watchdog Timer starts counting. The time-out interval is selected by the three bits WPS2, WPS1, and WPS0 (WDCON0[2:0]). When the selected time-out occurs, the Watchdog Timer will set the interrupt flag WDTF (WDCON0.5). The Watchdog Timer interrupt enable bit locates at EIE.4 register. If Watchdog Timer reset is enabled by writing logic 1 to EWRST (WDCON1.0) bit. An additional 512 clocks of LIRC delays to expect a counter clearing by setting

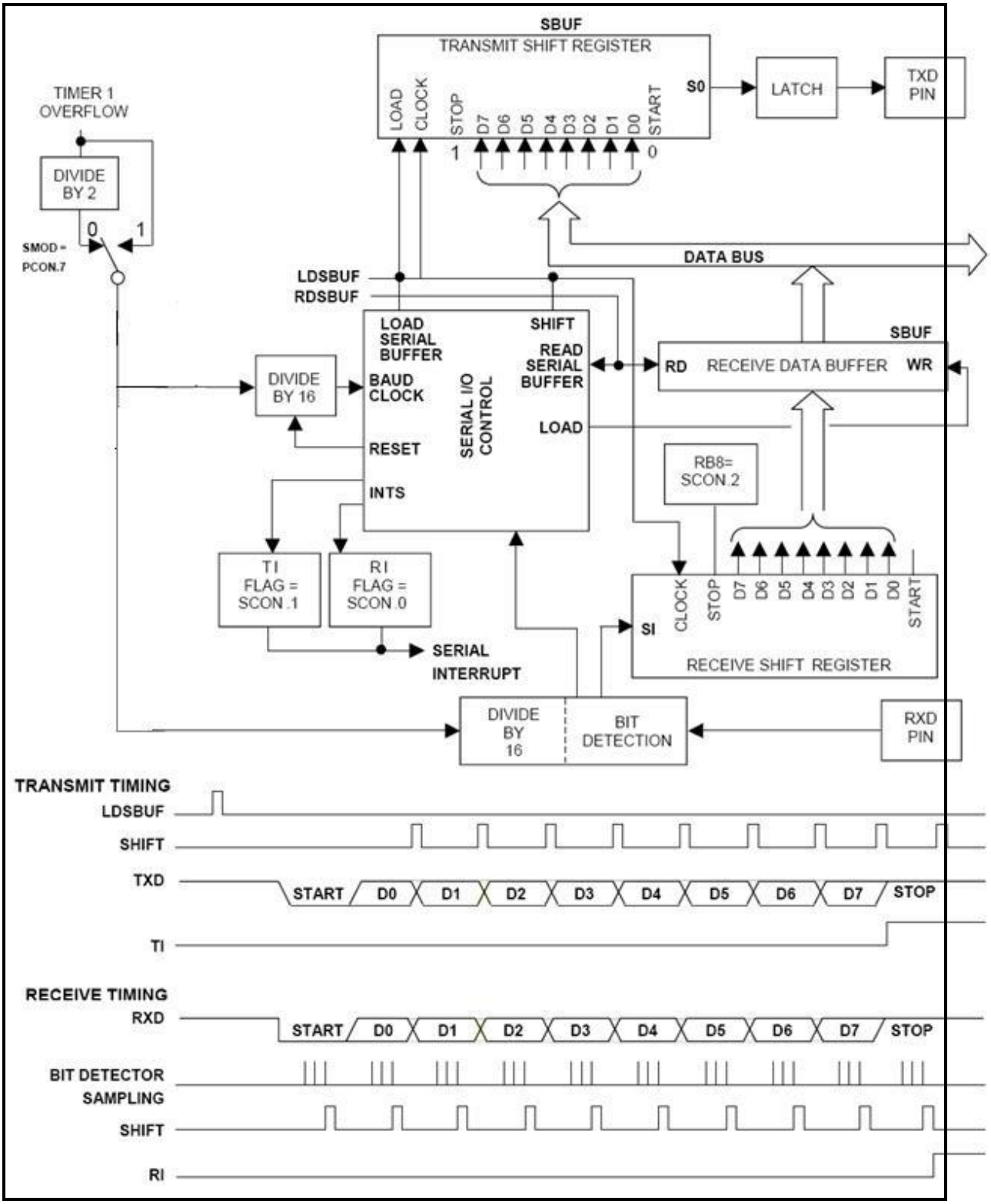


Figure 12–12-2 Serial Port Mode 1 Function Block and Timing Diagram

Figure 13–1 shows SPI block diagram and provides an overview of SPI architecture in this device. The main blocks of SPI are the SPI control register logic, SPI status logic, clock rate control logic, and pin control logic. For a serial data transfer or receiving, The SPI block exists a shift register and a read data buffer. It is single buffered in the transmit direction and double buffered in the receiving direction. Transmit data cannot be written to the shifter until the previous transfer is complete. Receiving logic consists of parallel read data buffer so the shift register is free to accept a second data, as the first received data will be transferred to the read data buffer.

The four pins of SPI interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SPCLK), and Slave Select ($\overline{SS}$). The MOSI pin is used to transfer a 8-bit data in series from the Master to the Slave. Therefore, MOSI is an output pin for Master device and a input for Slave. Respectively, the MISO is used to receive a serial data from the Slave to the Master.

The SPCLK pin is the clock output in Master mode, but is the clock input in Slave mode. The shift clock is used to synchronize the data movement both in and out of the devices through their MOSI and MISO pins. The shift clock is driven by the Master mode device for eight clock cycles which exchanges one byte data on the serial lines. For the shift clock is always produced out of the Master device, the system should never exist more than one device in Master mode for avoiding device conflict. It is strongly recommended that the Schmitt trigger input buffer be enabled.

Each Slave peripheral is selected by one Slave Select pin ($\overline{SS}$). The signal should stay low for any Slave access. When $\overline{SS}$ is driven high, the Slave device will be inactivated. If the system is multi-slave, there should be only one Slave device selected at the same time. In the Master mode MCU, the $\overline{SS}$ pin does not function and it can be configured as a general purpose I/O. However, $\overline{SS}$ can be used as Master Mode Fault detection (see Section 13.7 “Mode Fault Detection”) via software setting if multi-master environment exists. The N79E715 also provides auto-activating function to toggle $\overline{SS}$ between each byte-transfer.

SPDR – Serial Peripheral Data Register

7	6	5	4	3	2	1	0
SPDR[7:0]							
R/W							

Address: F5H Reset value: 0000 0000B

Bit	Name	Description
7:0	SPDR[7:0]	**Serial Peripheral Data** This byte is used for transmitting or receiving data on SPI bus. A write of this byte is a write to the shift register. A read of this byte is actually a read of the read data buffer. In Master mode, a write to this register initiates transmission and reception of a byte simultaneously.

13.4 Operating Modes

13.4.1 Master Mode

The SPI can operate in Master mode while MSTR (SPCR.4) is set as 1. Only one Master SPI device can initiate transmissions. A transmission always begins by Master through writing to SPDR. The byte written to SPDR begins shifting out on MOSI pin under the control of SPCLK. Simultaneously, another byte shifts in from the Slave on the MISO pin. After 8-bit data transfer complete, SPIF (SPSR.7) will automatically set via hardware to indicate one byte data transfer complete. At the same time, the data received from the Slave is also transferred in SPDR. The user can clear SPIF and read data out of SPDR.

13.4.2 Slave Mode

When MSTR is 0, the SPI operates in Slave mode. The SPCLK pin becomes input and it will be clocked by another Master SPI device. The $\overline{SS}$ pin also becomes input. The Master device cannot exchange data with the Slave device until the $\overline{SS}$ pin of the Slave device is externally pulled low. Before data transmissions occurs, the $\overline{SS}$ of the Slave device should be pulled and remain low until the transmission is complete. If $\overline{SS}$ goes high, the SPI is forced into idle state. If the $\overline{SS}$ is force to high at the middle of transmission, the transmission will be aborted and the rest bits of the receiving shifter buffer will be high and goes into idle state.

In Slave mode, data flows from the Master to the Slave on MOSI pin and flows from the Slave to the Master on MISO pin. The data enters the shift register under the control of the SPCLK from the Master device. After one byte is received in the shift register, it is immediately moved into the read data buffer and the SPIF bit is set. A read of the SPDR is actually a read of the read data buffer. To prevent an

Table 14–1 Configuration for Different KBI Level Selection

KBLS1.n	KBLS0.n	KBI Channel n Type
0	0	Falling edge
0	1	Rising edge
1	0	Either falling or rising edge
1	1	Low level

KBIE – Keyboard Interrupt Enable Register

7	6	5	4	3	2	1	0
KBIE.7	KBIE.6	KBIE.5	KBIE.4	KBIE.3	KBIE.3	KBIE.1	KBIE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: E9H Reset value: 0000 0000B

Bit	Name	Description
7:0	KBIE	**Keyboard Interrupt** Enable P0[7:0] as a cause of a Keyboard interrupt.

KBIF – Keyboard Interface Flags

7	6	5	4	3	2	1	0
KBIF[7:0]							
R (level) R/W (edge)							

Address: EAH Reset value: 0000 0000B

Bit	Name	Description
7:0	KBIFn	**Keyboard Interface Channel n Flag** If any edge trigger mode of KBI is selected, this flag will be set by hardware if KBI channel n (P0.n) detects a type defined edge. This flag should be cleared by software. If the low level trigger mode of KBI is selected, this flag follows the inverse of the input signal's logic level on KBI channel n (P0.n)l. Software cannot control it.

KBLS0 – Keyboard Level Select 0[1]

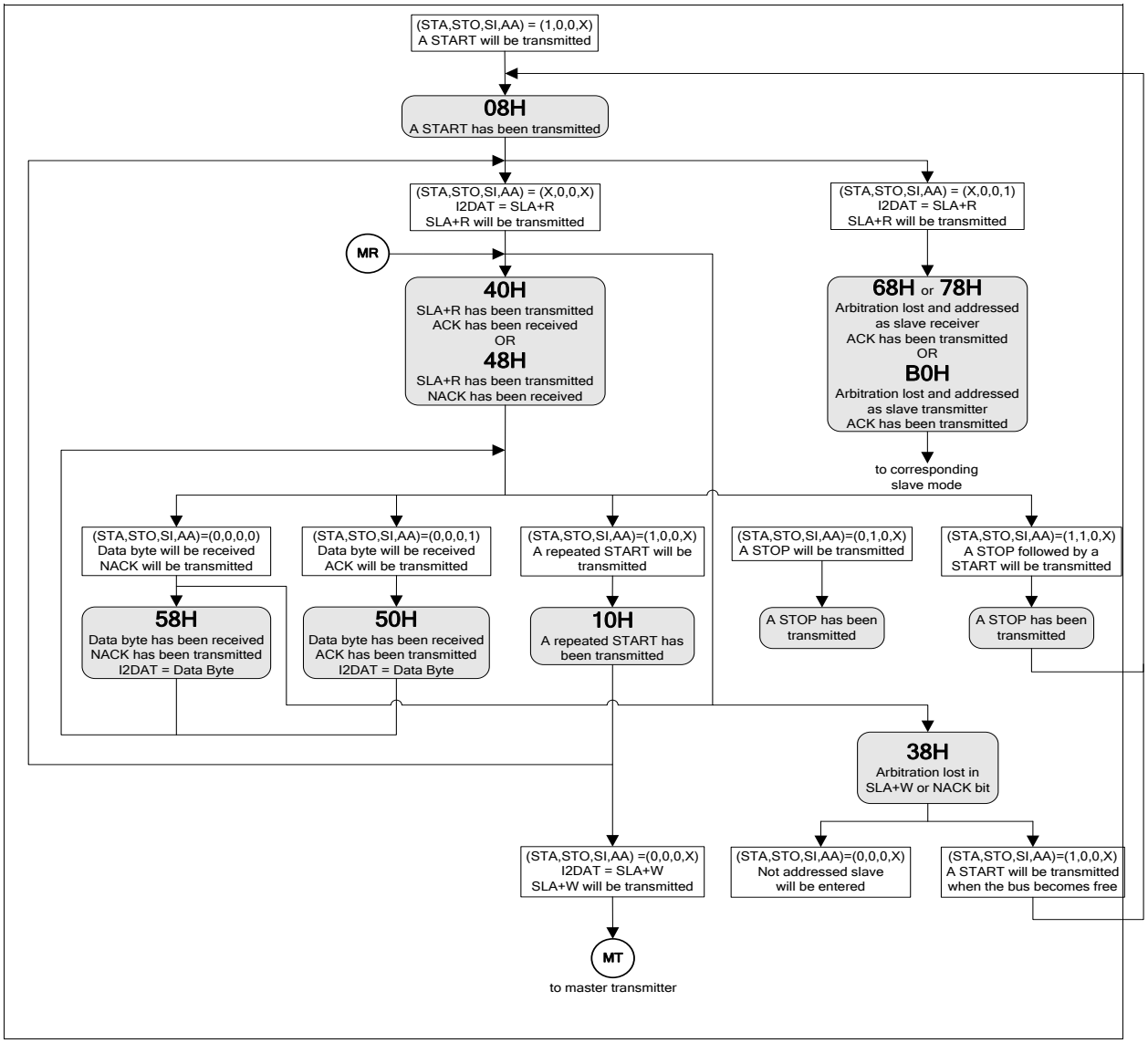
7	6	5	4	3	2	1	0
KBLS0[7:0]							
R/W							

Address: EBH Reset value: 0000 0000B

Bit	Name	Description
7:0	KBLS0[7:0]	**Keyboard Level Select 0**

16.4.2 Master Receiver Mode

In Master Receiver mode, several bytes of data are received from a slave transmitter. The transaction is initialized just as the master transmitter mode. Following the START condition, I2DAT should be loaded with the target slave address and the data direction bit “read” (SLA+R). After the SLA+R byte is transmitted and an acknowledge bit has been returned, the SI flag is set again and I2STA is read as 40H. SI flag should then be cleared to receive data from the slave transmitter. If AA flag (I2CON.3) is set, the master receiver will acknowledge the slave transmitter. If AA is cleared, the master receiver will not acknowledge the slave and release the slave transmitter as a not addressed slave. After that, the master can generate a STOP condition or a repeated START condition to terminate the transmission or initial another one.



16.6 I²C Time-out

There is a 14-bit time-out counter which can be used to deal with the I²C bus hang-up. If the time-out counter is enabled, the counter starts up counting until it overflows. Meanwhile TIF will be set by hardware and requests I²C interrupt. When time-out counter is enabled, setting flag SI to high will reset counter and restart counting up after SI is cleared. If the I²C bus hangs up, it causes the SI flag not set for a period. The 14-bit time-out counter will overflow and require the interrupt service.

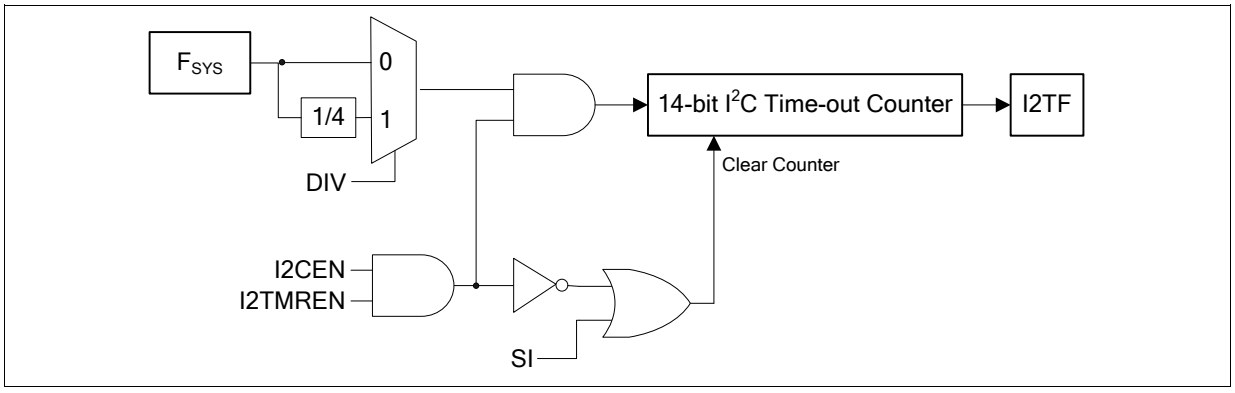


Figure 16-12 I²C Time-out Count

I2TOC – I²C Time-out Counter

7	6	5	4	3	2	1	0
-	-	-	-	-	I2TOCEN	DIV	I2TOF
-	-	-	-	-	R/W	R/W	R/W

Address: BFH Reset value: 0000 0000B

Bit	Name	Description
7:3	-	**Reserved**
2	I2TOCEN	**I²C Time-out Counter Enable** 0 = The I²C time-out counter is disabled. 1 = The I²C time-out counter is enabled.
1	DIV	**I²C time-out Counter Clock Divider** 0 = The divider of I²C time-out counter is 1/1 of F_{SYS}. 1 = The divider of I²C time-out counter is 1/4 of F_{SYS}.
0	I2TOF	**I²C Time-out Counter Overflow Flag** I2TOF flag is set by hardware if 14-bit I²C time-out counter overflows. I2TOF flag is cleared by software.

16.7 I²C Interrupts

There are two I²C flags, SI and I2TOF. Both of them can generate an I²C event interrupt requests. If I²C interrupt mask is enabled via setting EI2C (EIE.0) and EA is 1, CPU will executes the I²C interrupt

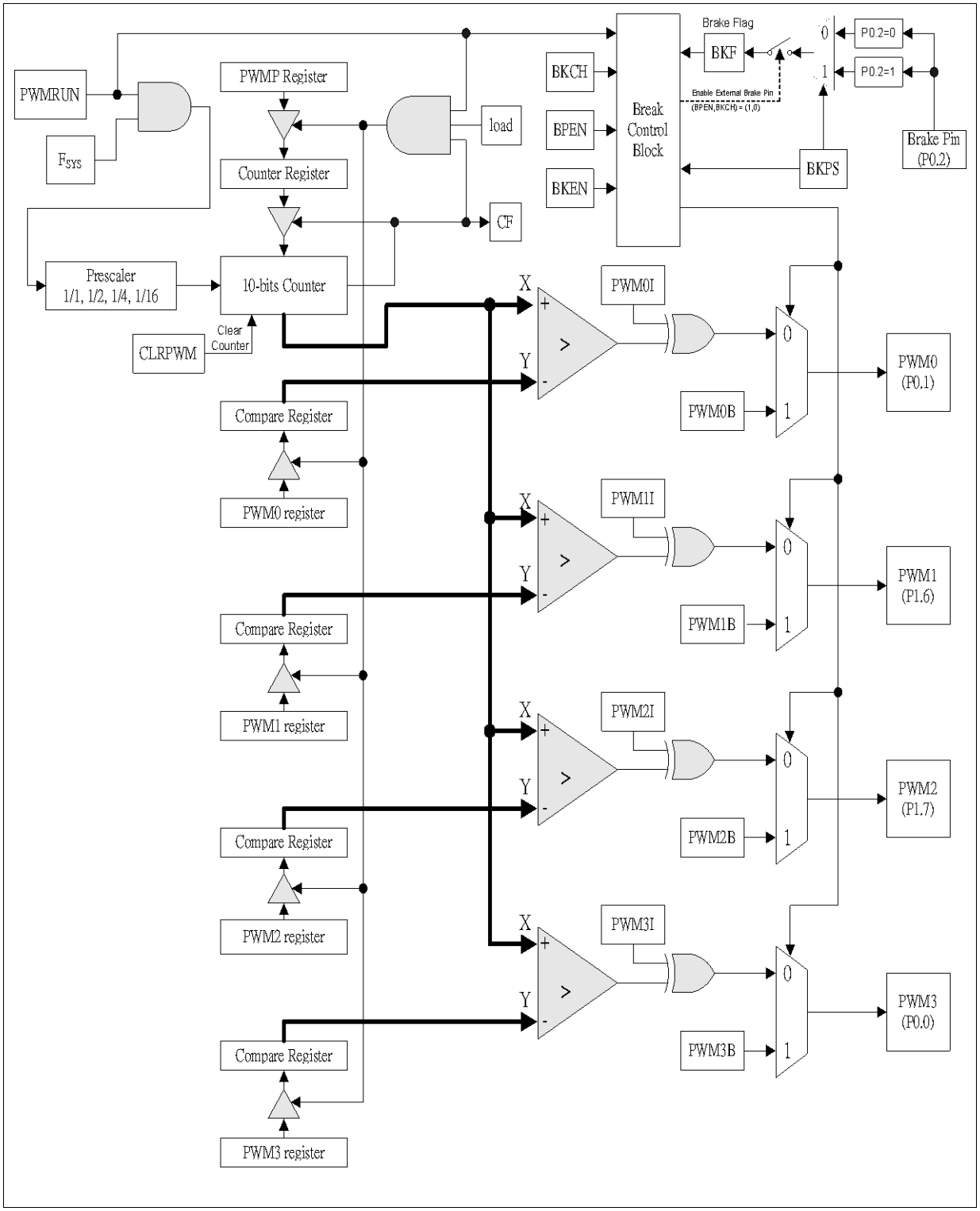


Figure 17-1 PWM Block Diagram

A compare value greater than the counter reloaded value is in the PWM output being permanently low. In addition, there are two special cases. A compare value of all zeroes, 000H, causes the output

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: DFH Reset value: 0000 0000B

Bit	Name	Description
7	BKCH	See the following table (when BKEN is set).
6	BKPS	0 = Brake is asserted if P0.2 is low. 1 = Brake is asserted if P0.2 is high
5	BPEN	See the following table (when BKEN is set).
4	BKEN	0 = Brake is never asserted. 1 = Brake is enabled, and see the following table.
3	PWM3B	0 = PWM3 output is low, when Brake is asserted. 1 = PWM3 output is high, when Brake is asserted.
2	PWM2B	0 = PWM2 output is low, when Brake is asserted. 1 = PWM2 output is high, when Brake is asserted.
1	PWM1B	0 = PWM1 output is low, when Brake is asserted. 1 = PWM1 output is high, when Brake is asserted.
0	PWM0B	0 = PWM0 output is low, when Brake is asserted. 1 = PWM0 output is high, when Brake is asserted.

Brake Condition Table

BPEN	BKCH	BREAK CONDITIONS
0	0	Brake on (software brake and keeping brake)
0	1	On, when PWM is not running (PWMRUN=0), the PWM output condition is follow PWMNB setting. Off, when PWM is running (PWMRUN=1).
1	0	Brake on, when break pin asserted, no PWM output, the bit of PWMRUN will be cleared and BKF flag will be set. The PWM output condition is follow PWMNB setting.
1	1	Not active.

PWMCON2 – PWM Control Register 2

7	6	5	4	3	2	1	0
-	-	-	-	FP1	FP0	-	BKF
-	-	-	-	R/W	R/W	-	R/W

Address: D7H Reset value: 0000 0000B

Bit	Name	Description
7:4	-	**Reserved**

Bit	Name	Description
0	BOS	**BOD Status** 1 = V_{DD} voltage level is higher than V_{BOD}. 0 = V_{DD} voltage level is lower than V_{BOD}.

24.3 RST Pin Reset

The hardware reset input is RST pin which is the input with a Schmitt trigger. A hardware reset is accomplished by holding the RST pin low for at least two machine-cycles to ensure detection of a valid hardware reset signal. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST pin is 1. After the RST low is removed, the CPU will exit the reset state with in two machine-cycles and begin code executing from address 0000H. There is no flag associated with the RST pin reset condition. However since the other reset sources have flags, the external reset can be considered as the default reset if those reset flags are cleared.

If a RST pin reset applies while CPU is in Power-down mode, the way to trigger a hardware reset is slightly different. Since the Power-down mode stops clock system, the reset signal will asynchronously cause the clock system resuming. After the clock system is stable, CPU will enter the reset state, then exit and start to execute program code from address 0000H.

Note: After the CPU is released from all reset state, the hardware will always check the BS bit instead of the CBS bit to determine from APROM or LDROM that the device reboots.

24.4 Watchdog Timer Reset

The Watchdog Timer is a free running timer with programmable time-out intervals. The user can clear the Watchdog Timer at any time, causing it to restart the count. When the selected time-out occurs, the Watchdog Timer will reset the system directly. The reset condition is maintained via hardware for two machine-cycles. After the reset is removed the device will begin execution from 0000H.

Once a reset due to Watchdog Timer occurs the Watchdog Timer reset flag WDTRF (WDCON0.3) will be set. This bit keeps unchanged after any reset other than a power-on reset. The user may clear WDTRF via software.

CHPCON – Chip Control (TA Protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	-	-	-	BS	ISPEN
W	R/W	R/W	-	-	-	R/W	R/W

Address: 9FH Reset value: see Table 7–2 N79E715 SFR Description and Reset Values

Bit	Name	Description
7	SWRST	**Software Reset** Setting this bit as logic 1 will cause a software reset. It will automatically be cleared via hardware after reset in finished.

The software demo code is listed below.

```
CLR EA                    ;If any interrupt is enabled, disable temporarily
MOV TA,#0AAh              ;TA protection.
MOV TA,#55h               ;
ANL CHPCON,#0FDh          ;BS = 0, reset to APROM.
MOV TA,#0AAh
MOV TA,#55h
ORL CHPCON,#80h           ;Software reset
```

24.6 Boot Selection

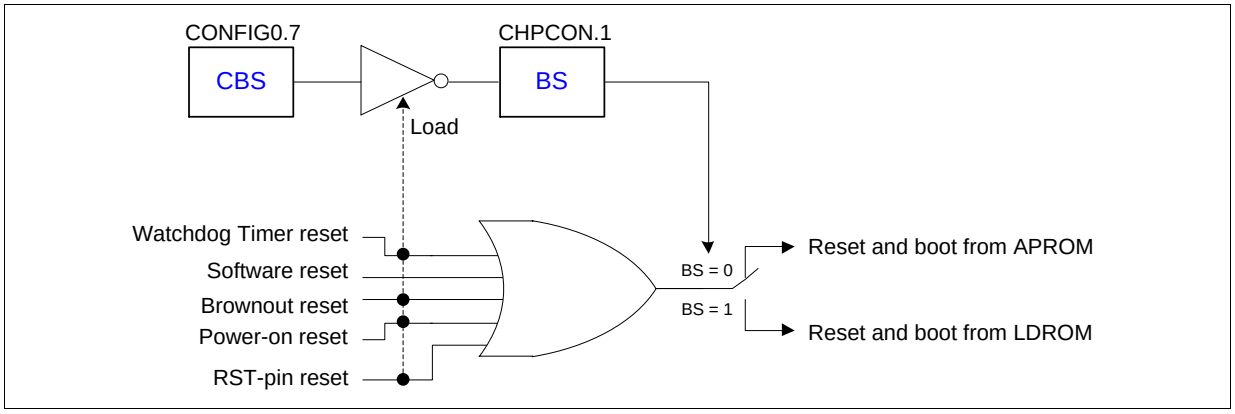


Figure 24-1 Boot Selection Diagram

The N79E715 provides user a flexible boot selection for variant application. The SFR bit BS in CHPCON.1 determines CPU booting from APROM or LDROM after any source of reset. If reset occurs and BS is 0, CPU will reboot from APPROM. Else, the CPU will reboot from LDROM.

25 CONFIG Bits (CONFIG)

The N79E715 has several hardware configuration bytes, called CONFIG bits, which are used to configure the hardware options such as the security bits, clock system source, and so on. These hardware options can be re-configured through the Programmer/Writer or ISP modes. N79E715 have four CONFIG bits those are CONFIG0~3. Several functions which are defined by certain CONFIG bits are also available to be re-configured by certain SFR bits. Therefore, there is a need to LOAD such CONFIG bits into respective SFR bits. Such loading will occurs after resets. (Software reset will reload all CONFIG bits except CBS bit in CONFIG0.7) These SFR bits can be continuously controlled via user's software. Other resets will remain the values in these SFR bits unchanged.

Note: CONFIG bits marked as "-" should always keep unprogrammed.

25.1 CONFIG0

7	6	5	4	3	2	1	0
CBS	-	-	-	-	-	LOCK	DFEN
R/W	-	-	-	-	-	R/W	R/W

Factory default value: 1111 1111B

Bit	Name	Description
7	CBS	**CONFIG Boot Selection** This bit defines from which block MCU boots after all resets except software reset. 1 = MCU will boot from APROM after all resets except software reset. 0 = MCU will boot from LDROM after all resets except software reset.
6:2	-	**Reserved**

Bit	Name	Description
1	LOCK	**Chip Lock Enable** 1 = Chip is unlocked. All of APROM, LDROM, and Data Flash are not locked. Their contents can be read out through a parallel Programmer/Writer. 0 = Chip is locked. APROM, LDROM, and Data Flash are locked. Their contents read through parallel Programmer/Writer will become FFH. Note that CONFIG bytes are always unlocked and can be read. Hence, once the chip is locked, the CONFIG bytes cannot be erased or programmed individually. The only way to disable chip lock is to use the whole chip erase mode. However, all data within APROM, LDROM, Data Flash, and other CONFIG bits will be erased when this procedure is executed. If the chip is locked, it does not alter the ISP function.
0	DFEN	**Data Flash Enable** 1 = There is no Data Flash space. The APROM size is 16 Kbytes. 0 = Data Flash exists. The Data Flash and APROM share 16 Kbytes depending on SHBDA settings.

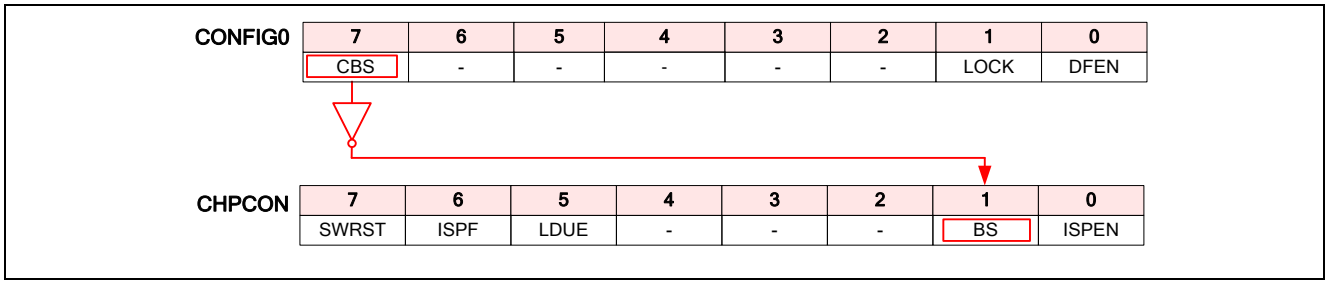


Figure 25-1 CONFIG0 Reset Reloading Except Software Reset

25.2 CONFIG1

7	6	5	4	3	2	1	0
CHBDA[7:0][1]							
R/W							

Factory default value: 1111 1111B

Bit	Name	Description
7:0	CHBDA[7:0]	**CONFIG High Byte of Data Flash Starting Address** This byte is valid only when DFEN (CONFIG0.0) is 0. It is used to determine the starting address of the Data Flash.

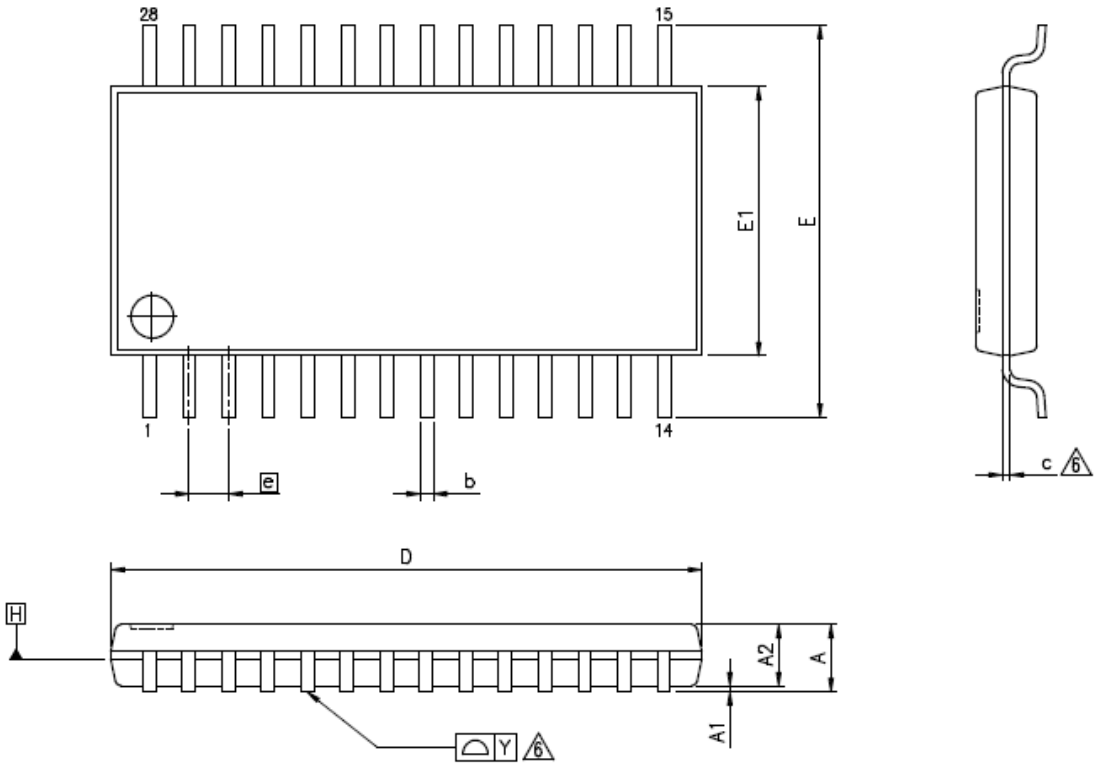
[1]: There will be no APROM if setting CHBDA 00H. CPU will execute codes in minimum size(256B) of internal Program Memory.

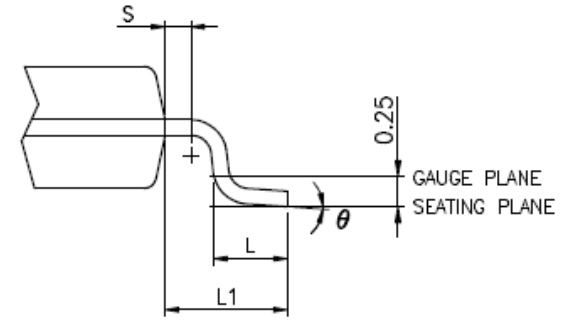
Table 28–3 DC Characteristics

(V_{DD}–V_{SS} = 2.4~5.5V, TA = -40°C ~+85°C, unless otherwise specified.)

Sym	Parameter	Test Conditions	MIN	TYP	MAX	Unit
		F_{SYS} = 24 MHz, V_{DD} = 5.5V		**3.7**		mA
		F_{SYS} = 12 MHz, V_{DD} = 3.3V		**1.3**		mA
		F_{SYS} = 24 MHz, V_{DD} = 3.3V		**2.3**		mA
		F_{SYS} = 22.1184 MHz, V_{DD} = 5V		**1.6**		mA
		F_{SYS} = 22.1184 MHz, V_{DD} = 3.3V		**1.6**		mA
I_{PD}	Power-down mode			**<10**		µA
	Power-down mode(BOD Enable)			**100**		µA
R_{RST}	RST-pin Internal Pull-High Resistor	2.4V < V_{DD} < 5.5V	**100**		**250**	KΩ
V_{BOD38}	BOD38 Detect Voltage (Temp.=25℃)		**3.5**	**3.8**	**4.1**	V
	BOD38 Detect Voltage (Temp.=85℃)		**3.5**	**3.8**	**4.9**	V
	BOD38 Detect Voltage (Temp.=-40℃)		**3.0**	**3.8**	**4.1**	V
V_{BOD27}	BOD27 Detect Voltage (Temp.=25℃)		**2.5**	**2.7**	**2.9**	V
	BOD27 Detect Voltage (Temp.=85℃)		**2.5**	**2.7**	**3.1**	V
	BOD27 Detect Voltage (Temp.=-40℃)		**2.4**	**2.7**	**2.9**	V

30.2 28-pin TSSOP - 4.4X9.7 mm

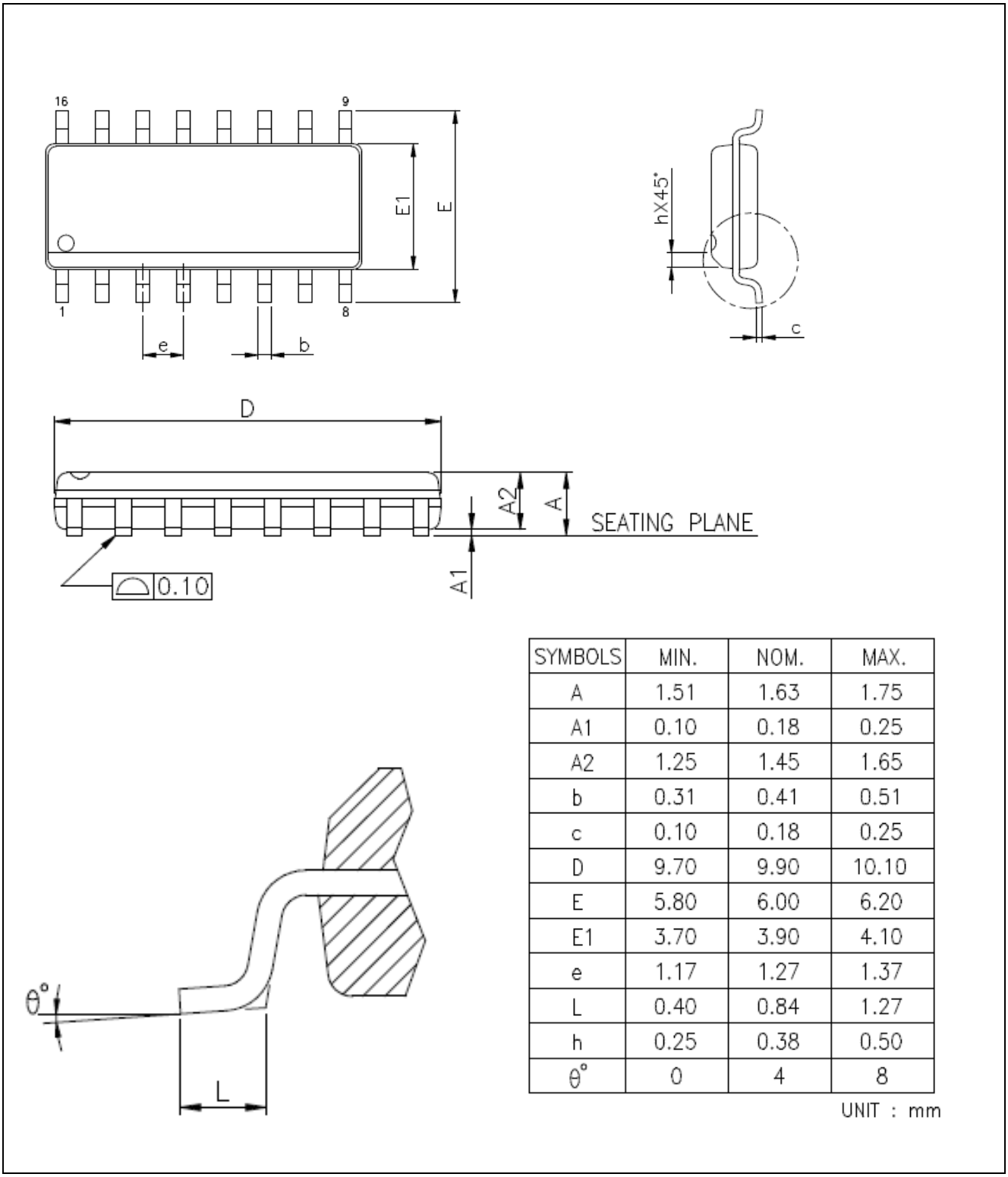




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

30.5 16-pin SOP - 150 mil



SYMBOLS	MIN.	NOM.	MAX.
A	1.51	1.63	1.75
A1	0.10	0.18	0.25
A2	1.25	1.45	1.65
b	0.31	0.41	0.51
c	0.10	0.18	0.25
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.17	1.27	1.37
L	0.40	0.84	1.27
h	0.25	0.38	0.50
θ°	0	4	8

UNIT : mm