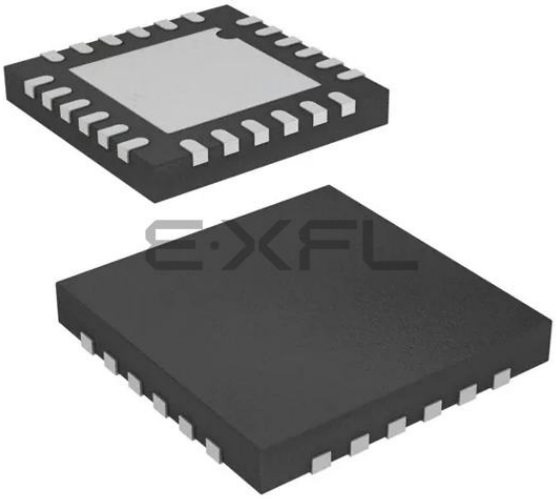


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART
Number of I/O	12
Voltage - Supply	3V ~ 24.5V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3171-24lqxq

Contents

priate voltage on VBUS pin as per the negotiated contract with the peer device over Type-C.

Integrated Digital Blocks

Serial Communication Blocks (SCB)

EZ-PD CCG3PA has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG3PA and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on the SCB blocks of EZ-PD CCG3PA are not completely compliant with the I^2C spec in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3PA has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

I/O Subsystem

EZ-PD CCG3PA has up to 12 GPIOs of which, some of them can be re-purposed to support functions of SCB (I^2C, UART, SPI). GPIO pins P0.0 and P0.1 are overvoltage-tolerant (OVT) (upto 7V).

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate Fault for OCP/SCP/OVP/UVP conditions. Any two fault conditions can be mapped to two GPIOs or all the four faults can be OR'ed to indicate over one GPIO.

Power Systems Overview

CCG3PA can operate from two possible external supply sources: VBUS_IN_DISCHARGE (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS_IN_DISCHARGE, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. CCG3PA has three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS_IN_DISCHARGE pin, VDDD cannot be used to power external devices and should be connected to a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 1. CCG3PA Power Modes

Mode	Description
Power-On Reset (POR)	Power is valid and an internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available.

Figure 1. Power System Requirement Block Diagram

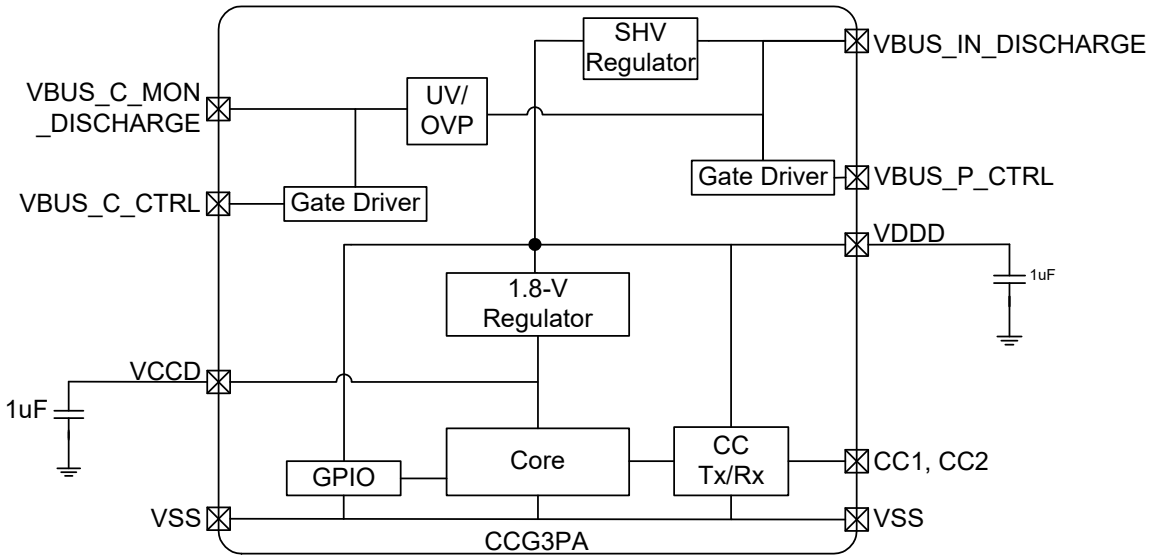


Table 3. GPIO Ports, Pins and Their Functionality

Port	24-QFN	16-SOIC	SCB Function			TCPWM	Fault Indicator	Protection Capability		USB Charging Signal				IEC4
Pin	Pin#	Pin#	UART	SPI	I2C			VBUS Short	OVT	AFC	QC	BC1.2	Apple	
P0.0	7	6	UART_0_CTS	SPI_1_MOSI	I2C_0_SDA	TCPWM_line_0:0	–	–	Yes	–	–	–	–	–
P0.1	8	7	UART_0_RTS	SPI_1_MISO	I2C_0_SCL	TCPWM_line_1:0	–	–	Yes	–	–	–	–	–
P1.0	1		UART_1_CTS	SPI_0_SEL	I2C_1_SDA:1	TCPWM_line_2:1	Yes	–	–	–	–	–	–	–
P1.1	2		UART_1_RTS	SPI_0_MISO	I2C_1_SCL:1	TCPWM_line_3:1	Yes	–	–	–	–	–	–	–
P1.2	5		UART_1_TX1	SPI_0_MOSI	–	–	–	–	–	D+	D+	D+	D+	–
P1.3	6		UART_1_RX1	SPI_0_CLK	–	–	–	–	–	D-	D-	D-	D-	–
P2.0	9	8	UART_0_TX0	SPI_1_SEL	–	TCPWM_line_2:0	–	–	–	–	–	–	–	–
P2.1	10		UART_0_RX0	SPI_1_CLK	–	TCPWM_line_3:0	–	–	–	–	–	–	–	–
P2.2	12		UART_0_TX1	–	I2C_1_SDA:0	TCPWM_line_0:1	–	Yes	–	–	–	–	–	Yes
P2.3	13		UART_0_RX1	–	I2C_1_SCL:0	TCPWM_line_1:1	–	Yes	–	–	–	–	–	Yes
P3.0	17	13	UART_1_TX0	–	–	–	–	–	–	D+	D+	D+	D+	Yes
P3.1	16	12	UART_1_RX0	–	–	–	–	–	–	D-	D-	D-	D-	Yes

Figure 2. Pinout of 24-QFN Package (Top View)

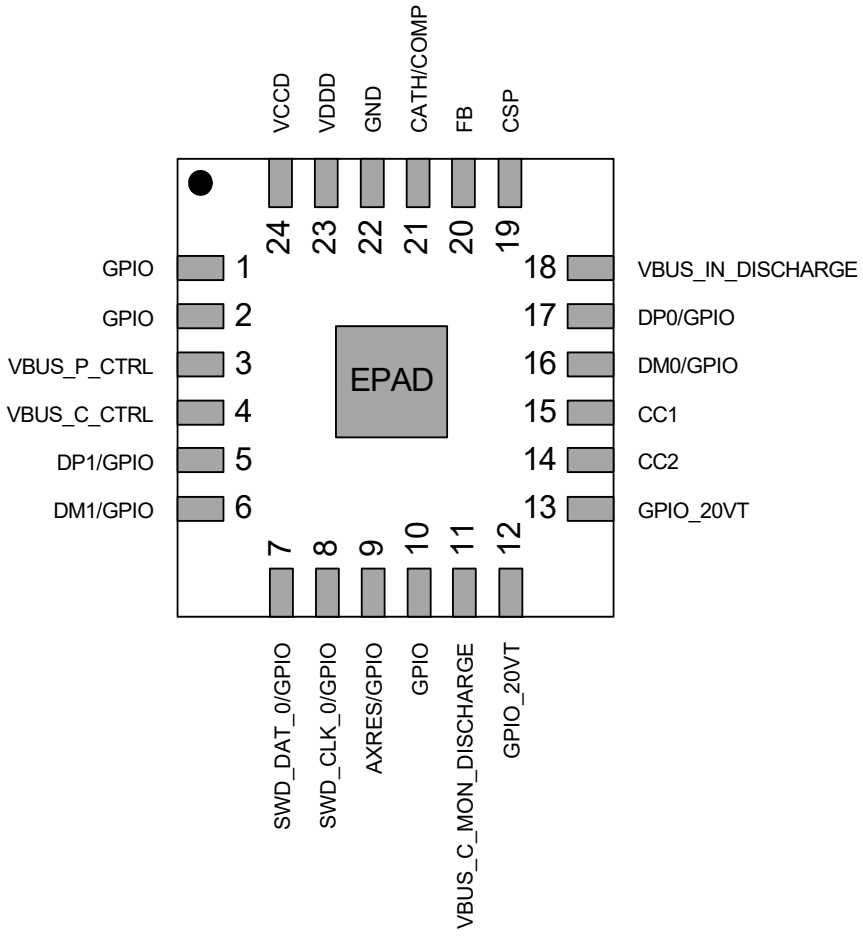
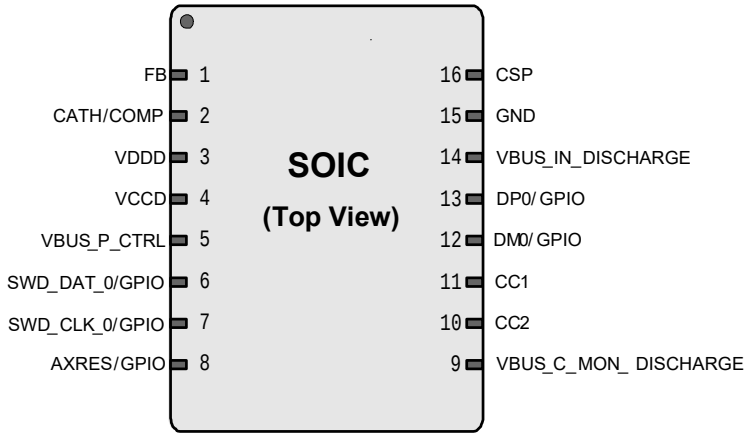


Figure 3. Pinout of 16-SOIC Package (Top View)



CCG3PA Programming and Bootloading

There are two ways to program application firmware into a CCG3PA device:

1. Programming the device flash over SWD Interface

2. Application firmware update over CC interface

Generally, the CCG3PA devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG3PA device's application firmware can be updated via the CC bootloader interface.

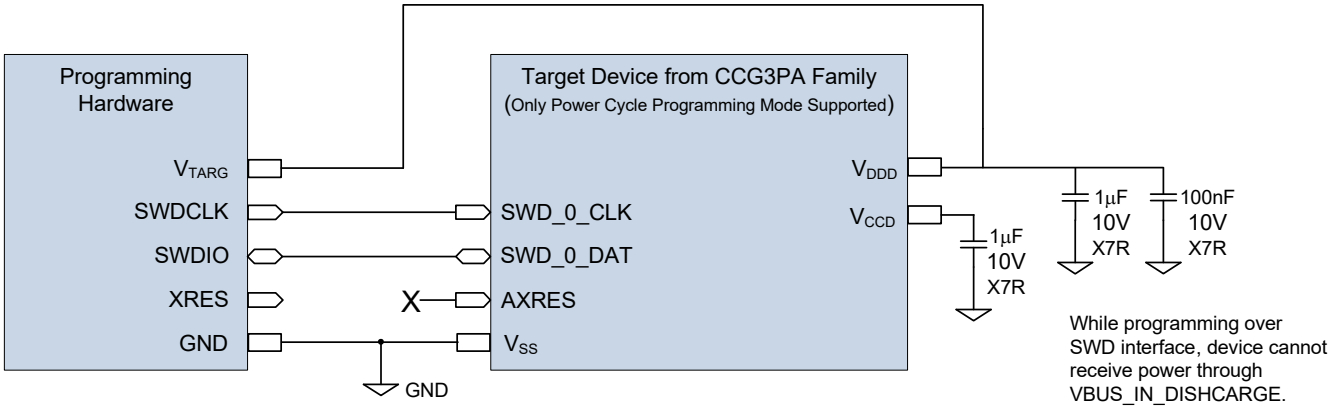
Programming the Device Flash over SWD Interface

CCG3PA family of devices can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3 and PSoC Programmer Software which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 4, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the CCG3PA device has to be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pin of CCG3PA device. While programming over SWD interface, the CCG3PA device cannot receive power through VBUS_IN_DISCHARGE.

The CCG3PA device family does not have the XRES pin. Due to that, the XRES line from the host programmer remains unconnected, and hence programming using Reset Mode is not supported. In other words, CCG3PA devices are supported by Power Cycle programming mode only since XRES line is not used. Contact Cypress for further details on CYPD3XXX Programming Specifications.

Figure 4. Connecting the Programmer to CYPD317x Device



Application Firmware Update over CC Interface

For bootloading CCG3PA applications, the CY4532 CCG3PA EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4532 CCG3PA EVK's Power Board is connected to the system containing CCG3PA device on one end and a Windows PC running the EZ-PD™ Configuration Utility as shown in Figure 5 on the other end to bootload the CCG3PA device.

Figure 5. Application Firmware Update over CC Interface

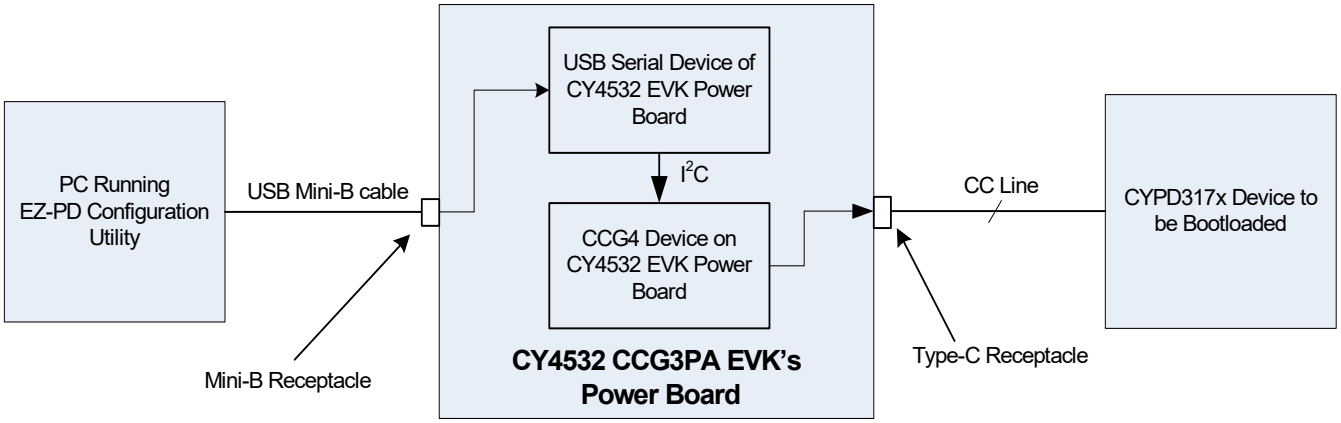
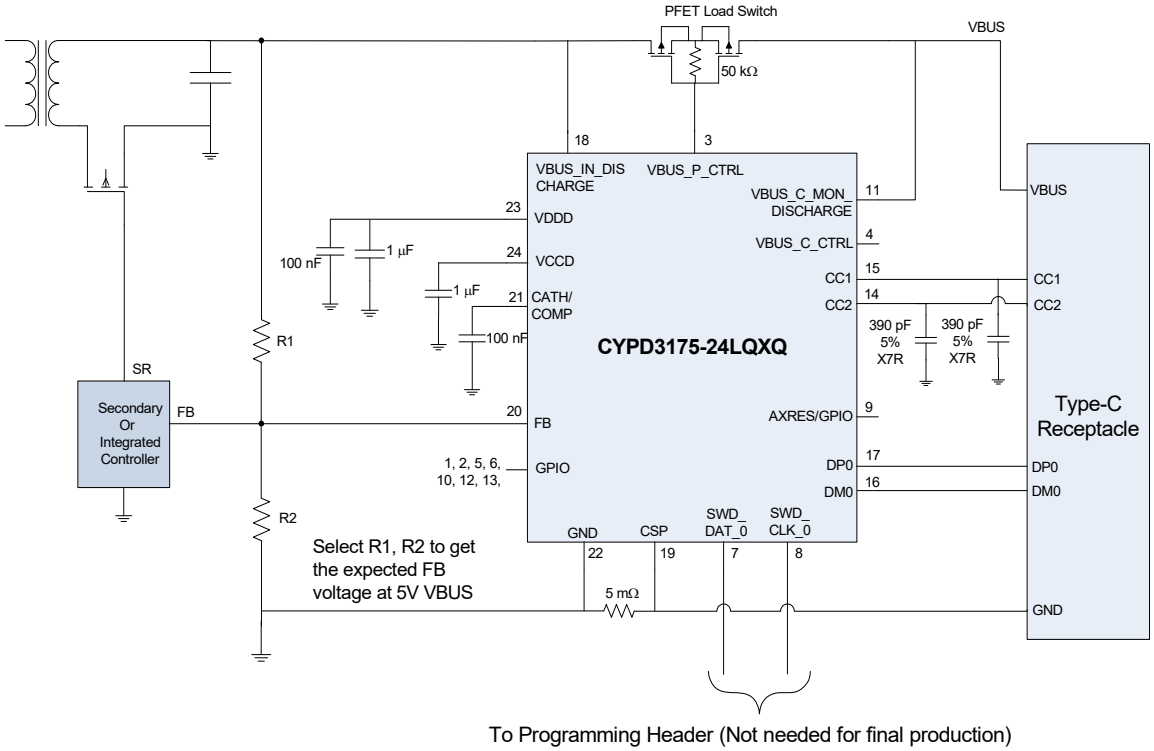


Figure 8 shows the application diagram of CCG3PA based power adapter with Direct Feedback control. In this application, VBUS is maintained at a constant voltage. The default value of VBUS upon power up (which is usually at 5 V) is set up by choosing the appropriate resistor divider that will set the FB node at a voltage expected by the secondary controller.

Feedback node is regulated using internal IDACs. Whenever a change in VBUS voltage is needed, CCG3PA will either source or sink a proportional current at feedback node, based on the amount of voltage change needed.

Figure 8. CCG3PA Based Power Adapter Application Diagram with Direct Feedback Control



I/O

Table 7. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	–
SID.GIO#41	$V_{IH\_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA at 3-V V_{DDD}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDD}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDD}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDD}
SID.GIO#17	C_{PIN_A}	Max pin capacitance	–	–	22	pF	Capacitance on DP0, DM0, DP1, DMI pins. Guaranteed by characterization.
SID.GIO#17A	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all other I/O_S. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL V_{DDD} > 2.7 V	15	40	–	mV	Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DDD} < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by design.
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 8. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 11. PWM AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 12. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	1.4	–	µA	–

Table 13. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	20	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 15. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 16. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 17. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 18. Fixed SPI Master Mode AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 19. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 20. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 21. Precise Power On Reset (POR)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 22. SWD Interface Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3V ≤ VDDD ≤ 5.5V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	2.7V ≤ VDDD ≤ 3.3V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	

Internal Main Oscillator

Table 23. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 24. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization.
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization.
SID.CLK#1	F_{IMO}	IMO frequency	24	36	48	MHz	Only 3 frequencies supported: 24 MHz, 36 MHz, and 48 MHz.

Internal Low-Speed Oscillator Power Down

Table 25. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 26. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by Characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by Characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 27. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194.4	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356.4	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0V and 1.32 V applied at CC1 or CC2
SID.PD.6	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter.

Table 28. LS-CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.LSCSA.1	Cin_inp	CSP Input capacitance	7	–	10	pF	Guaranteed by characterization
SID.LSCSA.2	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active Mode
SID.LSCSA.3	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10	%	
SID.LSCSA.4	Csa_Acc3	CSA accuracy 15 mV < Vsense < 20 mV	–6	–	6	%	
SID.LSCSA.5	Csa_Acc4	CSA accuracy 20 mV < Vsense < 30 mV	–5	–	5	%	
SID.LSCSA.6	Csa_Acc5	CSA accuracy 30 mV < Vsense < 50 mV	–4	–	4	%	
SID.LSCSA.7	Csa_Acc6	CSA accuracy 50 mV < Vsense	–4	–	4	%	
SID.LSCSA.8	Csa_SCP_Acc1	CSA SCP 80 mV	–16.5	–	30	%	
SID.LSCSA.9	Csa_SCP_Acc2	CSA SCP 100 mV	–13.4	–	24	%	
SID.LSCSA.10	Csa_SCP_Acc3	CSA SCP 150 mV	–9.4	–	16	%	
SID.LSCSA.11	Csa_SCP_Acc4	CSA SCP 200 mV	–7.5	–	12	%	
SID.LSCSA.12	Av	Nominal Gain values supported: 5, 10, 20, 35, 50, 75, 125, 150	5	–	150	V/V	
SID.LSCSA.24	Av1_E_Trim	Gain Error	–3	–	3	%	Guaranteed by characterization
SID.LSCSA.31	Av_E_SCP	Gain Error of SCP stage	–3.5	–	3.5	%	Guaranteed by characterization

Table 29. LS-CSA AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.LSCSA.AC.1	T_{OCP_GPIO}	Delay from OCP threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.2	T_{OCP_Gate}	Delay from OCP threshold trip to external PFET Power Gate Turn off	–	–	50	µs	–
SID.LSCSA.AC.3	T_{SCP_GPIO}	Delay from SCP threshold trip to output GPIO toggle	–	–	15	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.4	T_{SCP_Gate}	Delay from SCP threshold trip to external PFET Power Gate Turn off	–	–	50	µs	–
SID.LSCSA.AC.5	T_{SR_GPIO}	Delay from SR threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

Table 30. UV/OV Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	V_{THOV1}	Overvoltage Threshold Accuracy, 4.0 V to 11.0 V	–3	–	3	%	Active Mode
SID.UVOV.2	V_{THOV2}	Overvoltage Threshold Accuracy, 11 V to 27.4 V	–3.2	–	3.2	%	
SID.UVOV.3	V_{THUV1}	Undervoltage Threshold Accuracy, 2.7 V to 3.3 V	-4	–	4	%	
SID.UVOV.4	V_{THUV2}	Undervoltage Threshold Accuracy, 3.3 V to 4.0 V	–3.5	–	3.5	%	
SID.UVOV.5	V_{THUV3}	Undervoltage Threshold Accuracy, 4.0 V to 11.0 V	–3	–	3	%	
SID.UVOV.6	V_{THUV4}	Undervoltage Threshold Accuracy, 11.0 V to 22.0 V	–2.9	–	2.9	%	

Table 31. UV/OV AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.AC.1	T_{OV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.UVOV.AC.2	T_{OV_GATE}	Delay from UV threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.UVOV.AC.3	T_{UV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

Table 34. VBUS Discharge Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by Characterization.

Table 35. Voltage (VBUS) Regulation DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID.DC.VR.1	$V_{\_IN\_3}$	V(pad_in) at 3-V target	2.85	3	3.15	V	Active mode shunt regulator at 3 V with bandgap
SID.DC.VR.2	$V_{\_IN\_5}$	V(pad_in) at 5-V target	4.75	5	5.25	V	Active mode shunt regulator at 5 V
SID.DC.VR.3	$V_{\_IN\_9}$	V(pad_in) at 9-V target	8.55	9	9.45	V	Active mode shunt regulator at 9 V
SID.DC.VR.4	$V_{\_IN\_15}$	V(pad_in) at 15-V target	14.25	15	15.75	V	Active mode shunt regulator at 15 V
SID.DC.VR.5	$V_{\_IN\_20}$	V(pad_in) at 20-V target	19	20	21	V	Active mode shunt regulator at 20 V
SID.DC.VR.6	$V_{\_IN\_3\_DS}$	V(pad_in) at 3-V target	2.7	3	3.3	V	Deep Sleep mode shunt regulator at 3 V with bandgap
SID.DC.VR.7	$V_{\_IN\_5\_DS}$	V(pad_in) at 5-V target	4.5	5	5.5	V	Deep Sleep mode shunt regulator at 5 V
SID.DC.VR.8	$V_{\_IN\_9\_DS}$	V(pad_in) at 9-V target	8.1	9	9.1	V	Deep Sleep mode shunt regulator at 9 V
SID.DC.VR.9	$V_{\_IN\_15\_DS}$	V(pad_in) at 15-V target	13.5	15	16.5	V	Deep Sleep mode shunt regulator at 15 V
SID.DC.VR.10	$V_{\_IN\_20\_DS}$	V(pad_in) at 20-V target	18	20	22	V	Deep Sleep mode shunt regulator at 20 V
SID.DC.VR.11	I_{KA_OFF}	Off-state cathode current	–	–	10	µA	-
SID.DC.VR.12	I_{KA_ON}	Current through cathode pin	–	–	10	mA	-

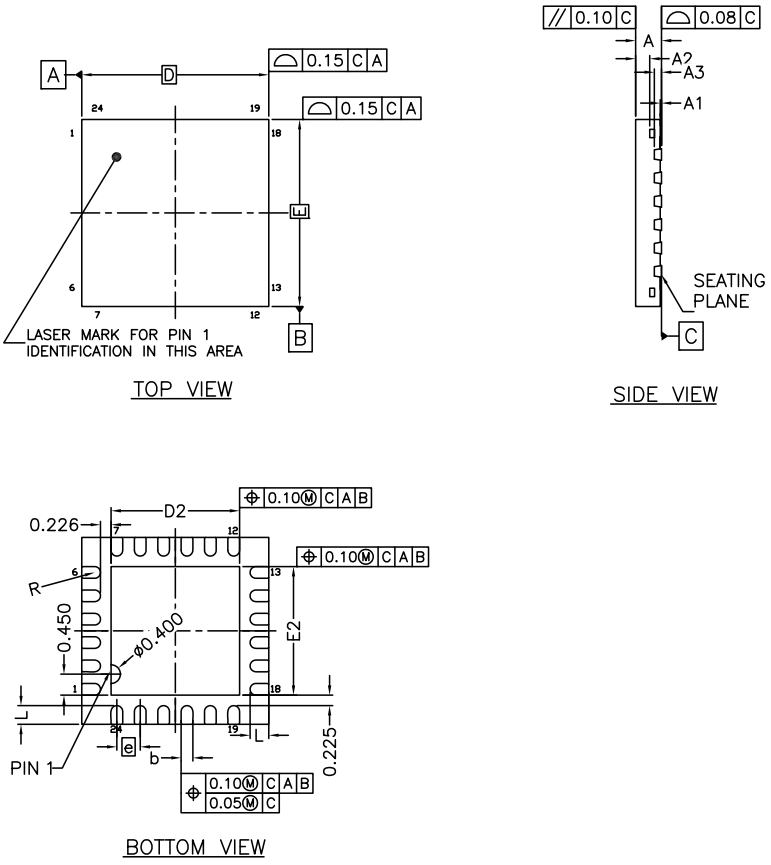
Table 36. VBUS Short Protection Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VSP.1	V_SHORT_TRIGGER	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by Characterization.

Table 37. VBUS DC Regulator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VREG.2	VBUS_-DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

Figure 11. 24-pin QFN Package Outline



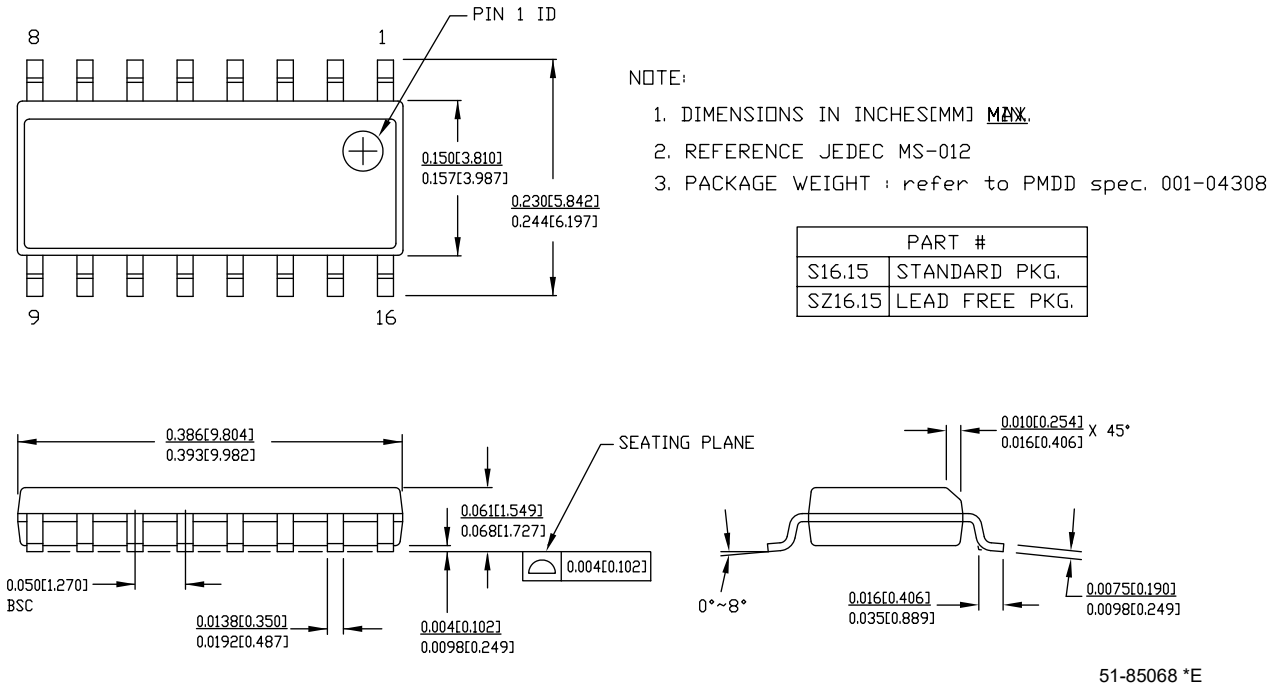
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A_1	0.00	—	0.05
A_2	—	0.40	0.425
A_3	0.152 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D_2	2.65	2.75	2.85
E	4.00 BSC		
E_2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.

002-16934 *A

Figure 12. 16-pin SOIC Package Outline



Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier

Table 46. Acronyms Used in this Document *(continued)*

Acronym	Description
OCP	overcurrent protection
OTP	over temperature protection
OVP	overvoltage protection
OVT	overvoltage tolerant
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SCP	short circuit protection
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
UVP	undervoltage protection
XRES	external reset I/O pin

Document History Page

Document Title: EZ-PD™ CCG3PA Datasheet, USB Type-C Port Controller Document Number: 002-16951				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5473667	VGT	10/13/2016	New datasheet
*A	5544333	VGT	12/13/2016	Changed datasheet status to Preliminary. Updated Features. Updated Logic Block Diagram. Updated Functional Overview Updated Figure 2, Figure 3, Figure 6, Figure 8, Figure 9, and Figure 10. Updated Pinouts. Updated Table 4 with VCC_PIN_ABS and VSBU_PIN_ABS parameters. Added Q-temp parts in Table 42.
*B	5583660	VGT	01/18/2017	Updated General Description, Features, I/O Subsystem, CPU, Charger Detection, and Ordering Information. Updated Table 2 and Table 4. Updated Figure 6 through Figure 10. Updated Sales page.
*C	5665676	VGT	03/22/2017	Updated Figure 2, Figure 6, Figure 8, Figure 10, Table 1,Table 2, Table 4, Table 42, Features, Logic Block Diagram, Functional Overview, Power Systems Overview, Ordering Code Definitions, Acronyms. Added Internal Block Diagram. Added Table 5 through Table 41 in Device-Level Specifications. Updated compliance with USB spec in Sales, Solutions, and Legal Information. Updated Cypress logo.
*D	5738854	VGT	05/19/2017	Added Application Diagram description before Figure 6, Figure 8, Figure 9, and Figure 10. Added Figure 1. Added CCG3PA Programming and Bootloading section. Added Document History Page section. Added Table 3. Updated Figure 3, Figure 4, Figure 6, Figure 8, Figure 9, and Figure 10. Updated Table 2, Table 4, Table 5, and Table 42. Updated Figure 11 (spec 002-16934 Rev. ** to *A) in Packaging. Updated Cypress logo, Sales page, and Copyright information.
*E	5984670	VGT	12/06/2017	Removed Preliminary document status. Updated System-Level Fault Protection, Power, and System-Level ESD Protection. Updated Internal Block Diagram Updated Figure 2. Table 2: Updated Pins 12 and 13. Added Note 5. Updated Figure 6. Added Figure 7. Table 4: Updated max value for $V_{CC\_PIN\_ABS}$ Table 5: Removed SID_DS and updated typ value for SID_PB_DS_UA. Table 7: Added new SID.GIO#17 spec and changed SID.GIO#17 to SID.GIO#17A. Added Table 9 and Table 10. Table 12: Updated max value for SID149. Table 22; Added “Guaranteed by Characterization” Table 24: Updated Conditions for SID226 and SID228. Updated typ value and conditions for SID.CLK#1. Table 26: Updated Conditions for SID234 and SID238. Table 28: Updated min, typ, and max values for SID.LSCSA.1,SID.LSCSA.7, and SID.LSCSA.24 Updated Conditions for SID.GIO#17A, SID.GIO#43, SID.GIO#44, SID.GIO#45, and SID69. Table 31: Added “Guaranteed by Characterization” Table 32: Added SID.GD.9, SID.GD.10, SID.GD.11, SID.GD.12, SID.GD.13, SID.GD.14. Changed description of spec IDs SID.GD.1 to SID.GD.8. Table 33: Renumbered all spec IDs starting from SID.GD.15 to SID.GD.20. Modified max values of SID.GD.15, SID.GD.17 and SID.GD.18. Modified Details/Conditions of all parameters. Table 34: Removed spec IDs SID.VBUS.DISC.1 to SID.VBUS.DISC5. Renumbered SID.VBUS.DISC6 to SID.VBUS.DISC11. Added new spec IDs SID.VBUS.DISC6 to SID.VBUS.DISC10.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support