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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0208hec1925

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Document Disclaimer

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PIN DESCRIPTION

Pin diagrams and identification for the device are displayed in Figure 3 through Figure 6, and in Table 2 through Table 5.

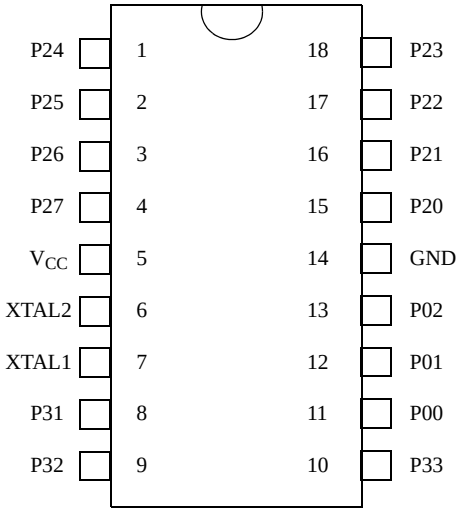

Figure 3. 18-Pin DIP/SOIC Configuration, STANDARD Mode

Table 2. 18-Pin DIP/SOIC Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4-7	Input/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1 AN1	Input
9	P32	Port 3, Pin 1 AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0-2	Input/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0-3	Input/Output

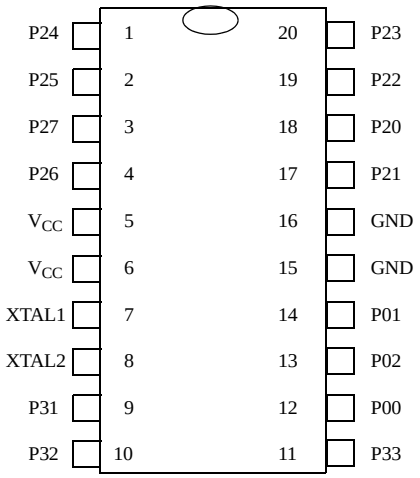

Figure 5. 20-Pin SSOP Pin Configuration, STANDARD Mode

Table 4. 20-Pin SSOP Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1,2	P24-P25	Port 2, Pins 4-5	Input/Output
3	P27	Port 2, Pin 7	Input/Output
4	P26	Port 2, Pin 6	Input/Output
5	V_{CC}	Power Supply	
6	V_{CC}	Power Supply	
7	XTAL1	Crystal Oscillator Clock	Input
8	XTAL2	Crystal Oscillator Clock	Output
9	P31	Port 3, Pin 1, AN1	Input
10	P32	Port 3, Pin 2, AN2	Input
11	P33	Port 3, Pin 3, REF	Input
12	P00	Port 0, Pin 0	Input/Output
13	P02	Port 0, Pin 1	Input/Output
14	P01	Port 0, Pin 1	Input/Output
15	GND	Ground	
16	GND	Ground	
17	P21	Port 2, Pin 1	Input/Output
18	P20	Port 2, Pin 0	Input/Output
19-20	P22-P23	Port 2, Pins 2-3	Input/Output

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed on Table 6 may cause permanent damage to the device. This rating is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mΩ for the package. See Table 6. Power dissipation is calculated as follows:

Total Power Dissipation = V_{CC} X [I_{CC}–(sum of I_{OH})]
+sum of [(V_{CC}–V_{OH}) X I_{OH}]
+ sum of (V_{OL} X I_{OL})

Table 6. Absolute Maximum Ratings

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	-40	+105	C	
Storage Temperature	-65	+150	C	
Voltage on any Pin with Respect to V_{SS}	-0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V	
Voltage on XTAL1, P31, P32, P33 with respect to V_{SS}	-0.6	V_{DD}+1	V	3
Total Power Dissipation		462	mΩ	
Maximum Allowable Current out of V_{SS}		300	mA	
Maximum Allowable Current into V_{DD}		270	mA	
Maximum Allowable Current into an Input Pin	-600	+600	µA	4
Maximum Allowable Current into an Open-Drain Pin	-600	+600	µA	2
Maximum Allowable Output Current Linked by any I/O Pin		20	mA	
Maximum Allowable Output Current Sourced by any I/O Pin		20 mA		

1. Applies to all pins except where otherwise noted. Maximum current into or out of pin must be ±600 µA.
2. Device pin is not at an output Low state.
3. There is no input protection diode from pin to V_{DD}.
4. This excludes XTAL1 and XTAL2.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin See Figure 7.

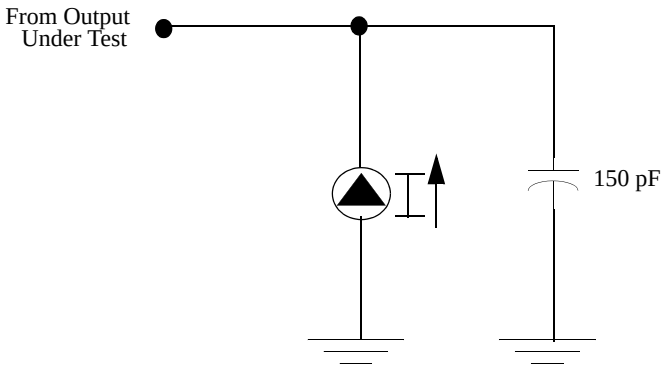

Figure 7. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = OV, f = 1.0 MHz, unmeasured pins returned to GND. See Table 7.

Table 7. Capacitance

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC Electrical Characteristics

Standard Temperature Range

Table 8 provides Direct Current characteristics for the Z86E02 SL1925 microcontroller, at a standard ambient temperature range of 0°C to 70°C.

Table 8. DC Characteristics, Standard Temperature Range

TA = 0°C to +70°C							
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1] Units**	**Conditions**	**Notes**
V_{INMAX}	Max Input Voltage	3.5V	-12	12	V	I_{IN} < 250 µA	2
		5.5V	-12	12	V	I_{IN} < 250 µA	2

AC Electrical Timing Characteristics

Figure 8 illustrates Alternating Current timing for the Z86E02 SL1925 microcontroller.

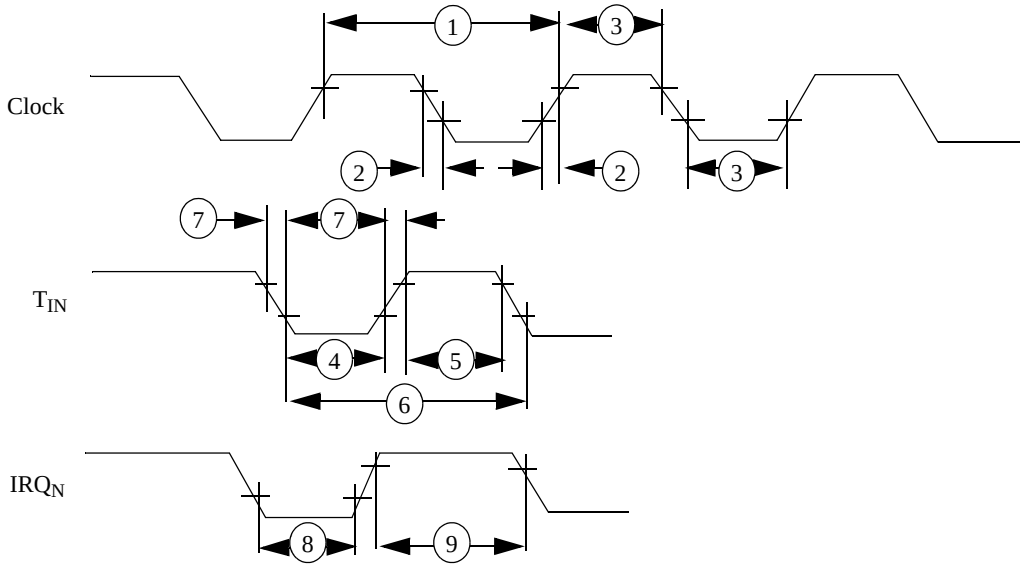

Figure 8. AC Electrical Timing

STANDARD Mode at Standard Temperature

Table 10 describes timing characteristics in STANDARD mode at standard temperature for the timing diagram noted in Figure 8.

Table 10. AC Electrical Characteristics, Standard Mode and Temperature

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	T_PC	Input Clock Period	3.5V	125	DC	ns	1
			5.5V	125	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25	ns	1
			5.5V		25	ns	1
3	T_WC	Input Clock Width	3.5V	62		ns	1
			5.5V	62		ns	1

Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	100		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	100		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	3.5V	4	36	ms	
			5.5V	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Standard Temperature

Table 12 describes timing characteristics in LOW EMI mode at standard temperature for the timing diagram noted in Figure 8.

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = 0°C to +70°C						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	3.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	3TpC		3TpC			1,2
			5.5V	3TpC		3TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		10		ms	
			5.5V	5		5		ms	

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option prevents accidental entry into EPROM Mode or Test Mode.

STANDARD Mode

XTAL1, XTAL2. Crystal In, Crystal Out (time-based input and output, respectively). These pins connect an external parallel-resonant crystal, resonator, RC, LC, or an external single-phase clock (8 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 9).

Auto Latch. The Auto Latch places valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch sets the ports to an undetermined state of 0 or 1. The default condition is AUTO LATCH ENABLED. The Auto Latch can be disabled by programming the AUTO LATCH DISABLE option bit.

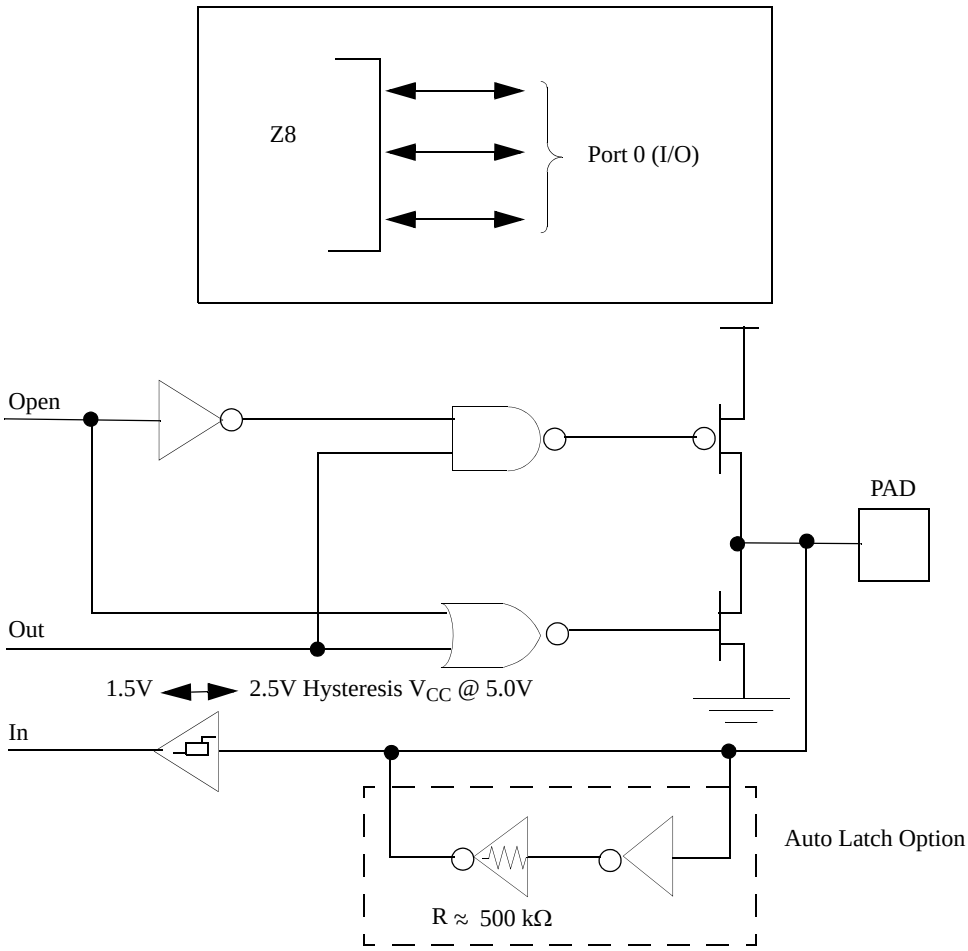

Figure 9. Port 0 Configuration

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 10).

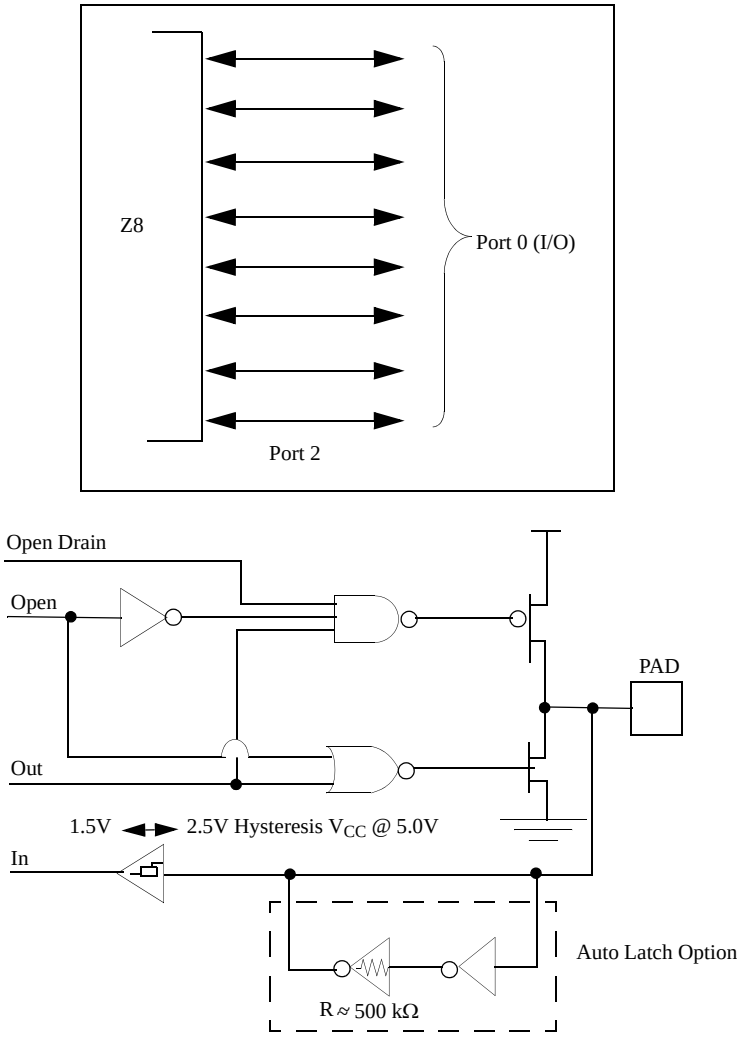

Figure 10. Port 2 Configuration

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 11).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8® interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

Note: The rising edge interrupt is not supported. on the CCP emulator (a hardware/software work around must be employed).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX      Push RP
                LD RP, #0Fh
                LD R0, #0FFh
                POP RP
```

Op Code WDT (5Fh)

The first time Op Code 5Fh is executed, the WDT is enabled; subsequent execution clears the WDT counter. This clearing of the counter must be performed at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 crystal clock cycles. The software enabled WDT does not run in STOP mode.

On the CCP emulator, a software workaround must be used to emulate the software WDT. This workaround follows.

```
SWFIXSWDT:    PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Op Code WDH (4Fh)

When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters – it just makes it possible to operate the WDT during HALT mode. A WDH instruction executed without executing WDT (5Fh) yields no effect.

Note: On the CCP emulator, a software workaround must be used to enable the software in HALT Mode/STOP Mode or hardware-enabled WDT. This workaround follows.

Software Work Around on the Z86CCP01ZEM Emulator to Emulate the Software WDT Running in HALT Mode

```
SWFIXSWDT:    PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Permanent WDT

Selecting the hardware-enabled Permanent WDT option bit automatically enables the WDT upon exiting reset. The permanent WDT always runs in HALT mode and STOP mode, and it cannot be disabled.

Software Work Around on the Z86CCP01ZEM Emulator to Emulate the Hardware Enabled Permanent WDT in HALT Mode and Stop Mode

The following functions must be performed

1. The first instruction after reset at address 000Ch must be the WDT instruction or op code 5F. The following routine must be added in the initialization of the

```
HSWFIXHWDT:   PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Auto Reset Voltage (V_{LV})

The Z8® features an auto-reset built-in. The auto-reset circuit resets the Z8® when it detects the V_{CC} below V_{LV}. Figure 19 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the V_{CC} operating voltage range, the Z8® functions down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

Table 21. Port 3 Mode Register, R247 P3M F7h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-2	Reserved	W	X	Reserved-must be 0
1	Port 3	W	0	**Port 3 Outputs** 0: DIGITAL Mode 1: ANALOG Mode
0	Port 2	W	0	**Port 2 Outputs** 0: Open-Drain 1: Push-Pull

Table 22. Port 0 and 1 Mode Register, R248 P01 F8h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	X	1	0	1
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-5, 3	Reserved	W	X	Reserved-must be 0
4	Reserved	W	0	Reserved-must be 0
2	Reserved	W	X	Reserved-must be 1
1-0	P02-P00	W	01	**P02-P00 Mode** 0: Output 1: Input

Table 25. Interrupt Mask Register, R251 IMR FBh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7	Master Interrupt Enable	R/W	0	0: Disables global interrupts* 1: Enables global interrupts*
6	Reserved	R/W	X	Reserved-must be 0
5-0	IRQ0-IRQ5	R/W	X	1: Enables IRQ0-IRQ5 (D0 = IRQ0)
Note: *Must use Ei/Di instruction to set/reset this bit.				

Table 26. Flag Register, R252 FCh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	X	X	X	X	X	X	X
Note: R = Read, X= Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7	Carry	R/W	X	Carry Flag
6	Zero	R/W	X	Zero Flag
5	Sign	R/W	X	Sign Flag
4	Overflow	R/W	X	Overflow Flag
3	Decimal Adjust	R/W	X	Decimal Adjust Flag
2	Half Carry	R/W	X	Half Carry Flag
1	User	R/W	X	User Flag F2*
0	User	R/W	X	User Flag F1*
Note: *Not affected by RESET.				

Table 29. Stack Pointer Low, R255 SPL FFh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W= Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	Stack	R/W	0	Stack Pointer Lower Byte (SP0-SP7)