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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0208hec1925tr

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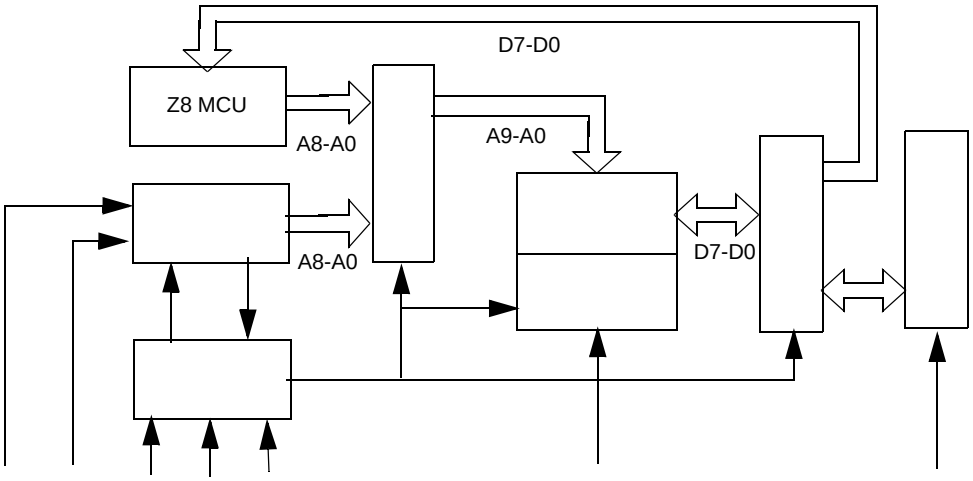

Figure 2. EPROM Programming Mode Block Diagram

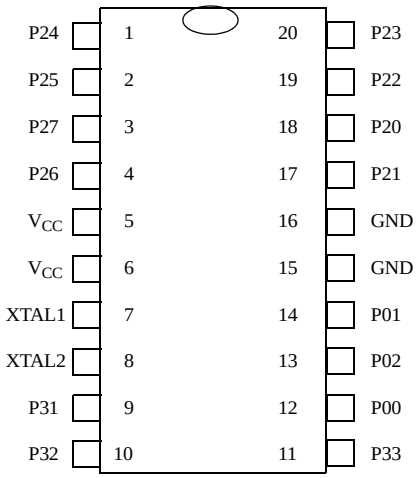

Figure 5. 20-Pin SSOP Pin Configuration, STANDARD Mode

Table 4. 20-Pin SSOP Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1,2	P24-P25	Port 2, Pins 4-5	Input/Output
3	P27	Port 2, Pin 7	Input/Output
4	P26	Port 2, Pin 6	Input/Output
5	V_{CC}	Power Supply	
6	V_{CC}	Power Supply	
7	XTAL1	Crystal Oscillator Clock	Input
8	XTAL2	Crystal Oscillator Clock	Output
9	P31	Port 3, Pin 1, AN1	Input
10	P32	Port 3, Pin 2, AN2	Input
11	P33	Port 3, Pin 3, REF	Input
12	P00	Port 0, Pin 0	Input/Output
13	P02	Port 0, Pin 1	Input/Output
14	P01	Port 0, Pin 1	Input/Output
15	GND	Ground	
16	GND	Ground	
17	P21	Port 2, Pin 1	Input/Output
18	P20	Port 2, Pin 0	Input/Output
19-20	P22-P23	Port 2, Pins 2-3	Input/Output

Table 8. DC Characteristics, Standard Temperature Range (Continued)

TA = 0°C to +70°C								
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	3.5V	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}-0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}-0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}-0.3	0.2 V_{CC}	0.8	V		
		5.5V	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}-0.4		3.3	V	I_{OH} = -2.0 mA	3
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	3
		3.5V	V_{CC}-0.4		3.3	V	I_{OH} = -0.5 mA	10
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	10
V_{OL1}	Output Low Voltage	3.5V		0.8	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		3.5V		0.4	0.2	V	I_{OL}=1.0mA	10
		5.5V		0.4	0.1	V	I_{OL}=1.0mA	10
V_{OL2}	Output Low Voltage	3.5V		1.2	1.0	V	I_{OL} = +12 mA	3
		5.5V		1.2	0.8	V	I_{OL} = +12 mA	3
V_{LV}	V_{CC} Low Voltage Auto Reset		2.6	3.2	2.9	V	@ 4MHz Maximum Internal Clock Frequency	4
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			TA = -40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	4.5V		7.0	6.8	mA	@ 2 MHz	3,6
		5.5V		7.0	6.8	mA	@ 2 MHz	3,6
		4.5V		11.0	8.2	mA	@ 8 MHz	3,6
		5.5V		11.0	8.2	mA	@ 8 MHz	3,6
I_{CC1}	Standby Current (HALT Mode)	4.5V		3.0	2.5	mA	@ 2 MHz	3,6
		5.5V		3.0	2.5	mA	@ 2 MHz	3,6
		4.5V		5.0	3.0	mA	@ 8 MHz	3,6
		5.5V		5.0	3.0	mA	@ 8 MHz	3,6
I_{CC}	Supply Current (Low EMI Mode)	4.5V		7.0	6.8	mA	@ 1 MHz	6,10
		5.5V		7.0	6.8	mA	@ 1 MHz	6,10
		4.5V		9.0	7.5	mA	@ 2 MHz	6,10
		5.5V		9.0	7.5	mA	@ 2 MHz	6,10
		4.5V		11.0	8.2	mA	@ 4 MHz	6,10
		5.5V		11.0	8.2	mA	@ 4 MHz	6,10
I_{CC1}	Standby Current (HALT and Low EMI Mode)	4.5V		1.6	0.9	mA	@ 1 MHz	6,10
		5.5V		1.6	0.9	mA	@ 1 MHz	6,10
		4.5V		1.9	1.0	mA	@ 2 MHz	6,10
		5,5V		1.9	1.0	mA	@ 2 MHz	6,10
		4.5V		2.4	3.0	mA	@ 4 MHz	6,10
		5.5V		2.4	3.0	mA	@ 4 MHz	6,10
I_{CC2}	Standby Current (Stop mode)	4.5V		20	1.0	µA	WDT is not Running	6,7,8
		5.5V		20	1.0	µA	WDT is not Running	6,7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	9

AC Electrical Timing Characteristics

Figure 8 illustrates Alternating Current timing for the Z86E02 SL1925 microcontroller.

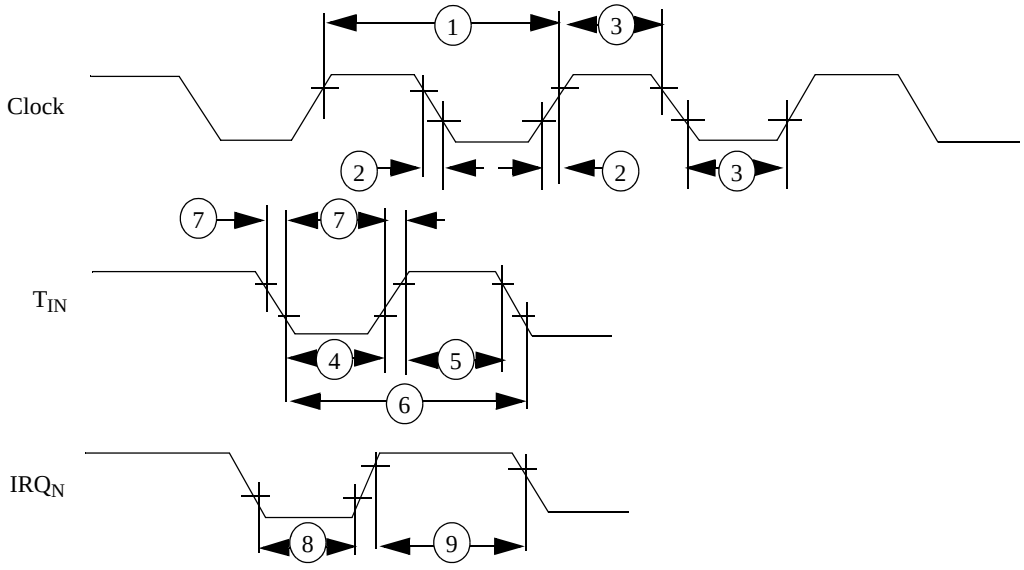

Figure 8. AC Electrical Timing

STANDARD Mode at Standard Temperature

Table 10 describes timing characteristics in STANDARD mode at standard temperature for the timing diagram noted in Figure 8.

Table 10. AC Electrical Characteristics, Standard Mode and Temperature

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	T_PC	Input Clock Period	3.5V	125	DC	ns	1
			5.5V	125	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25	ns	1
			5.5V		25	ns	1
3	T_WC	Input Clock Width	3.5V	62		ns	1
			5.5V	62		ns	1

STANDARD Mode at Extended Temperature

Table 11 describes timing characteristics in STANDARD mode at extended temperature for the timing diagram noted in Figure 8.

Table 11. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = -40°C to +105°C				
				8MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	125	DC	ns	1
			5.5V	125	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25	ns	1
			5.5V		25	ns	1
3	T_WC	Input Clock Width	4.5V		62	ns	1
			5.5V		62	ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	4.5V	70		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	4.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	4.5V	5		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	4.5V	1	20	ms	
			5.5V	1	20	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature (Continued)

				TA = 0°C to +70°					
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	T_{POR}	Power-On Reset Time	3.5V	2	18	2	18	ms	
			5.5V	2	18	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Extended Temperature

Table 13 describes timing characteristics in LOW EMI mode at extended temperature for the timing diagram noted in Figure 8.

Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature

				TA = 0°C to +70°C					
				1MHz		4MHz			
No	Symbol	Parameter	Vcc	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1

Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature (Continued)

			TA = 0°C to +70°C						
				1MHz		4MHz			
No	Symbol	Parameter	Vcc	Min	Max	Min	Max	Units	Notes
8	T_WIL	Interrupt Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input	4.5V	3TpC		3TpC			1,2
			5.5V	3TpC		3TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time for Time-out	4.5V	5		5		ms	
			5.5V	5		5		ms	
11	T_{POR}	Power-On Reset Time	4.5V	1	20	1	20	ms	
			5.5V	1	20	1	20	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

Low-EMI Mode

The device can be programmed to operate in a LOW EMI EMISSION mode by means of a OTP bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 200 ohms
- Oscillator divide-by-two circuitry eliminated

The LOW EMI mode is a OTP programmable option to be selected by the customer at the time of Device Programming.

Software Work Around on the Z86CCP01ZEM Emulator to Emulate Low EMI Mode

```
SWFIXLEMI:      PUSH RP
                LD RP, #0Fh
                LD R12, #00110110B
                LD R0,#11010111B
                POP RP
```

Pin Functions

EPROM Mode

D7–D0 Data Bus. Data can be read from, or written to, the EPROM through this data bus.

V_{CC} Power Supply. It is typically 5V during all EPROM Read Mode and typically 6.4V during other modes (PROGRAM, PROGRAM VERIFY, etc.).

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM READ mode, PROGRAM mode, and PROGRAM VERIFY mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the data bus is output. When High, the data bus is input.This pin must toggle for each data output read.

EPM EPROM Program Mode. This pin controls the selection of EPROM operation modes by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear (active High). This pin resets the internal address counter at the High level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one count with one clock cycle.

$\overline{PGM}$ Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the data bus.

Pin Function Changes in EPROM Mode

With the exception of V_{CC} and GND, the Z8® changes all of its pin functions in EPROM mode. X_{OUT} offers no function; X_{IN} functions as $\overline{CE}$, P31 functions as $\overline{OE}$, P32 functions as EPM, P33 functions as V_{PP} P00 functions as CLEAR, P01 functions as CLOCK, and P02 functions as $\overline{PGM}$. Please refer to Program Memory for additional EPROM mode descriptions.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if excessive noise surges above V_{CC} occur on the XTAL1 pin ($\overline{OE}$).

In addition, processor operation of Z8® OTP devices maybe affected by excessive noise surges on the P33 (V_{PP}), XTAL1 ($\overline{CE}$), P32 (EPM), P31 ($\overline{OE}$) pins while the microcontroller is in Standard Mode.

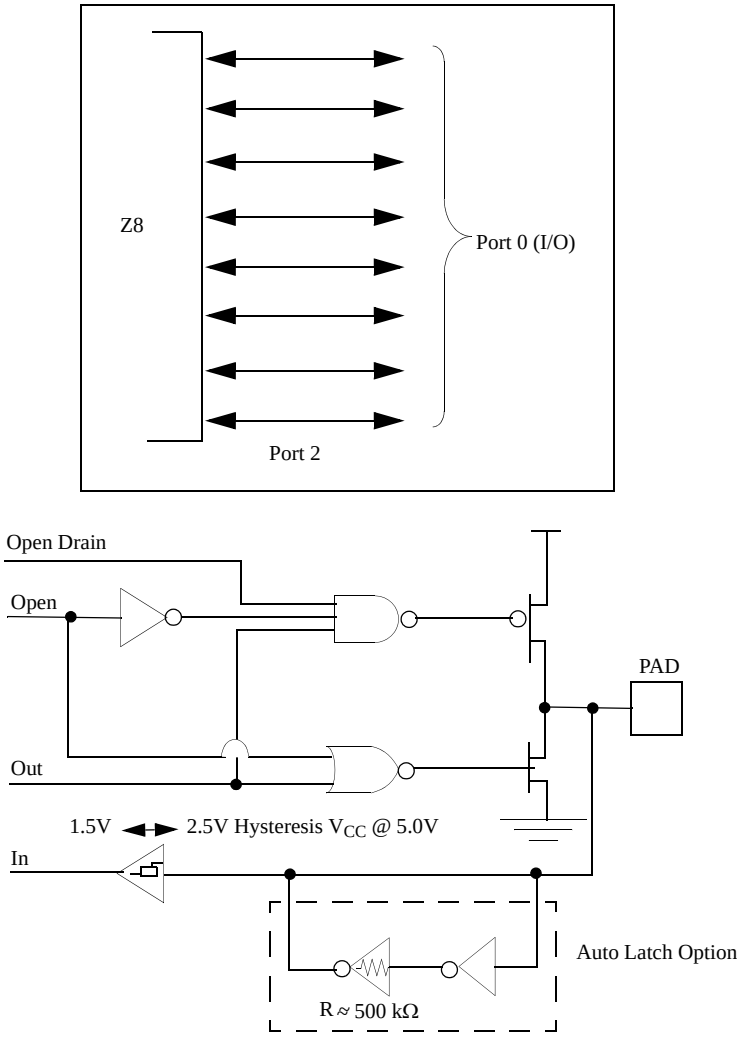

Figure 10. Port 2 Configuration

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 11).

Functional Description

The following special functions are incorporated into the Z8® devices to enhance the standard Z8 core architecture and to provide the user with increased design flexibility.

RESET

A RESET can be triggered in the following two ways:

- Power-On Reset
- Watch-Dog Timer Reset

Power-On Reset (POR)

Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000Ch (Figure 12). The Z8® control registers' reset value is indicated in Table 14.

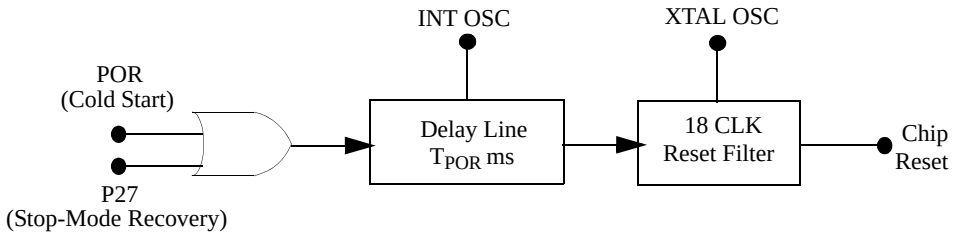

Figure 12. Internal Reset Configuration

Table 14. Z8® Control Registers Reset Values*

		Reset Condition								
Address	**Register**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**Dl**	**D0**	**Comments**
FFh	SPL	0	0	0	0	0	0	0	0	
FDh	RP	0	0	0	0	0	0	0	0	
FCh	FLAGS	U	U	U	U	U	U	U	U	
FBh	IMR	0	U	U	U	U	U	U	U	
FAh	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9h	IPR	U	U	U	U	U	U	U	U	
F8h*	P01M	U	U	U	0	U	1	0	1	
F7h*	P3M	U	U	U	0	U	U	0	0	
F6h*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F3h	PRE1	U	U	U	0	U	U	0	0	
F2h	T1	U	U	U	0	U	U	U	U	
F1h	TMR	0	0	0	0	0	0	0	0	

Note: Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset causes these control registers to be reconfigured as indicated in Table 14 and the user must avoid bus contention on the port pins or it may affect device reliability

A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out (in Halt mode)

Watch-Dog Timer Reset

The WDT is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Clock

The Z8® on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to an external crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, up to 8 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitor values from each pin directly to device ground pin 14 on DIP and SOIC packages or pins 5 and 6 on SSOP package (Figure 18).

Note: The crystal capacitor loads should be connected directly to the Z8® GND pin to reduce Ground noise injection. They should not connect to system Ground.

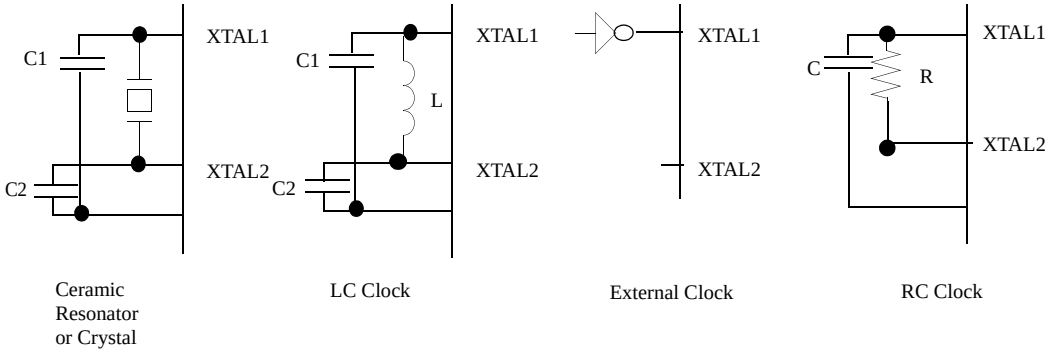

Figure 18. Oscillator Configuration

Table 16. Typical Frequency (MHz) vs. RC Values V_{CC} = 5.0 V @ 25°C

	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
Resistor (R)	A	B	A	B	A	B	A	B
1.0 MΩ	0.05	0.03	0.03	0.02	0.02	0.01	0.001	0.001
560 KΩ	0.09	0.04	0.05	0.025	0.03	0.02	0.003	0.002
220 KΩ	0.23	0.11	0.12	0.07	0.07	0.043	0.007	0.005
100 KΩ	0.5	0.19	0.28	0.13	0.15	0.086	0.014	0.01
56 KΩ	0.93	0.28	0.48	0.2	0.27	0.13	0.026	0.02
20 KΩ	2.2	0.57	1.1	0.41	0.71	0.28	0.07	0.05
10 KΩ	3.5	1.0	2.1	0.64	1.4	0.45	0.14	0.08

Control Registers

Table 17. Timer Mode Register, R241 TMR F1h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	R/W	00	Reserved-must be 0
5-4	T_{IN} Mode	R/W	0	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (non retriggerable) 11: Trigger Input (retriggerable)
3	T1 Count	R/W	0	**TI Count** 0: Disable 1: Enable
2	T1	R/W	0	**TI** 0: No Function 1: Load T1
1-0	Reserved	R/W	0	Reserved - must be 0

Table 18. Counter/Timer 1 Register, R242 T1 F2h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	T1	R	X	**T1 Current Value**
		W	X	**T1 Initial Value** Range = 1-256 decimal; 01h-00h

Table 19. Prescaler 1 Register, R243 PRE1 F3h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-2	Prescaler	W	X	**Prescaler Modulo** Range = 1-64 decimal; 01h-00h
1	Clock	W	0	**Clock Source** 0: T1 External Timing Input (T_{IN}) Mode 1: Internal
0	Count	W	0	**TI Count Mode** 0: Single Pass 1: Modulo N

Table 20. Port 2 Mode Register, R246 P2M F6h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1
Note: W = Write,								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	P20-P27	W	1	**P20-P27 I/O Definition** 0: Defines bit as Output 1: Defines bit as Input

Table 21. Port 3 Mode Register, R247 P3M F7h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-2	Reserved	W	X	Reserved-must be 0
1	Port 3	W	0	**Port 3 Outputs** 0: DIGITAL Mode 1: ANALOG Mode
0	Port 2	W	0	**Port 2 Outputs** 0: Open-Drain 1: Push-Pull

Table 22. Port 0 and 1 Mode Register, R248 P01 F8h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	X	1	0	1
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-5, 3	Reserved	W	X	Reserved-must be 0
4	Reserved	W	0	Reserved-must be 0
2	Reserved	W	X	Reserved-must be 1
1-0	P02-P00	W	01	**P02-P00 Mode** 0: Output 1: Input

Table 23. Interrupt Priority Register, R249 IPR F9h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X

Note: W = Write, X = Indeterminate

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	W	X	Reserved-must be 0
5	IRQ3, IRQ5	W	X	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3 1: IRQ3 < IRQ5
4, 3, 0	Interrupt	W	X	**Interrupt Group Priority** 000: Reserved* 001: C>A>B 010: A>B>C 011: A>C>B 100: B>C>A 101: C>B>A 110: B>A>C 111: Reserved
2	IRQ0, IRQ2	W	X	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0 1: IRQ0 < IRQ2
1	IRQ1, IRQ4	W	X	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4 1: IRQ4 < IRQ1

Note: *Selecting a Reserved mode causes an undefined operation.

Table 29. Stack Pointer Low, R255 SPL FFh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W= Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	Stack	R/W	0	Stack Pointer Lower Byte (SP0-SP7)