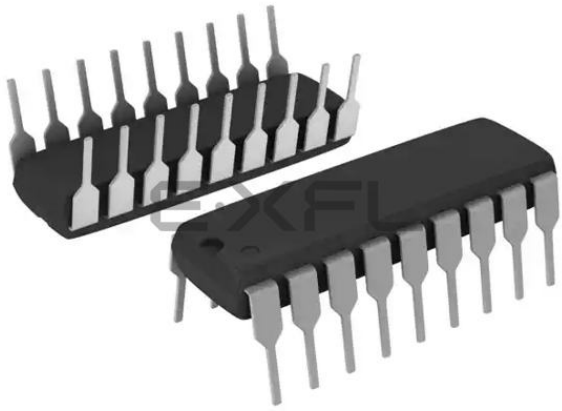

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 14 |
| Program Memory Size | 512B (512 x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 61 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 18-DIP (0.300", 7.62mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86e0208peg1925 |

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- Low-Power Consumption (50 mΩ typical)
- Fast Instruction Pointer (1.5µs @ 8 MHz)
- RAM Bytes (61)

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

## BLOCK DIAGRAMS

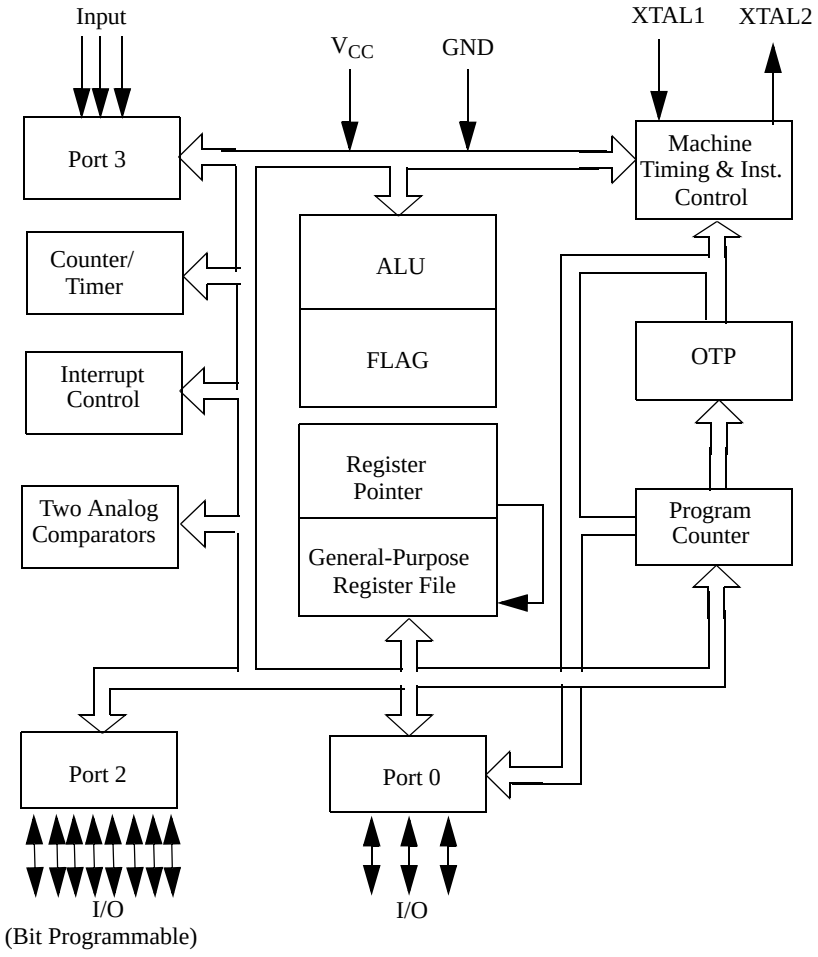


**Figure 1. Functional Block Diagram**

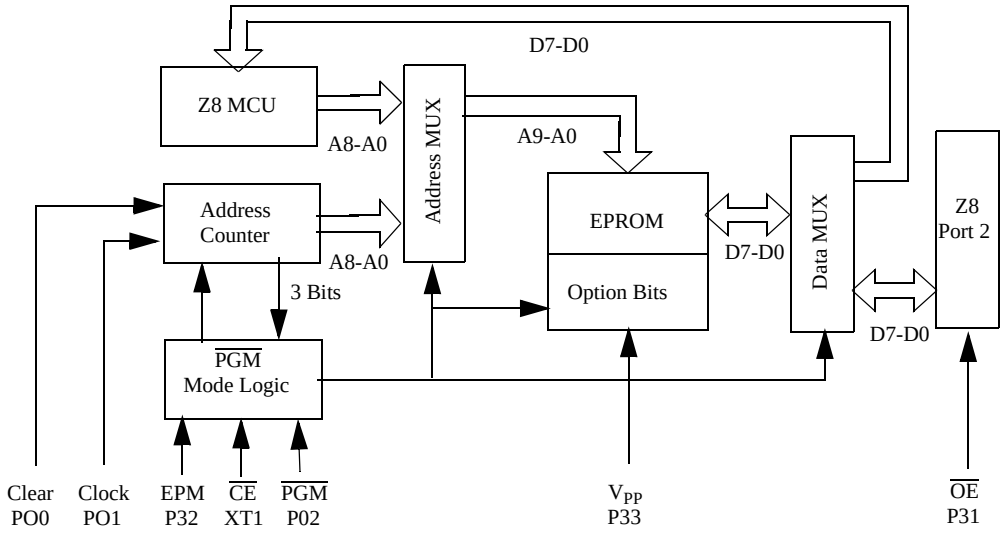


**Figure 2. EPROM Programming Mode Block Diagram**

**Table 8. DC Characteristics, Standard Temperature Range (Continued)**

| TA = 0°C to +70°C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Sym** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Typical @ 25°C[1] Units** | | **Conditions** | **Notes** |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | | 0 | $V_{CC}$ - 1.0 | | V | | |
| $I_{CC}$ | Supply Current | 3.5V | 3.5 | | 1.5 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | 7.0 | | 6.8 | mA | @ 2 MHz | 3,6 |
| | | 3.5V | 8.0 | | 3.0 | mA | @ 8 MH | 3,6 |
| | | 5.5V | 11.0 | | 8.2 | mA | @ 8 MHz | 3,6 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 3.5V | 2.5 | | 0.7 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | 4.0 | | 2.5 | mA | @ 2 MHz | 3,6 |
| | | 3.5V | 4.0 | | 1.0 | mA | @ 8 MHz | 3,6 |
| | | 5.5V | 5.0 | | 3.0 | mA | @ 8 MHz | 3,6 |
| $I_{CC}$ | Supply Current (HALT and Low EMI Mode) | 3.5V | 3.5 | | 1.5 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | 7.0 | | 6.8 | mA | @ 1 MHz | 6,10 |
| | | 3.5V | 5.8 | | 2.5 | mA | @ 2 MHz | 6,10 |
| | | 5.5V | 9.0 | | 7.5 | mA | @ 2 MHz | 6,10 |
| | | 3.5V | 8.0 | | 3.0 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | 11.0 | | 8.2 | mA | @ 4 MHz | 6,10 |
| $I_{CC1}$ | Standby Current (Low EMI Mode) | 3.5V | 1.2 | | 0.4 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | 1.6 | | 0.9 | mA | @ 1 MHz | 6,10 |
| | | 3.5V | 1.5 | | 0.5 | mA | @ 2 MHz | 6,10 |
| | | 5.5V | 1.9 | | 1.0 | mA | @ 2 MHz | 6,10 |
| | | 3.5V | 2.0 | | 0.8 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | 2.4 | | 3.0 | mA | @ 4 MHz | 6,10 |
| $I_{CC2}$ | Standby Current (STOP Mode) | 3.5V | 10.0 | | 1.0 | µA | WDT is not Running | 6,7,8 |
| | | 5.5V | 10.0 | | 1.0 | µA | WDT is not Running | 6,7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 3.5V | 12.0 | | 3 | µA | $0V < V_{IN} < V_{CC}$ | 9 |
| | | 5.5V | 32.0 | | 16 | µA | $0V < V_{IN} < V_{CC}$ | 9 |

**Table 8. DC Characteristics, Standard Temperature Range (Continued)**

| TA = 0°C to +70°C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Sym** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Typical @ 25°C[1]** | **Units** | **Conditions** | **Notes** |
| $I_{ALH}$ | Auto Latch High Current | 3.5V | -8.0 | | -1.5 | µA | $0V < V_{IN} < V_{CC}$ | 9 |
| | | 5.5V | -16.0 | | -8.0 | µA | $0V < V_{IN} < V_{CC}$ | 9 |

1. Typical values are read at a $V_{CC}$ of 5.0V and $V_{CC}$ of 3.5V.
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not low EMI mode).
4. These values apply while operating in RUN mode or HALT mode.
5. These values apply while operating in STOP mode.
6. All outputs are unloaded and all inputs are at the $V_{CC}$ or $V_{SS}$ level.
7. If the analog comparator is selected, then the comparator inputs must be at the $V_{CC}$ level.
8. A 10-M pull-up resistor is required in the circuit between the $X_{IN}$ pin to the $V_{CC}$ pin.
9. Auto latches are enabled.
10. Low EMI Mode (not Standard Mode)

## Extended Temperature Range

Table 9 provides Direct Current characteristics for the Z86E02 SL1925 microcontroller, at an extended ambient temperature range of -40°C to 105°C.

**Table 9. DC Characteristics, Extended Temperature Range**

| | | | TA = -40°C to +105°C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Sym** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Typical @ 25°C[1]** | **Units** | **Conditions** | **Notes** |
| $V_{INMAX}$ | Max Input Voltage | 4.5V | | 12.0 | | V | $I_{IN} < 250$ µA | 2 |
| | | 5.5V | | 12.0 | | V | $I_{IN} < 250$ µA | 2 |
| $V_{CH}$ | Clock Input High Voltage | 4.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 4.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$-0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |

**Table 9. DC Characteristics, Extended Temperature Range (Continued)**

| | | | TA = -40°C to +105°C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Sym** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Typical @ 25°C[1]** | **Units** | **Conditions** | **Notes** |
| $I_{CC}$ | Supply Current | 4.5V | | 7.0 | 6.8 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | | 7.0 | 6.8 | mA | @ 2 MHz | 3,6 |
| | | 4.5V | | 11.0 | 8.2 | mA | @ 8 MHz | 3,6 |
| | | 5.5V | | 11.0 | 8.2 | mA | @ 8 MHz | 3,6 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 4.5V | | 3.0 | 2.5 | mA | @ 2 MHz | 3,6 |
| | | 5.5V | | 3.0 | 2.5 | mA | @ 2 MHz | 3,6 |
| | | 4.5V | | 5.0 | 3.0 | mA | @ 8 MHz | 3,6 |
| | | 5.5V | | 5.0 | 3.0 | mA | @ 8 MHz | 3,6 |
| $I_{CC}$ | Supply Current (Low EMI Mode) | 4.5V | | 7.0 | 6.8 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | | 7.0 | 6.8 | mA | @ 1 MHz | 6,10 |
| | | 4.5V | | 9.0 | 7.5 | mA | @ 2 MHz | 6,10 |
| | | 5.5V | | 9.0 | 7.5 | mA | @ 2 MHz | 6,10 |
| | | 4.5V | | 11.0 | 8.2 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | | 11.0 | 8.2 | mA | @ 4 MHz | 6,10 |
| $I_{CC1}$ | Standby Current (HALT and Low EMI Mode) | 4.5V | | 1.6 | 0.9 | mA | @ 1 MHz | 6,10 |
| | | 5.5V | | 1.6 | 0.9 | mA | @ 1 MHz | 6,10 |
| | | 4.5V | | 1.9 | 1.0 | mA | @ 2 MHz | 6,10 |
| | | 5,5V | | 1.9 | 1.0 | mA | @ 2 MHz | 6,10 |
| | | 4.5V | | 2.4 | 3.0 | mA | @ 4 MHz | 6,10 |
| | | 5.5V | | 2.4 | 3.0 | mA | @ 4 MHz | 6,10 |
| $I_{CC2}$ | Standby Current (Stop mode) | 4.5V | | 20 | 1.0 | µA | WDT is not Running | 6,7,8 |
| | | 5.5V | | 20 | 1.0 | µA | WDT is not Running | 6,7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 4.5V | | 40 | 16 | µA | $0V < V_{IN} < V_{CC}$ | 9 |
| | | 5.5V | | 40 | 16 | µA | $0V < V_{IN} < V_{CC}$ | 9 |

**Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)**

| | | | TA = 0°C to +70°C | | | | |
|---|---|---|---|---|---|---|---|
| | | | 8MHz | | | | |
| **No** | **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Units** | **Notes** |
| 4 | $T_WT_{IN}L$ | Timer Input Low Width | 3.5V | 100 | | ns | 1 |
| | | | 5.5V | 70 | | ns | 1 |
| 5 | $T_WT_{IN}H$ | Timer Input High Width | 3.5V | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | | 1 |
| 6 | $T_PT_{IN}$ | Timer Input Period | 3.5V | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | | 1 |
| 7 | $T_RT_{IN}$, $T_TT_{IN}$ | Timer Input Rise and Fall Time | 3.5V | | 100 | ns | 1 |
| | | | 5.5V | | 100 | ns | 1 |
| 8 | $T_WIL$ | Interrupt Request Input Low Time | 3.5V | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | ns | 1,2 |
| 9 | $T_WIH$ | Interrupt Request Input High Time | 3.5V | 5TpC | | | 1,2 |
| | | | 5.5V | 5TpC | | | 1,2 |
| 10 | $T_{WDT}$ | Watch-Dog Timer Delay Time before Time-out | 3.5V | 10 | | ms | |
| | | | 5.5V | 5 | | ms | |
| 11 | $T_{POR}$ | Power-On Reset Time | 3.5V | 4 | 36 | ms | |
| | | | 5.5V | 2 | 18 | ms | |

1. Timing reference is 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0
2. Interrupt request through Port 3 (P33-P31)

## LOW EMI Mode at Standard Temperature

Table 12 describes timing characteristics in LOW EMI mode at standard temperature for the timing diagram noted in Figure 8.

**Table 12. AC Electrical Timing, Standard Mode at Extended Temperature**

| | | | TA = 0°C to +70°C | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1MHz | | 4MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | $T_PC$ | Input Clock Period | 3.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | $T_RC$,$T_FC$ | Clock Input Rise and Fall Times | 3.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | $T_WC$ | Input Clock Width | 3.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4 | $T_WT_{IN}L$ | Timer Input Low Width | 3.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | $T_WT_{IN}H$ | Timer Input High Width | 3.5V | 3TpC | | 3TpC | | | 1 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1 |
| 6 | $T_PT_{IN}$ | Timer Input Period | 3.5V | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1 |
| 7 | $T_RT_{IN}$, $T_TT_{IN}$ | Timer Input Rise and Fall Time | 3.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | $T_WIL$ | Interrupt Request Input Low Time | 3.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | $T_WIH$ | Interrupt Request Input High Time | 3.5V | 3TpC | | 3TpC | | | 1,2 |
| | | | 5.5V | 3TpC | | 3TpC | | | 1,2 |
| 10 | $T_{WDT}$ | Watch-Dog Timer Delay Time before Time-out | 3.5V | 10 | | 10 | | ms | |
| | | | 5.5V | 5 | | 5 | | ms | |

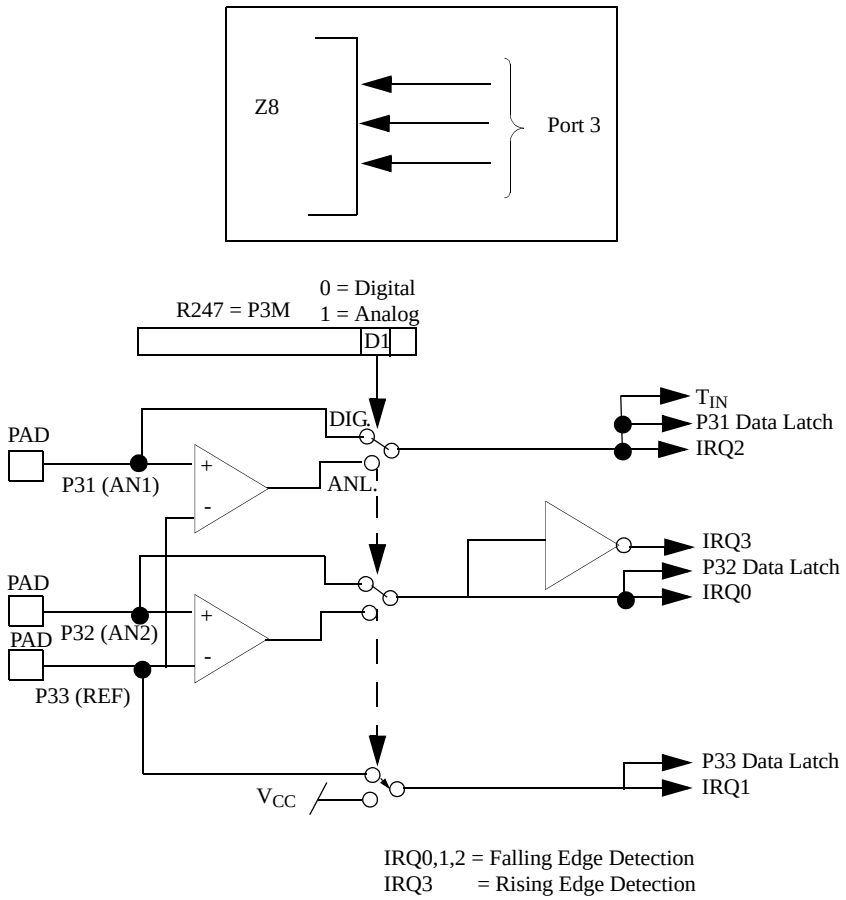


**Figure 11. Port 3 Configuration**

**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, AID conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4 V when the $V_{CC}$ is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt gener-

# Functional Description

The following special functions are incorporated into the Z8® devices to enhance the standard Z8 core architecture and to provide the user with increased design flexibility.

## RESET

A RESET can be triggered in the following two ways:

- Power-On Reset
- Watch-Dog Timer Reset

### Power-On Reset (POR)

Upon power-up, the Power-On Reset circuit waits for $T_{POR}$ ms, plus 18 clock cycles, then starts program execution at address 000Ch (Figure 12). The Z8® control registers' reset value is indicated in Table 14.

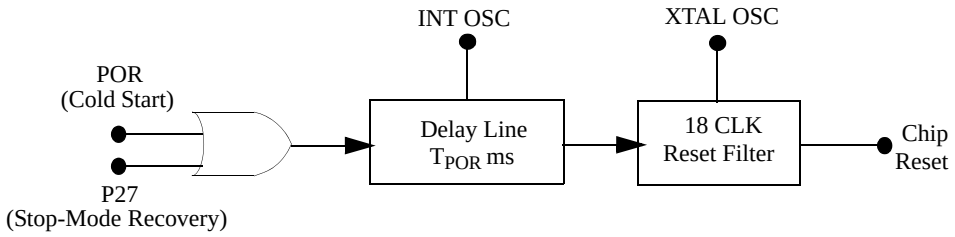


**Figure 12. Internal Reset Configuration**

## Counter/Timer

There is one 8-bit programmable counter/timer (T1), driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources (Figure 16).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO-N CONTINUOUS mode).

The counter, but not the prescaler, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The TIMER mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

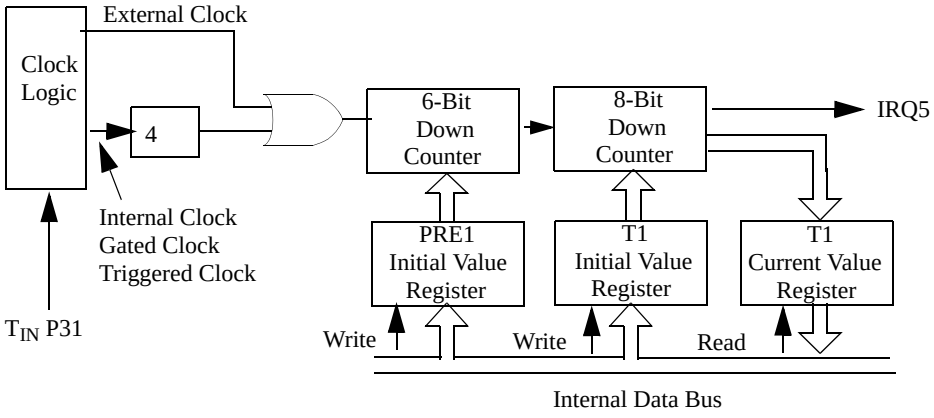


**Figure 16. Counter/Timer Block Diagram**

## Interrupts

The Z8® features six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 17). The sources are divided as follows: the falling edge of P31 (AN 1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), by software, and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Interrupt Types, Sources, and Vectors).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8® interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

**Note:** The rising edge interrupt is not supported. on the CCP emulator (a hardware/software work around must be employed).

## Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

## Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX      Push RP
                LD RP, #0Fh
                LD R0, #0FFh
                POP RP
```

**Table 15. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | AN2(P32) | 0,1 | External (F) Edge |
| IRQ1 | REF(P33) | 2,3 | External (F) Edge |
| IRQ2 | AN1 (P31) | 4,5 | External (F) Edge |
| IRQ3 | AN2 (P32) | 6,7 | External (R) Edge |
| IRQ4 | Software | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |
| Note: Note: F = Falling edge triggered: R = Rising edge triggered | | | |

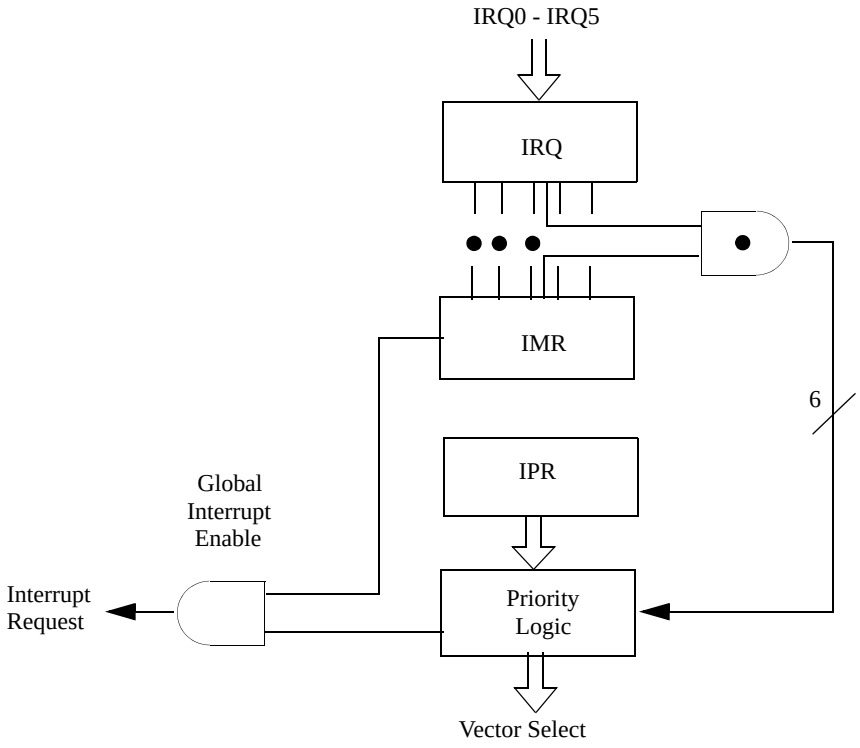


**Figure 17. Interrupt Block Diagram**

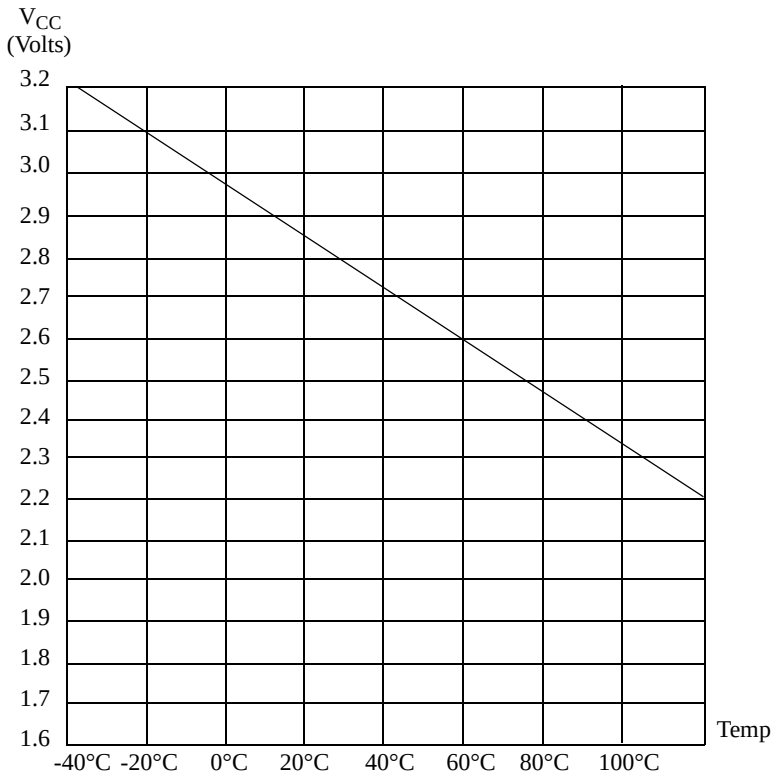


**Figure 19. Typical Auto Reset Voltage ($V_{LV}$) vs. Temperature**

## OTP Option Bit Description

One-Time Programmable EPROM option bits for the device are described in this section. The Z86E02 SL1925 must be power-cycled to fully implement the selected option after programming.

**Low-EMI Emission.** The Low EMI option bit, when programmed, enables the Z8 to operate in a low-EMI emission (low-noise) mode. Use of this feature results in:

- All pre-driver slew rates are typically reduced to 10 ns
- Internal SCLK /TCLK operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 200 ohms
- Oscillator divide-by-two circuitry eliminated

**RC Oscillator.** The RC Oscillator option bit, when programmed, enables the internal RC oscillator to connect to the XTAL2 and XTAL1 pins while disabling the internal crystal oscillator to XTAL2 and XTAL1.

**Table 19. Prescaler 1 Register, R243 PRE1 F3h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | X | X | X | X | X | X | X | X |
| Note: R = Read, W = Write, X = Indeterminate | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-2 | Prescaler | W | X | **Prescaler Modulo**<br>Range = 1-64 decimal; 01h-00h |
| 1 | Clock | W | 0 | **Clock Source**<br>0: T1 External Timing Input ($T_{IN}$) Mode<br>1: Internal |
| 0 | Count | W | 0 | **TI Count Mode**<br>0: Single Pass<br>1: Modulo N |

**Table 20. Port 2 Mode Register, R246 P2M F6h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | W | W | W | W | W | W | W | W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Note: W = Write, | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-0 | P20-P27 | W | 1 | **P20-P27 I/O Definition**<br>0: Defines bit as Output<br>1: Defines bit as Input |

**Table 23. Interrupt Priority Register, R249 IPR F9h Bank 0h: WRITE ONLY**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | W | W | W | W | W | W | W | W |
| Reset | X | X | X | X | X | X | X | X |

Note: W = Write, X = Indeterminate

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-6 | Reserved | W | X | Reserved-must be 0 |
| 5 | IRQ3, IRQ5 | W | X | **IRQ3, IRQ5 Priority (Group A)**<br>0: IRQ5 > IRQ3<br>1: IRQ3 < IRQ5 |
| 4, 3, 0 | Interrupt | W | X | **Interrupt Group Priority**<br>000: Reserved*<br>001: C>A>B<br>010: A>B>C<br>011: A>C>B<br>100: B>C>A<br>101: C>B>A<br>110: B>A>C<br>111: Reserved |
| 2 | IRQ0, IRQ2 | W | X | **IRQ0, IRQ2 Priority (Group B)**<br>0: IRQ2 > IRQ0<br>1: IRQ0 < IRQ2 |
| 1 | IRQ1, IRQ4 | W | X | **IRQ1, IRQ4 Priority (Group C)**<br>0: IRQ1 > IRQ4<br>1: IRQ4 < IRQ1 |

Note: *Selecting a Reserved mode causes an undefined operation.

**Table 24. Interrupt Request Register, R250 IPR FAh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Note: R = Read, W = Write | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-6 | Reserved | R/W | 00 | Reserved-must be 0 |
| 5 | IRQ5 | R/W | 0 | **Interrupt**<br>IRQ5 = T1<br>0: No interrupt pending<br>1: Interrupt pending |
| 4 | IRQ4 | R/W | **0** | **Interrupt**<br>RQ4 = Software generated<br>0: No interrupt pending<br>1: Interrupt pending |
| 3 | IRQ3 | R/W | **0** | **Interrupt**<br>RQ3 = P32 Input (rising edge)<br>0: No interrupt pending<br>1: Interrupt pending |
| 2 | IRQ2 | R/W | **0** | **Interrupt**<br>RQ2 = P31 Input<br>0: No interrupt pending<br>1: Interrupt pending |
| 1 | IRQ1, | R/W | **0** | **Interrupt**<br>RQ1 = P33 Input<br>0: No interrupt pending<br>1: Interrupt pending |
| 0 | IRQ0 | R/W | **0** | **Interrupt**<br>RQ0 = P32 Input<br>0: No interrupt pending<br>1: Interrupt pending |
| Note: *Selecting a Reserved mode causes an undefined operation. | | | | |

**Table 25. Interrupt Mask Register, R251 IMR FBh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Note: R = Read, W = Write | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7 | Master Interrupt Enable | R/W | 0 | 0: Disables global interrupts*<br>1: Enables global interrupts* |
| 6 | Reserved | R/W | X | Reserved-must be 0 |
| 5-0 | IRQ0-IRQ5 | R/W | X | 1: Enables IRQ0-IRQ5 (D0 = IRQ0) |
| Note: *Must use Ei/Di instruction to set/reset this bit. | | | | |

**Table 26. Flag Register, R252 FCh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | X | X | X | X | X | X | X |
| Note: R = Read, X= Indeterminate | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7 | Carry | R/W | X | Carry Flag |
| 6 | Zero | R/W | X | Zero Flag |
| 5 | Sign | R/W | X | Sign Flag |
| 4 | Overflow | R/W | X | Overflow Flag |
| 3 | Decimal Adjust | R/W | X | Decimal Adjust Flag |
| 2 | Half Carry | R/W | X | Half Carry Flag |
| 1 | User | R/W | X | User Flag F2* |
| 0 | User | R/W | X | User Flag F1* |
| Note: *Not affected by RESET. | | | | |

**Table 27. Register Pointer, R253 RP FDh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Note: R = Read, W= Write | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-4 | Working Register Pointer | R/W | 0 | Working Register Pointer |
| 3-0 | Reserved | R/W | X | Reserved-must be 0 |

**Table 28. General-Purpose Register, R254 GPR FEh Bank 0h: READ/WRITE**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Note: R = Read, W= Write | | | | | | | | |

| Bit Position | Bit Field | R/W | Reset Value | Description |
|---|---|---|---|---|
| 7-0 | Stack | R/W | 0 | General-Purpose Register |