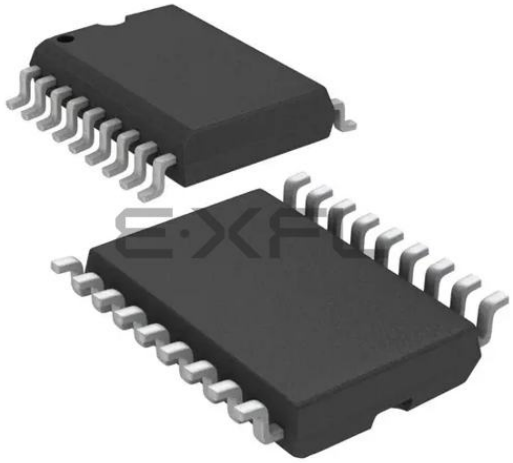

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0208sec1925

Architectural Overview

ZiLOG's Z86E02 SL1925 Microcontroller (MCU) is a One-Time Programmable (OTP) member of ZiLOG's single-chip Z8® MCU family that allows easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E02 SL1925's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O. One on-chip counter/timer, with a large number of user-selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Z86E02 SL1925 Features

Table 1. Z86E02 SL1925 Features

Device	OTP (KB)	RAM* (Bytes)	Speed (MHz)
Z86E02 SL1925	0.5	61	8

Note: *General-Purpose.

- 3.5V to 5.5V Operating Range @ 0°C to +70°C
- 4.5V to 5.5V Operating Range @ -40°C to +105°C
- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 1 timer, 1 software)
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - RC Oscillator
- One Programmable 8-Bit Counter/Timer, with 6-bit Programmable Prescaler
- WDT/Power-On Reset (POR)
- On-Chip Oscillator that accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset

PIN DESCRIPTION

Pin diagrams and identification for the device are displayed in Figure 3 through Figure 6, and in Table 2 through Table 5.

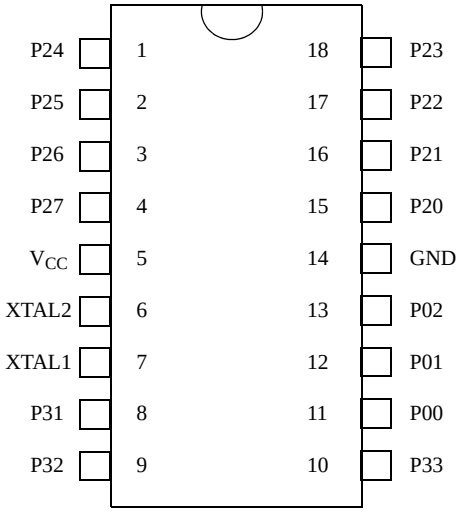


Figure 3. 18-Pin DIP/SOIC Configuration, STANDARD Mode

Table 2. 18-Pin DIP/SOIC Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4-7	Input/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1 AN1	Input
9	P32	Port 3, Pin 1 AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0-2	Input/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0-3	Input/Output

Table 8. DC Characteristics, Standard Temperature Range (Continued)

TA = 0°C to +70°C								
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1] Units**		**Conditions**	**Notes**
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} - 1.0		V		
I_{CC}	Supply Current	3.5V	3.5		1.5	mA	@ 2 MHz	3,6
		5.5V	7.0		6.8	mA	@ 2 MHz	3,6
		3.5V	8.0		3.0	mA	@ 8 MH	3,6
		5.5V	11.0		8.2	mA	@ 8 MHz	3,6
I_{CC1}	Standby Current (HALT Mode)	3.5V	2.5		0.7	mA	@ 2 MHz	3,6
		5.5V	4.0		2.5	mA	@ 2 MHz	3,6
		3.5V	4.0		1.0	mA	@ 8 MHz	3,6
		5.5V	5.0		3.0	mA	@ 8 MHz	3,6
I_{CC}	Supply Current (HALT and Low EMI Mode)	3.5V	3.5		1.5	mA	@ 1 MHz	6,10
		5.5V	7.0		6.8	mA	@ 1 MHz	6,10
		3.5V	5.8		2.5	mA	@ 2 MHz	6,10
		5.5V	9.0		7.5	mA	@ 2 MHz	6,10
		3.5V	8.0		3.0	mA	@ 4 MHz	6,10
		5.5V	11.0		8.2	mA	@ 4 MHz	6,10
I_{CC1}	Standby Current (Low EMI Mode)	3.5V	1.2		0.4	mA	@ 1 MHz	6,10
		5.5V	1.6		0.9	mA	@ 1 MHz	6,10
		3.5V	1.5		0.5	mA	@ 2 MHz	6,10
		5.5V	1.9		1.0	mA	@ 2 MHz	6,10
		3.5V	2.0		0.8	mA	@ 4 MHz	6,10
		5.5V	2.4		3.0	mA	@ 4 MHz	6,10
I_{CC2}	Standby Current (STOP Mode)	3.5V	10.0		1.0	µA	WDT is not Running	6,7,8
		5.5V	10.0		1.0	µA	WDT is not Running	6,7,8
I_{ALL}	Auto Latch Low Current	3.5V	12.0		3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	32.0		16	µA	$0V < V_{IN} < V_{CC}$	9

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			TA = -40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	3
		5.5V	V_{CC}-0.4		4.8	V	I_{OH}= -2.0 mA	3
		4.5V	V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	10
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	10
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		4.5V		0.4	0.1	V	I_{OL}=1.0 mA	10
		5.5V		0.4	0.1	V	I_{OL}=1.0 mA	10
V_{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	I_{OL} = +12 mA	3
		5.5V		1.0	0.3	V	I_{OL} = +12 mA	3
V_{LV}	V_{CC} Low Voltage Auto Reset		2.3	3.5	2.9	V	@ 4 MHz Maximum Internal Clock Frequency	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		-1.0	1.0	µA	V_{IN}= 0V, V_{CC}	
		5.5V		-1.0	1.0	µA	V_{IN}= 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V		-1.0	1.0	µA	V_{IN}= 0V, V_{CC}	
		5.5V		-1.0	1.0	µA	V_{IN}= 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}- 1.5		V		

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			TA = -40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{ALH}	Auto Latch High Current	4.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	9

1. Typical values are read at a V_{CC} of 5.0V
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not Low EMI mode).
4. These values apply while operating in RUN mode or HALT mode
5. These values apply while operating in STOP mode
6. All outputs are unloaded and all inputs are at the V_{CC}or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the XTAL1 pin to the V_{CC} pin.
9. Auto latches are enabled.
10. Low EMI Mode (not Standard Mode)

Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	100		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	100		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	3.5V	4	36	ms	
			5.5V	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Standard Temperature

Table 12 describes timing characteristics in LOW EMI mode at standard temperature for the timing diagram noted in Figure 8.

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = 0°C to +70°C						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	3.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	3TpC		3TpC			1,2
			5.5V	3TpC		3TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		10		ms	
			5.5V	5		5		ms	

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature (Continued)

				TA = 0°C to +70°					
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	T_{POR}	Power-On Reset Time	3.5V	2	18	2	18	ms	
			5.5V	2	18	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Extended Temperature

Table 13 describes timing characteristics in LOW EMI mode at extended temperature for the timing diagram noted in Figure 8.

Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature

				TA = 0°C to +70°C					
				1MHz		4MHz			
No	Symbol	Parameter	Vcc	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1

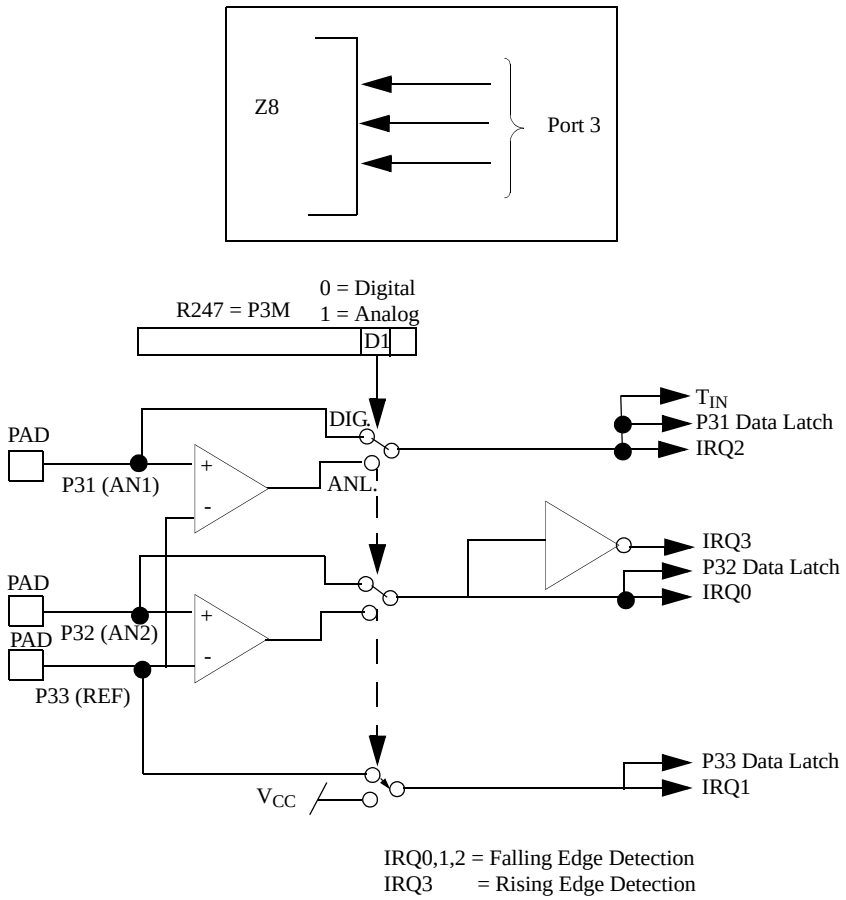


Figure 11. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, AID conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt gener-

Functional Description

The following special functions are incorporated into the Z8® devices to enhance the standard Z8 core architecture and to provide the user with increased design flexibility.

RESET

A RESET can be triggered in the following two ways:

- Power-On Reset
- Watch-Dog Timer Reset

Power-On Reset (POR)

Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000Ch (Figure 12). The Z8® control registers' reset value is indicated in Table 14.

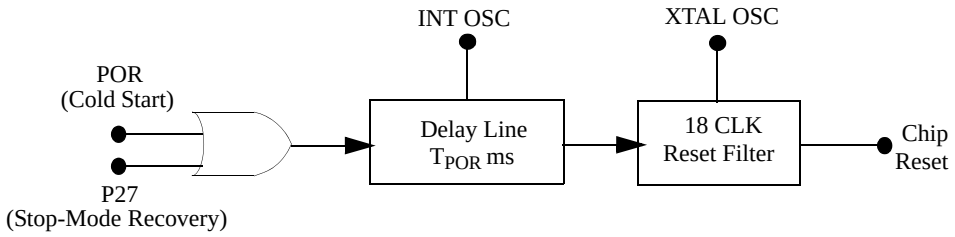


Figure 12. Internal Reset Configuration

Location		Identifiers
255(FFh)	Stack Pointer (Bits 7-0)	SPL
254(FEh)	General-Purpose Register	GPR
253(FDh)	Register Pointer	RP
252(FCh)	Program Control Flags	Flags
251(FBh)	Interrupt Mask Register	IMR
250(FBh)	Interrupt Request Register	IRQ
249(FAh)	Interrupt Priority Register	IRP
248(F8h)	Ports 0-1 Mode	P01M
247(F7h)	Port 3 Mode	P3M
246(F6h)	Port 2 Mode	P2M
245(F5h)	Reserved	Reserved
244(F4h)	Reserved	Reserved
243(F3h)	T1 Prescaler	PRE1
242(F2h)	TimerCounter1	T1
241(F1h)	Timer Mode	TMR
240(F0h) 64(40h)	Not Implemented	
63(30h) 4(04h)	General-Purpose Registers	
3(03h)	Port 3	P3
2(02h)	Port 2	P2
1(01h)	Reserved	Reserved
0(00h)	Port 0	P0

Figure 14. Register File

The Z8® instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing short 4-bit register addressing mode using the Register Pointer.

In the 4-bit address mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 15) addresses the starting location of the active working-register group.

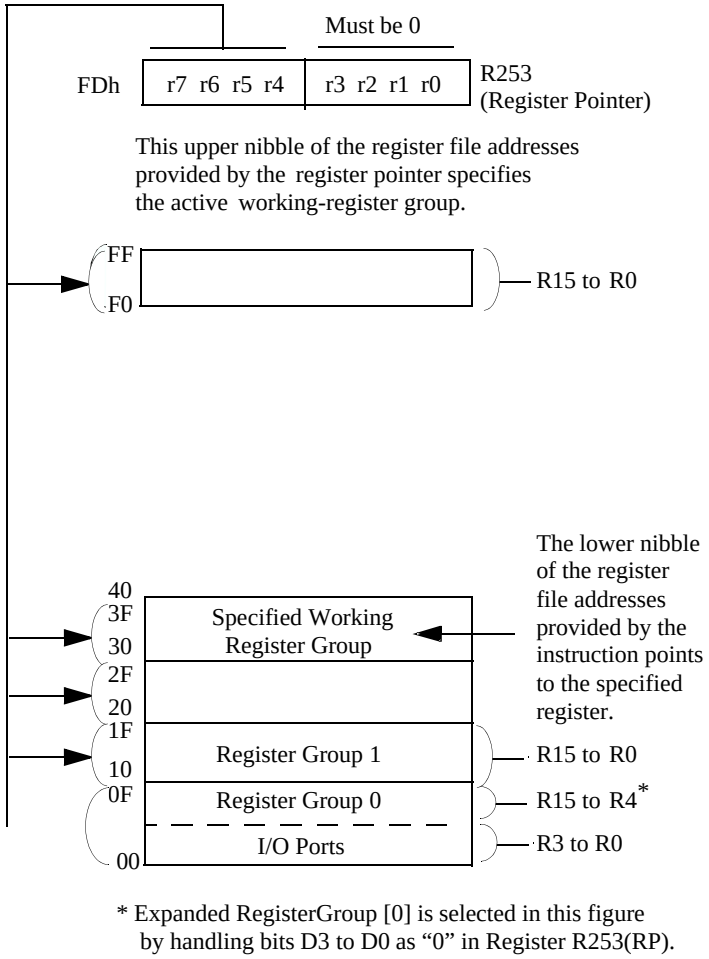


Figure 15. Register Pointer

Stack Pointer

The Z8® features an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60 general-purpose registers from 04h to 3Fh.

General-Purpose Registers (GPR)

These registers are undefined after the device is powered up. The registers keep their most recent value after any reset, as long as the reset occurs in the V_{CC} volt-age-specified operating range.

Note: Register R254 is designated as a general-purpose register and is set to 00h after any reset or Stop-Mode Recovery.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8® interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

Note: The rising edge interrupt is not supported. on the CCP emulator (a hardware/software work around must be employed).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX      Push RP
                LD RP, #0Fh
                LD R0, #0FFh
                POP RP
```

Table 15. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1 (P31)	4,5	External (F) Edge
IRQ3	AN2 (P32)	6,7	External (R) Edge
IRQ4	Software	8,9	Internal
IRQ5	T1	10,11	Internal
Note: Note: F = Falling edge triggered: R = Rising edge triggered			

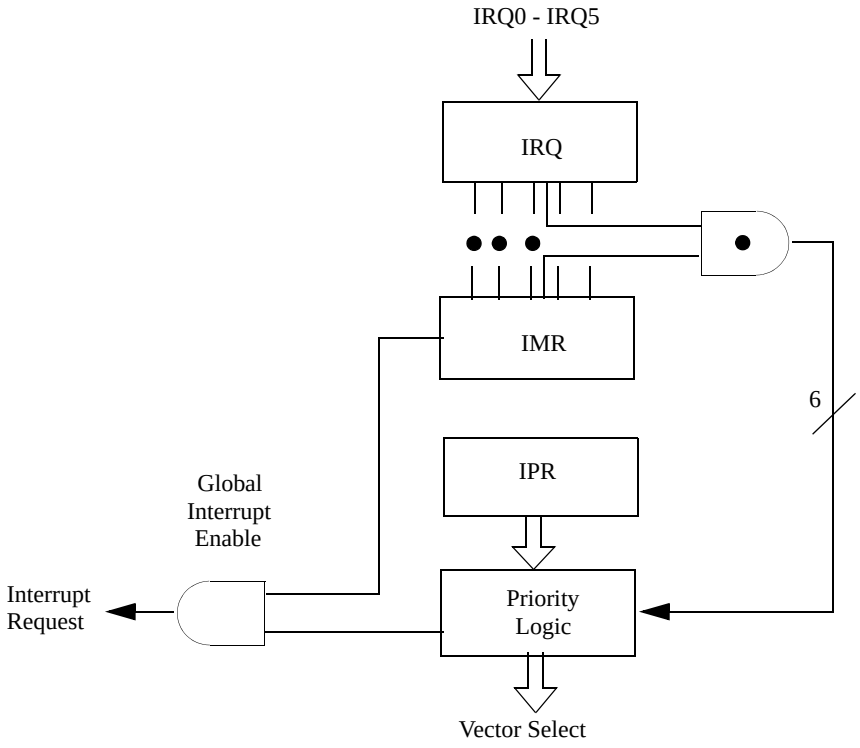


Figure 17. Interrupt Block Diagram

Table 16. Typical Frequency (MHz) vs. RC Values V_{CC} = 5.0 V @ 25°C (Continued)

	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
Resistor (R)	A	B	A	B	A	B	A	B
5 KΩ	7.6	1.6	3.6	1.0	2.3	0.7	0.28	0.14
2 KΩ	12.5	2.3	8.5	1.7	4.1	1.3	0.66	0.27
1 KΩ	17	3.1	13	2.5	9.5	1.8	1.2	0.42

1. A = Standard mode frequency
2. B = Low EMI mode frequency

HALT Mode

This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

Note: The device can be recovered by a WDT timeout. The WDT reset in HALT Mode generates a full reset similar to the Normal run mode (not STOP Mode).

STOP Mode

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 A. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A LOW INPUT condition on P27 releases the STOP mode. Program execution begins at location 000C (Hex). Refer to the Watch Dog Timer (WDT) section for information relating to WDT wakeup out of Stop Mode. However, when P27 is used to release STOP mode, the I/O port mode registers are not reconfigured to their default POWER-ON conditions. Thus the I/O, configured as output when the STOP instruction was executed, is prevented from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Note: X = Dependent on user's application.

Note: Any Low level detected on pin P27 takes the device out of STOP mode, even if it is configured as an output. It is not edge triggered.

To enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate SLEEP instruction, such as:

```
FFh     NOP     ; clear the pipeline
6Fh     STOP    ; enter STOP mode
        or
FFH     NOP     ; clear the pipeline
7Fh     HALT    ; enter HALT mode
```

Note: On the CCP emulator, a software workaround must be used to enable P27 as the Stop-Mode Recovery source. This workaround follows.

Software Work Around on the Z86CCP01ZEM Emulator to Enable P27 as Stop-Mode Recovery Source

```
SWFIXP27:   PUSH RP
            LD RP, #0Fh
            LD R012, #001101X0B     X= 1 for LOW EMI Mode
                                    X= 0 for STANDARD Mode
            POP RP
```

Watch-Dog Timer (WDT)

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 T_{WDT} period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z = 1, S = 0, V = 0.

WDT = 5Fh

Op Code WDT (5Fh)

The first time Op Code 5Fh is executed, the WDT is enabled; subsequent execution clears the WDT counter. This clearing of the counter must be performed at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 crystal clock cycles. The software enabled WDT does not run in STOP mode.

On the CCP emulator, a software workaround must be used to emulate the software WDT. This workaround follows.

```
SWFIXSWDT:    PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Op Code WDH (4Fh)

When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters – it just makes it possible to operate the WDT during HALT mode. A WDH instruction executed without executing WDT (5Fh) yields no effect.

Note: On the CCP emulator, a software workaround must be used to enable the software in HALT Mode/STOP Mode or hardware-enabled WDT. This workaround follows.

Software Work Around on the Z86CCP01ZEM Emulator to Emulate the Software WDT Running in HALT Mode

```
SWFIXSWDT:    PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Permanent WDT

Selecting the hardware-enabled Permanent WDT option bit automatically enables the WDT upon exiting reset. The permanent WDT always runs in HALT mode and STOP mode, and it cannot be disabled.

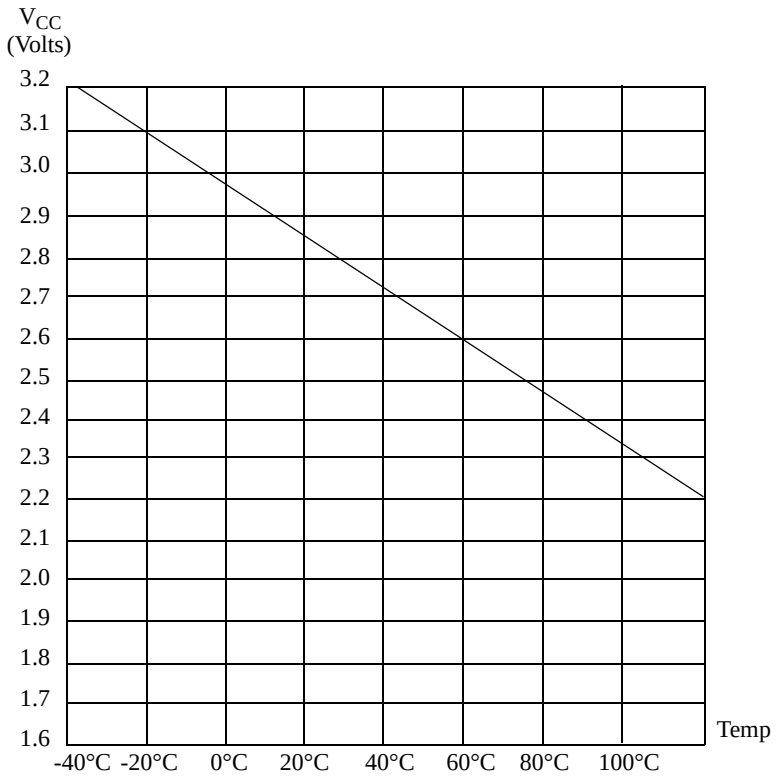


Figure 19. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

OTP Option Bit Description

One-Time Programmable EPROM option bits for the device are described in this section. The Z86E02 SL1925 must be power-cycled to fully implement the selected option after programming.

Low-EMI Emission. The Low EMI option bit, when programmed, enables the Z8 to operate in a low-EMI emission (low-noise) mode. Use of this feature results in:

- All pre-driver slew rates are typically reduced to 10 ns
- Internal SCLK /TCLK operation limited to a maximum of 4 MHz–250 ns cycle time
- Output drivers typically exhibit resistances of 200 ohms
- Oscillator divide-by-two circuitry eliminated

RC Oscillator. The RC Oscillator option bit, when programmed, enables the internal RC oscillator to connect to the XTAL2 and XTAL1 pins while disabling the internal crystal oscillator to XTAL2 and XTAL1.

Control Registers

Table 17. Timer Mode Register, R241 TMR F1h Bank 0h: READ/WRITE

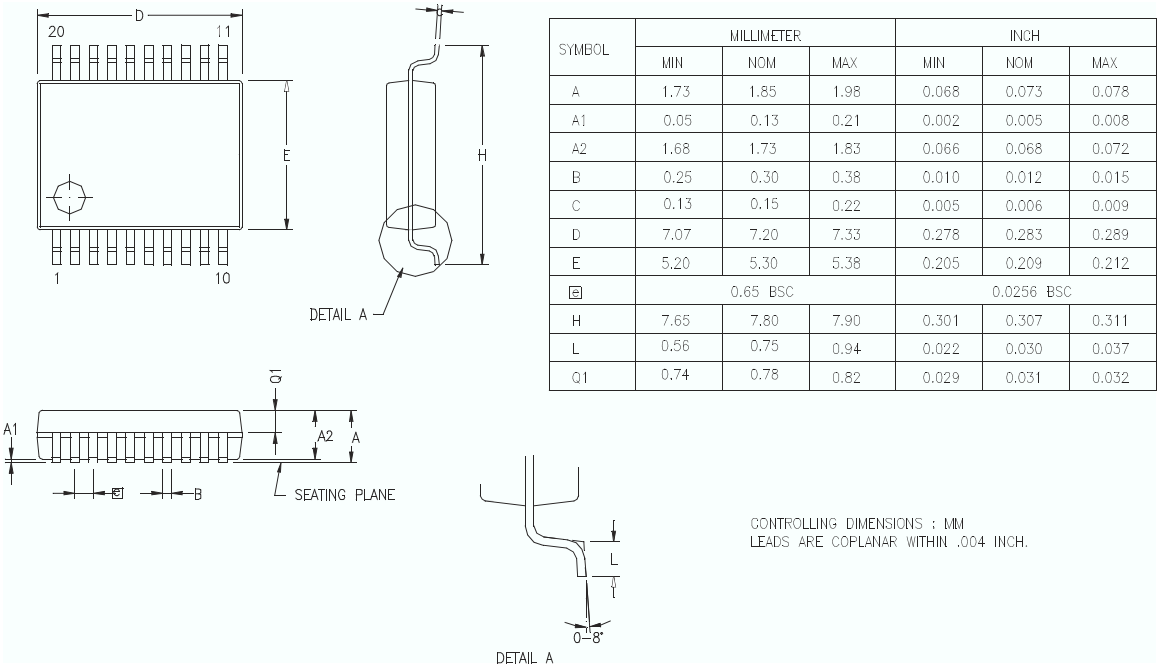
Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	R/W	00	Reserved-must be 0
5-4	T_{IN} Mode	R/W	0	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (non retriggerable) 11: Trigger Input (retriggerable)
3	T1 Count	R/W	0	**TI Count** 0: Disable 1: Enable
2	T1	R/W	0	**TI** 0: No Function 1: Load T1
1-0	Reserved	R/W	0	Reserved - must be 0

Table 18. Counter/Timer 1 Register, R242 T1 F2h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	T1	R	X	**T1 Current Value**
		W	X	**T1 Initial Value** Range = 1-256 decimal; 01h-00h



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 22. 20-Pin SSOP Package Diagram

Ordering Information

Table 30. Ordering Information

Pin Count	Package	Size (KB)	Description
18	DIP	0.5	Z86E0208PSC1925
			Z86E0208PEC1925
	SOIC	0.5	Z86E0208SSC1925
			Z86E0208SEC1925
20	SSOP	0.5	Z86E0208HSC1925
			Z86E0208HEC1925

Note: The Standard temperature range is 0°C to 70°C. For parts that operate in the Extended temperature range of -40°C to 105°C, substitute the letter E for the letter S. For example, the PSI number for an 18-pin DIP operating at 8 MHz in the extended temperature range is Z86E0208PEC