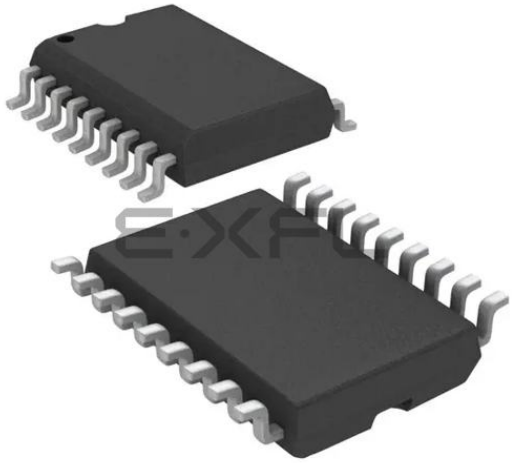

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0208sec1925tr

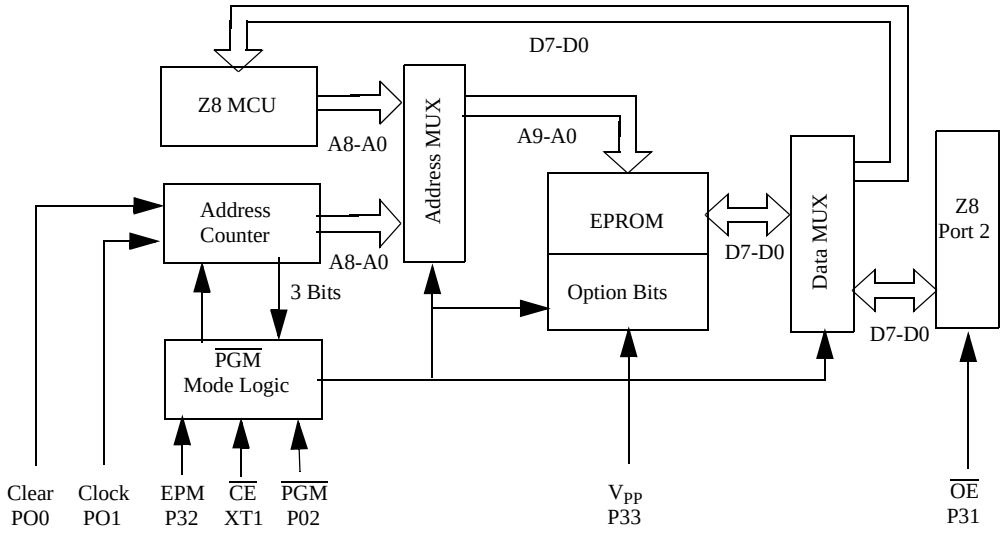

Figure 2. EPROM Programming Mode Block Diagram

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed on Table 6 may cause permanent damage to the device. This rating is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mΩ for the package. See Table 6. Power dissipation is calculated as follows:

Total Power Dissipation = V_{CC} X [I_{CC}–(sum of I_{OH})]
+sum of [(V_{CC}–V_{OH}) X I_{OH}]
+ sum of (V_{OL} X I_{OL})

Table 6. Absolute Maximum Ratings

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	-40	+105	C	
Storage Temperature	-65	+150	C	
Voltage on any Pin with Respect to V_{SS}	-0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V	
Voltage on XTAL1, P31, P32, P33 with respect to V_{SS}	-0.6	V_{DD}+1	V	3
Total Power Dissipation		462	mΩ	
Maximum Allowable Current out of V_{SS}		300	mA	
Maximum Allowable Current into V_{DD}		270	mA	
Maximum Allowable Current into an Input Pin	-600	+600	µA	4
Maximum Allowable Current into an Open-Drain Pin	-600	+600	µA	2
Maximum Allowable Output Current Linked by any I/O Pin		20	mA	
Maximum Allowable Output Current Sourced by any I/O Pin		20 mA		

1. Applies to all pins except where otherwise noted. Maximum current into or out of pin must be ±600 µA.
2. Device pin is not at an output Low state.
3. There is no input protection diode from pin to V_{DD}.
4. This excludes XTAL1 and XTAL2.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin See Figure 7.

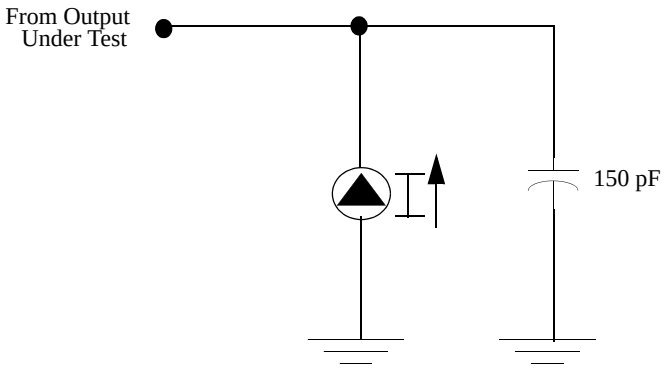

Figure 7. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = OV, f = 1.0 MHz, unmeasured pins returned to GND. See Table 7.

Table 7. Capacitance

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC Electrical Characteristics

Standard Temperature Range

Table 8 provides Direct Current characteristics for the Z86E02 SL1925 microcontroller, at a standard ambient temperature range of 0°C to 70°C.

Table 8. DC Characteristics, Standard Temperature Range

TA = 0°C to +70°C							
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1] Units**	**Conditions**	**Notes**
V_{INMAX}	Max Input Voltage	3.5V	-12	12	V	I_{IN} < 250 µA	2
		5.5V	-12	12	V	I_{IN} < 250 µA	2

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			TA = -40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{ALH}	Auto Latch High Current	4.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	9

1. Typical values are read at a V_{CC} of 5.0V
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not Low EMI mode).
4. These values apply while operating in RUN mode or HALT mode
5. These values apply while operating in STOP mode
6. All outputs are unloaded and all inputs are at the V_{CC}or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the XTAL1 pin to the V_{CC} pin.
9. Auto latches are enabled.
10. Low EMI Mode (not Standard Mode)

Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	100		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	100		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	3.5V	4	36	ms	
			5.5V	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

STANDARD Mode at Extended Temperature

Table 11 describes timing characteristics in STANDARD mode at extended temperature for the timing diagram noted in Figure 8.

Table 11. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = -40°C to +105°C				
				8MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	125	DC	ns	1
			5.5V	125	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25	ns	1
			5.5V		25	ns	1
3	T_WC	Input Clock Width	4.5V		62	ns	1
			5.5V		62	ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	4.5V	70		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	4.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	4.5V	5		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	4.5V	1	20	ms	
			5.5V	1	20	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Standard Temperature

Table 12 describes timing characteristics in LOW EMI mode at standard temperature for the timing diagram noted in Figure 8.

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = 0°C to +70°C						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	3.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	3TpC		3TpC			1,2
			5.5V	3TpC		3TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		10		ms	
			5.5V	5		5		ms	

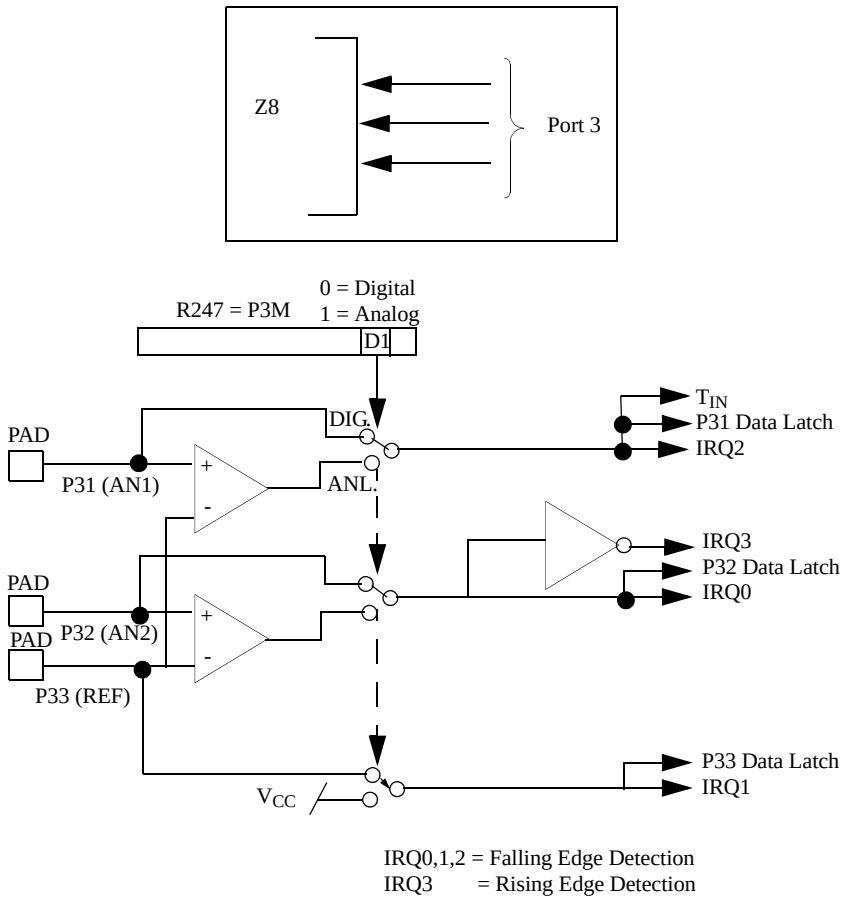

Figure 11. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, AID conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt gener-

ation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

The comparator requires two NOPs to be stable after setting the enable bit. ZiLOG recommends that interrupts IRQ0, IRQ1, and IRQ2 be disabled before setting the enable bit. After enabling the comparator, IRQ0, IRQ1, and IRQ2 should be cleared prior to re-enabling the interrupts. ZiLOG also recommends clearing these interrupts when disabling the comparator.

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX      Push RP
                LD RP, #0Fh
                LD R0, #0FFh
                POP RP
```

Program Memory

The Z86E02 SL1925 addresses up to 512B of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–511 are on-chip one-time programmable EPROM.

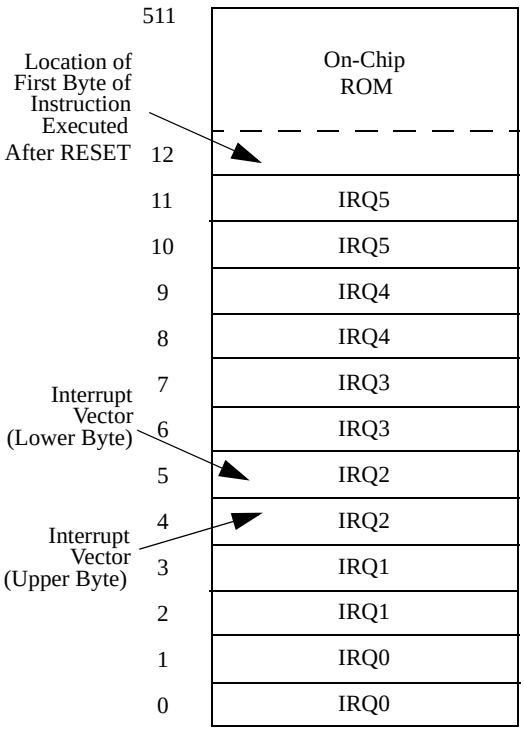

Figure 13. Program Memory Map

Register File

The Register File consists of three I/O port registers, 61 general-purpose registers, and 14 control and status registers R0, R2-R3, R4–R63, R254 and R241–R253, and R255, respectively (Figure 14). General-purpose registers occupy the 04h to 3Fh address space. I/O ports are mapped as per the existing CMOS Z8.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8® interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

Note: The rising edge interrupt is not supported. on the CCP emulator (a hardware/software work around must be employed).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX      Push RP
                LD RP, #0Fh
                LD R0, #0FFh
                POP RP
```

Table 15. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1 (P31)	4,5	External (F) Edge
IRQ3	AN2 (P32)	6,7	External (R) Edge
IRQ4	Software	8,9	Internal
IRQ5	T1	10,11	Internal
Note: Note: F = Falling edge triggered: R = Rising edge triggered			

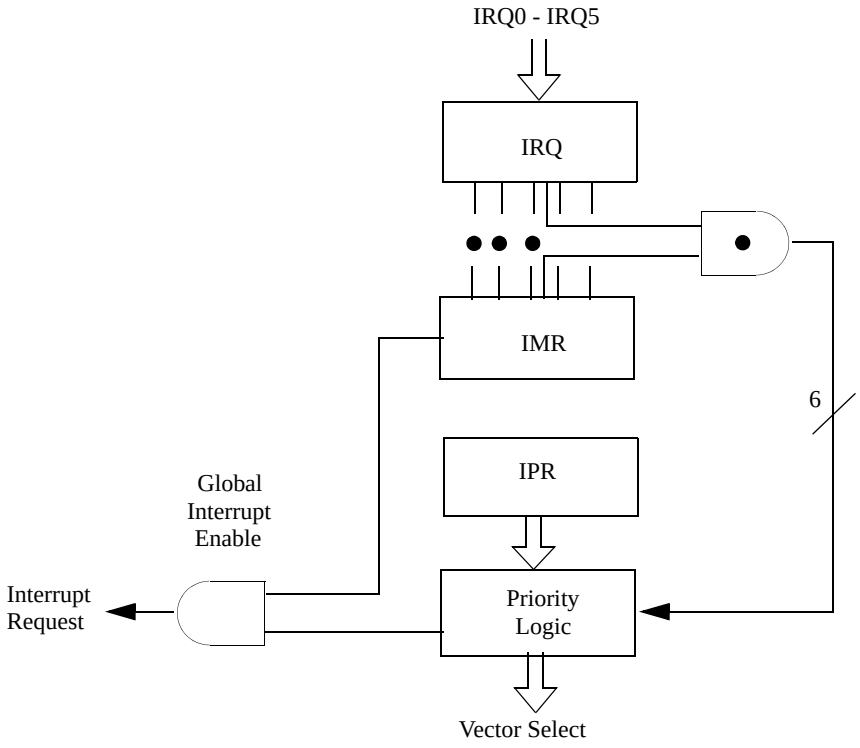

Figure 17. Interrupt Block Diagram

Table 16. Typical Frequency (MHz) vs. RC Values V_{CC} = 5.0 V @ 25°C (Continued)

	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
Resistor (R)	A	B	A	B	A	B	A	B
5 KΩ	7.6	1.6	3.6	1.0	2.3	0.7	0.28	0.14
2 KΩ	12.5	2.3	8.5	1.7	4.1	1.3	0.66	0.27
1 KΩ	17	3.1	13	2.5	9.5	1.8	1.2	0.42

1. A = Standard mode frequency
2. B = Low EMI mode frequency

HALT Mode

This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

Note: The device can be recovered by a WDT timeout. The WDT reset in HALT Mode generates a full reset similar to the Normal run mode (not STOP Mode).

STOP Mode

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 A. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A LOW INPUT condition on P27 releases the STOP mode. Program execution begins at location 000C (Hex). Refer to the Watch Dog Timer (WDT) section for information relating to WDT wakeup out of Stop Mode. However, when P27 is used to release STOP mode, the I/O port mode registers are not reconfigured to their default POWER-ON conditions. Thus the I/O, configured as output when the STOP instruction was executed, is prevented from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Note: X = Dependent on user's application.

Op Code WDT (5Fh)

The first time Op Code 5Fh is executed, the WDT is enabled; subsequent execution clears the WDT counter. This clearing of the counter must be performed at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 crystal clock cycles. The software enabled WDT does not run in STOP mode.

On the CCP emulator, a software workaround must be used to emulate the software WDT. This workaround follows.

```
SWFIXSWDT:    PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Op Code WDH (4Fh)

When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters – it just makes it possible to operate the WDT during HALT mode. A WDH instruction executed without executing WDT (5Fh) yields no effect.

Note: On the CCP emulator, a software workaround must be used to enable the software in HALT Mode/STOP Mode or hardware-enabled WDT. This workaround follows.

Software Work Around on the Z86CCP01ZEM Emulator to Emulate the Software WDT Running in HALT Mode

```
SWFIXSWDT:    PUSH RP
              LD RP, #0Fh
              LD R15,#00000101B
              POP RP
```

Permanent WDT

Selecting the hardware-enabled Permanent WDT option bit automatically enables the WDT upon exiting reset. The permanent WDT always runs in HALT mode and STOP mode, and it cannot be disabled.

Table 19. Prescaler 1 Register, R243 PRE1 F3h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-2	Prescaler	W	X	**Prescaler Modulo** Range = 1-64 decimal; 01h-00h
1	Clock	W	0	**Clock Source** 0: T1 External Timing Input (T_{IN}) Mode 1: Internal
0	Count	W	0	**TI Count Mode** 0: Single Pass 1: Modulo N

Table 20. Port 2 Mode Register, R246 P2M F6h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1
Note: W = Write,								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	P20-P27	W	1	**P20-P27 I/O Definition** 0: Defines bit as Output 1: Defines bit as Input

Table 21. Port 3 Mode Register, R247 P3M F7h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-2	Reserved	W	X	Reserved-must be 0
1	Port 3	W	0	**Port 3 Outputs** 0: DIGITAL Mode 1: ANALOG Mode
0	Port 2	W	0	**Port 2 Outputs** 0: Open-Drain 1: Push-Pull

Table 22. Port 0 and 1 Mode Register, R248 P01 F8h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	X	1	0	1
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-5, 3	Reserved	W	X	Reserved-must be 0
4	Reserved	W	0	Reserved-must be 0
2	Reserved	W	X	Reserved-must be 1
1-0	P02-P00	W	01	**P02-P00 Mode** 0: Output 1: Input

Table 23. Interrupt Priority Register, R249 IPR F9h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X

Note: W = Write, X = Indeterminate

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	W	X	Reserved-must be 0
5	IRQ3, IRQ5	W	X	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3 1: IRQ3 < IRQ5
4, 3, 0	Interrupt	W	X	**Interrupt Group Priority** 000: Reserved* 001: C>A>B 010: A>B>C 011: A>C>B 100: B>C>A 101: C>B>A 110: B>A>C 111: Reserved
2	IRQ0, IRQ2	W	X	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0 1: IRQ0 < IRQ2
1	IRQ1, IRQ4	W	X	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4 1: IRQ4 < IRQ1

Note: *Selecting a Reserved mode causes an undefined operation.

Table 29. Stack Pointer Low, R255 SPL FFh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W= Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	Stack	R/W	0	Stack Pointer Lower Byte (SP0-SP7)

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Part Number Description

ZiLOG part numbers consist of a number of components. For example, part number Z86E0208PSC1925 is a 8-MHz 18-pin DIP that operates in the -0°C to +70°C temperature range, with Plastic Standard Flow. The Z86E0208PSC1925 part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
E	OTP Product
02	Product Number
08	Speed (MHz)
P	Dual In-line Processor
S	Standard Temperature
C	Environmental Flow

Document Information

Document Number Description

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0148	Unique Document Number
02	Revision Number
0903	Month and Year Published