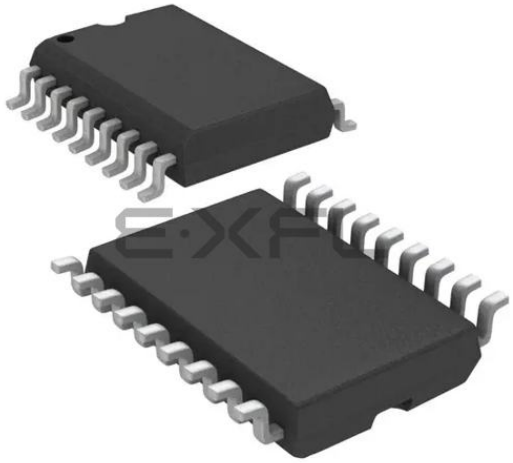

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0208seg1925

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Architectural Overview

ZiLOG's Z86E02 SL1925 Microcontroller (MCU) is a One-Time Programmable (OTP) member of ZiLOG's single-chip Z8® MCU family that allows easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E02 SL1925's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O. One on-chip counter/timer, with a large number of user-selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Z86E02 SL1925 Features

Table 1. Z86E02 SL1925 Features

Device	OTP (KB)	RAM* (Bytes)	Speed (MHz)
Z86E02 SL1925	0.5	61	8

Note: *General-Purpose.

- 3.5V to 5.5V Operating Range @ 0°C to +70°C
- 4.5V to 5.5V Operating Range @ -40°C to +105°C
- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 1 timer, 1 software)
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - RC Oscillator
- One Programmable 8-Bit Counter/Timer, with 6-bit Programmable Prescaler
- WDT/Power-On Reset (POR)
- On-Chip Oscillator that accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset

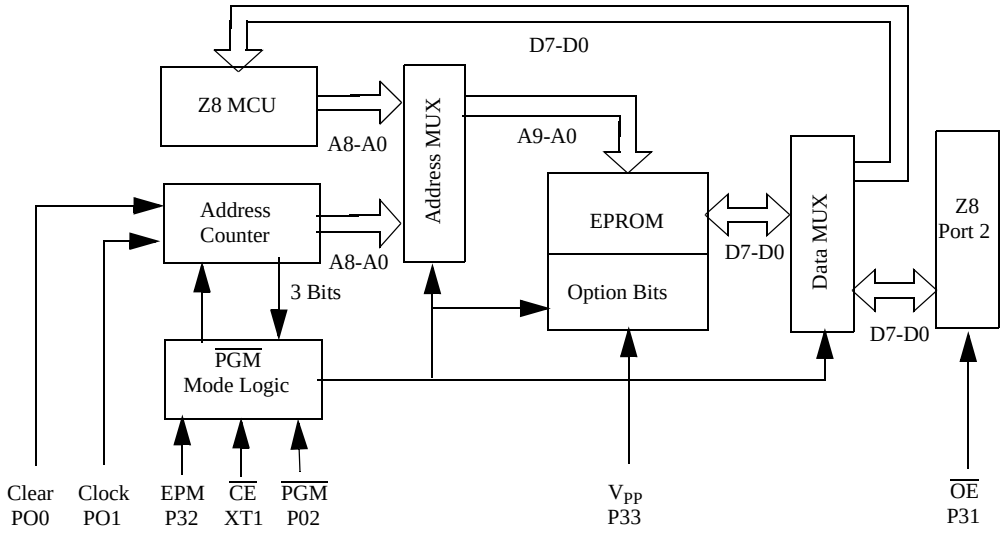


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

Pin diagrams and identification for the device are displayed in Figure 3 through Figure 6, and in Table 2 through Table 5.

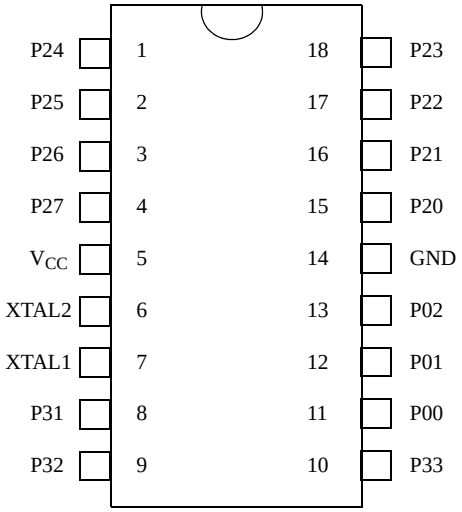


Figure 3. 18-Pin DIP/SOIC Configuration, STANDARD Mode

Table 2. 18-Pin DIP/SOIC Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4-7	Input/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1 AN1	Input
9	P32	Port 3, Pin 1 AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0-2	Input/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0-3	Input/Output

Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	100		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	100		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	3.5V	4	36	ms	
			5.5V	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Standard Temperature

Table 12 describes timing characteristics in LOW EMI mode at standard temperature for the timing diagram noted in Figure 8.

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = 0°C to +70°C						
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	3.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	3.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	3TpC		3TpC			1,2
			5.5V	3TpC		3TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		10		ms	
			5.5V	5		5		ms	

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature (Continued)

				TA = 0°C to +70°					
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	T_{POR}	Power-On Reset Time	3.5V	2	18	2	18	ms	
			5.5V	2	18	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Extended Temperature

Table 13 describes timing characteristics in LOW EMI mode at extended temperature for the timing diagram noted in Figure 8.

Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature

				TA = 0°C to +70°C					
				1MHz		4MHz			
No	Symbol	Parameter	Vcc	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1

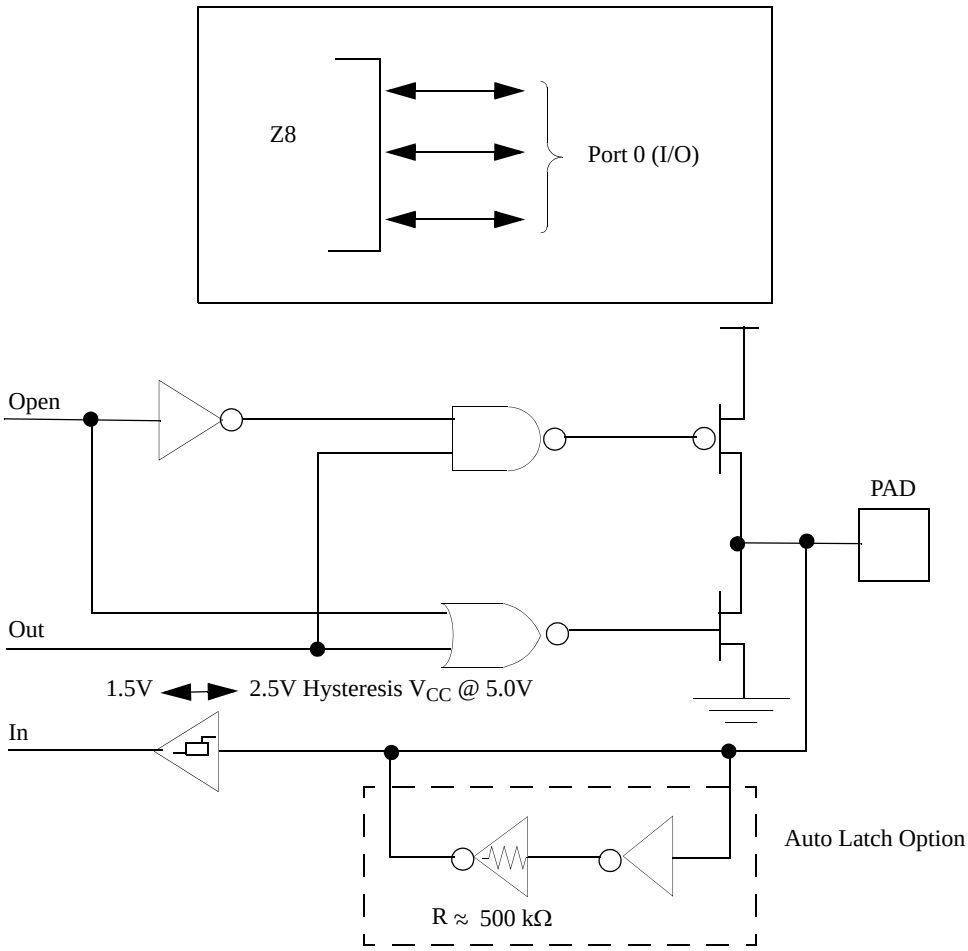


Figure 9. Port 0 Configuration

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 10).

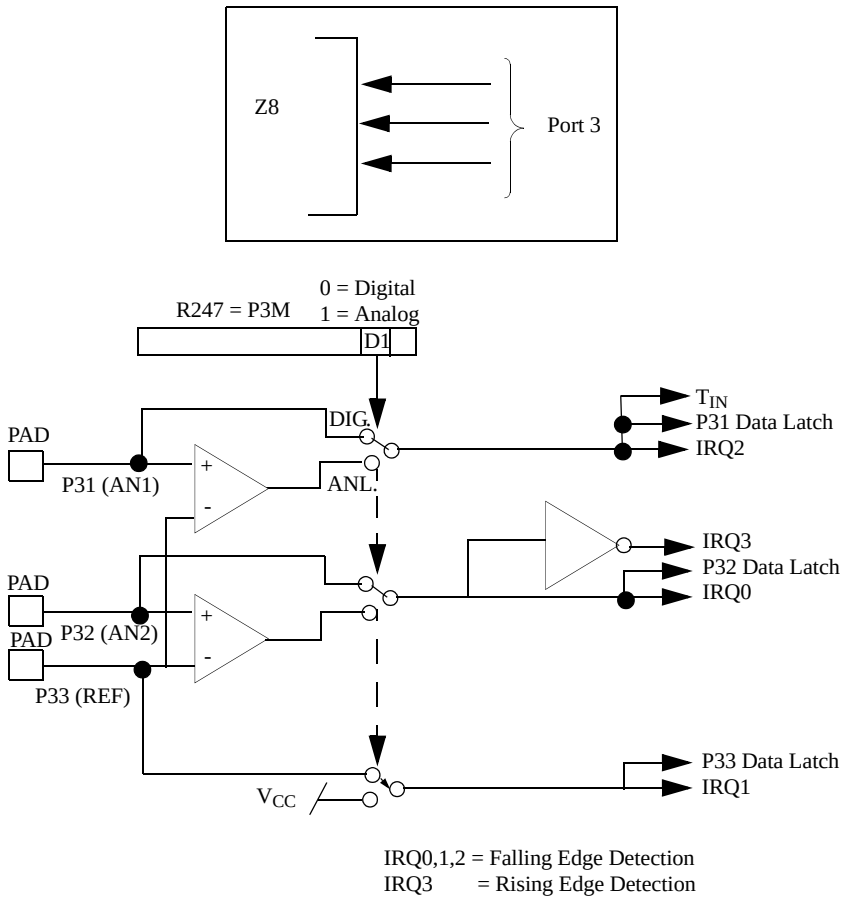


Figure 11. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, AID conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt gener-

Table 14. Z8® Control Registers Reset Values*

		Reset Condition								
Address	**Register**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**Dl**	**D0**	**Comments**
FFh	SPL	0	0	0	0	0	0	0	0	
FDh	RP	0	0	0	0	0	0	0	0	
FCh	FLAGS	U	U	U	U	U	U	U	U	
FBh	IMR	0	U	U	U	U	U	U	U	
FAh	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9h	IPR	U	U	U	U	U	U	U	U	
F8h*	P01M	U	U	U	0	U	1	0	1	
F7h*	P3M	U	U	U	0	U	U	0	0	
F6h*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F3h	PRE1	U	U	U	0	U	U	0	0	
F2h	T1	U	U	U	0	U	U	U	U	
F1h	TMR	0	0	0	0	0	0	0	0	

Note: Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset causes these control registers to be reconfigured as indicated in Table 14 and the user must avoid bus contention on the port pins or it may affect device reliability

A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out (in Halt mode)

Watch-Dog Timer Reset

The WDT is a retriggerable one-shot timer that resets the Z8® if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Program Memory

The Z86E02 SL1925 addresses up to 512B of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–511 are on-chip one-time programmable EPROM.

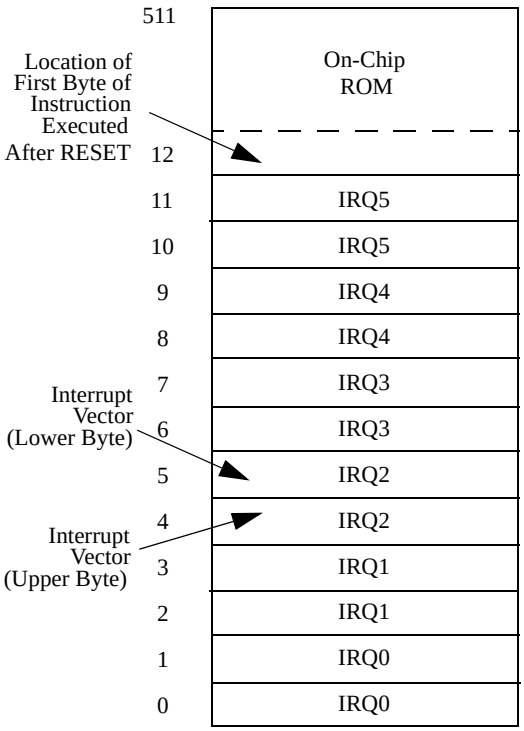


Figure 13. Program Memory Map

Register File

The Register File consists of three I/O port registers, 61 general-purpose registers, and 14 control and status registers R0, R2-R3, R4–R63, R254 and R241–R253, and R255, respectively (Figure 14). General-purpose registers occupy the 04h to 3Fh address space. I/O ports are mapped as per the existing CMOS Z8.

Counter/Timer

There is one 8-bit programmable counter/timer (T1), driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources (Figure 16).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO-N CONTINUOUS mode).

The counter, but not the prescaler, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The TIMER mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

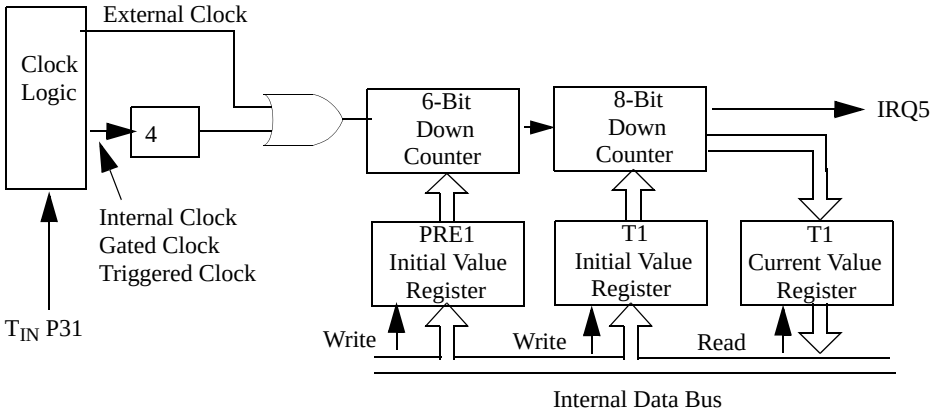


Figure 16. Counter/Timer Block Diagram

Interrupts

The Z8® features six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 17). The sources are divided as follows: the falling edge of P31 (AN 1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), by software, and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Interrupt Types, Sources, and Vectors).

Table 15. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F) Edge
IRQ1	REF(P33)	2,3	External (F) Edge
IRQ2	AN1 (P31)	4,5	External (F) Edge
IRQ3	AN2 (P32)	6,7	External (R) Edge
IRQ4	Software	8,9	Internal
IRQ5	T1	10,11	Internal
Note: Note: F = Falling edge triggered: R = Rising edge triggered			

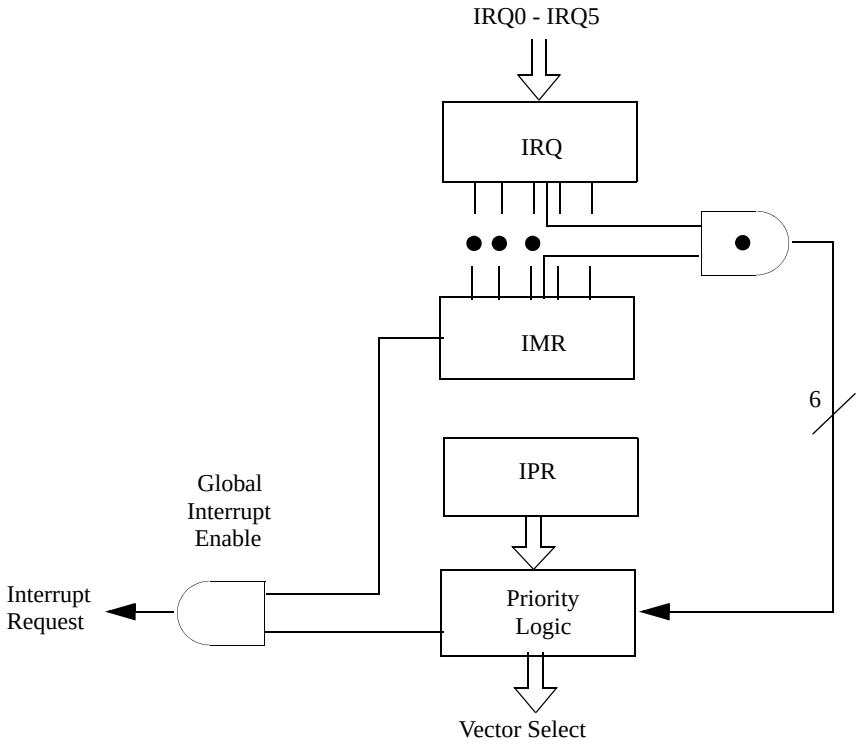


Figure 17. Interrupt Block Diagram

Clock

The Z8® on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to an external crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, up to 8 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's crystal recommended capacitor values from each pin directly to device ground pin 14 on DIP and SOIC packages or pins 5 and 6 on SSOP package (Figure 18).

Note: The crystal capacitor loads should be connected directly to the Z8® GND pin to reduce Ground noise injection. They should not connect to system Ground.

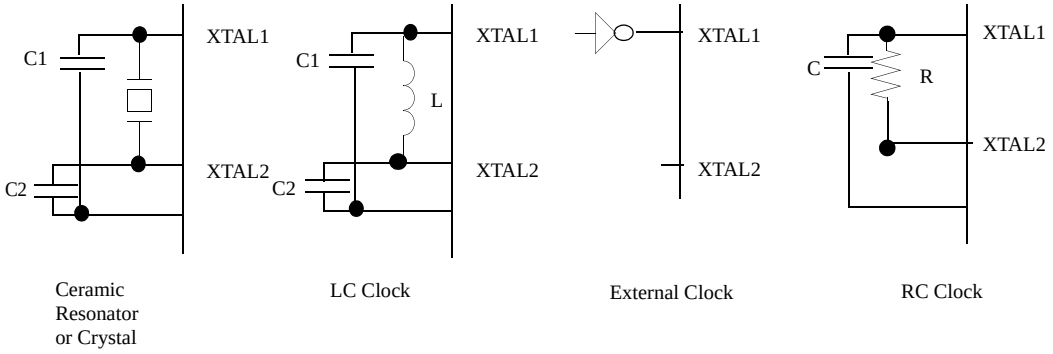


Figure 18. Oscillator Configuration

Table 16. Typical Frequency (MHz) vs. RC Values V_{CC} = 5.0 V @ 25°C

	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
Resistor (R)	A	B	A	B	A	B	A	B
1.0 MΩ	0.05	0.03	0.03	0.02	0.02	0.01	0.001	0.001
560 KΩ	0.09	0.04	0.05	0.025	0.03	0.02	0.003	0.002
220 KΩ	0.23	0.11	0.12	0.07	0.07	0.043	0.007	0.005
100 KΩ	0.5	0.19	0.28	0.13	0.15	0.086	0.014	0.01
56 KΩ	0.93	0.28	0.48	0.2	0.27	0.13	0.026	0.02
20 KΩ	2.2	0.57	1.1	0.41	0.71	0.28	0.07	0.05
10 KΩ	3.5	1.0	2.1	0.64	1.4	0.45	0.14	0.08

Note: Any Low level detected on pin P27 takes the device out of STOP mode, even if it is configured as an output. It is not edge triggered.

To enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate SLEEP instruction, such as:

```
FFh     NOP     ; clear the pipeline
6Fh     STOP    ; enter STOP mode
        or
FFH     NOP     ; clear the pipeline
7Fh     HALT    ; enter HALT mode
```

Note: On the CCP emulator, a software workaround must be used to enable P27 as the Stop-Mode Recovery source. This workaround follows.

Software Work Around on the Z86CCP01ZEM Emulator to Enable P27 as Stop-Mode Recovery Source

```
SWFIXP27:   PUSH RP
            LD RP, #0Fh
            LD R012, #001101X0B     X= 1 for LOW EMI Mode
                                    X= 0 for STANDARD Mode
            POP RP
```

Watch-Dog Timer (WDT)

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 T_{WDT} period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z = 1, S = 0, V = 0.

WDT = 5Fh

Control Registers

Table 17. Timer Mode Register, R241 TMR F1h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	R/W	00	Reserved-must be 0
5-4	T_{IN} Mode	R/W	0	**T_{IN} Mode** 00: External Clock Input 01: Gate Input 10: Trigger Input (non retriggerable) 11: Trigger Input (retriggerable)
3	T1 Count	R/W	0	**TI Count** 0: Disable 1: Enable
2	T1	R/W	0	**TI** 0: No Function 1: Load T1
1-0	Reserved	R/W	0	Reserved - must be 0

Table 18. Counter/Timer 1 Register, R242 T1 F2h Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
Note: R = Read, W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	T1	R	X	**T1 Current Value**
		W	X	**T1 Initial Value** Range = 1-256 decimal; 01h-00h

Table 24. Interrupt Request Register, R250 IPR FAh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write								

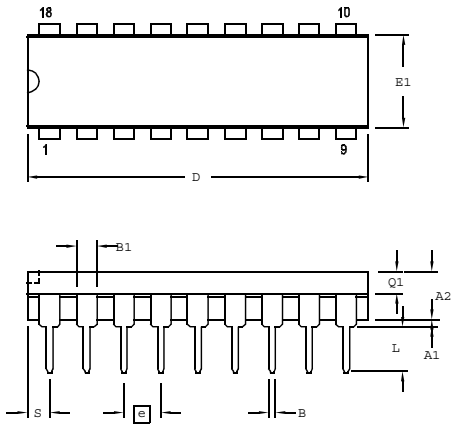
Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	R/W	00	Reserved-must be 0
5	IRQ5	R/W	0	**Interrupt** IRQ5 = T1 0: No interrupt pending 1: Interrupt pending
4	IRQ4	R/W	**0**	**Interrupt** RQ4 = Software generated 0: No interrupt pending 1: Interrupt pending
3	IRQ3	R/W	**0**	**Interrupt** RQ3 = P32 Input (rising edge) 0: No interrupt pending 1: Interrupt pending
2	IRQ2	R/W	**0**	**Interrupt** RQ2 = P31 Input 0: No interrupt pending 1: Interrupt pending
1	IRQ1,	R/W	**0**	**Interrupt** RQ1 = P33 Input 0: No interrupt pending 1: Interrupt pending
0	IRQ0	R/W	**0**	**Interrupt** RQ0 = P32 Input 0: No interrupt pending 1: Interrupt pending
Note: *Selecting a Reserved mode causes an undefined operation.				

Table 29. Stack Pointer Low, R255 SPL FFh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W= Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-0	Stack	R/W	0	Stack Pointer Lower Byte (SP0-SP7)

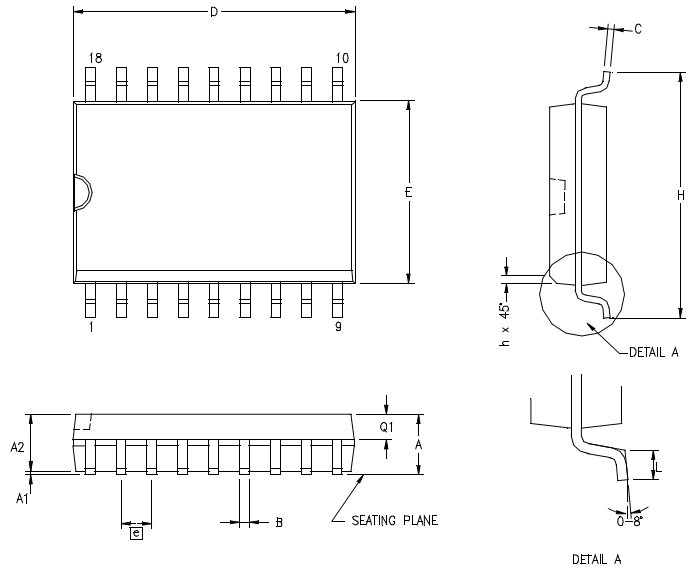
Package Information



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 BSC		.100 BSC	
eA	7.87	9.40	.310	0.370
L	3.18	3.81	.125	.150
Q1	1.47	1.65	.058	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 20. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 21. 18-Pin SOIC Package Diagram