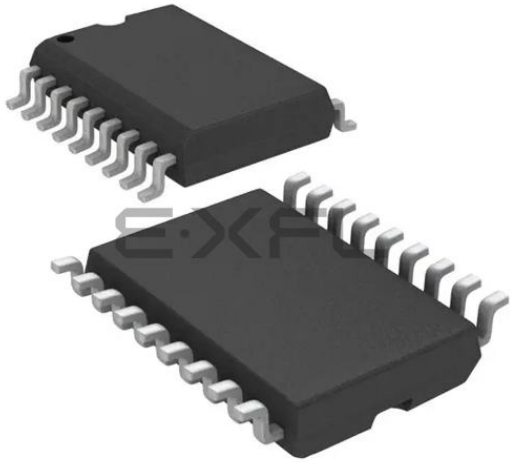

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	61 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0208ssc1925

Architectural Overview

ZiLOG's Z86E02 SL1925 Microcontroller (MCU) is a One-Time Programmable (OTP) member of ZiLOG's single-chip Z8® MCU family that allows easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E02 SL1925's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O. One on-chip counter/timer, with a large number of user-selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Z86E02 SL1925 Features

Table 1. Z86E02 SL1925 Features

Device	OTP (KB)	RAM* (Bytes)	Speed (MHz)
Z86E02 SL1925	0.5	61	8

Note: *General-Purpose.

- 3.5V to 5.5V Operating Range @ 0°C to +70°C
- 4.5V to 5.5V Operating Range @ -40°C to +105°C
- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 1 timer, 1 software)
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - RC Oscillator
- One Programmable 8-Bit Counter/Timer, with 6-bit Programmable Prescaler
- WDT/Power-On Reset (POR)
- On-Chip Oscillator that accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset

- Low-Power Consumption (50 mΩ typical)
- Fast Instruction Pointer (1.5µs @ 8 MHz)
- RAM Bytes (61)

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

BLOCK DIAGRAMS

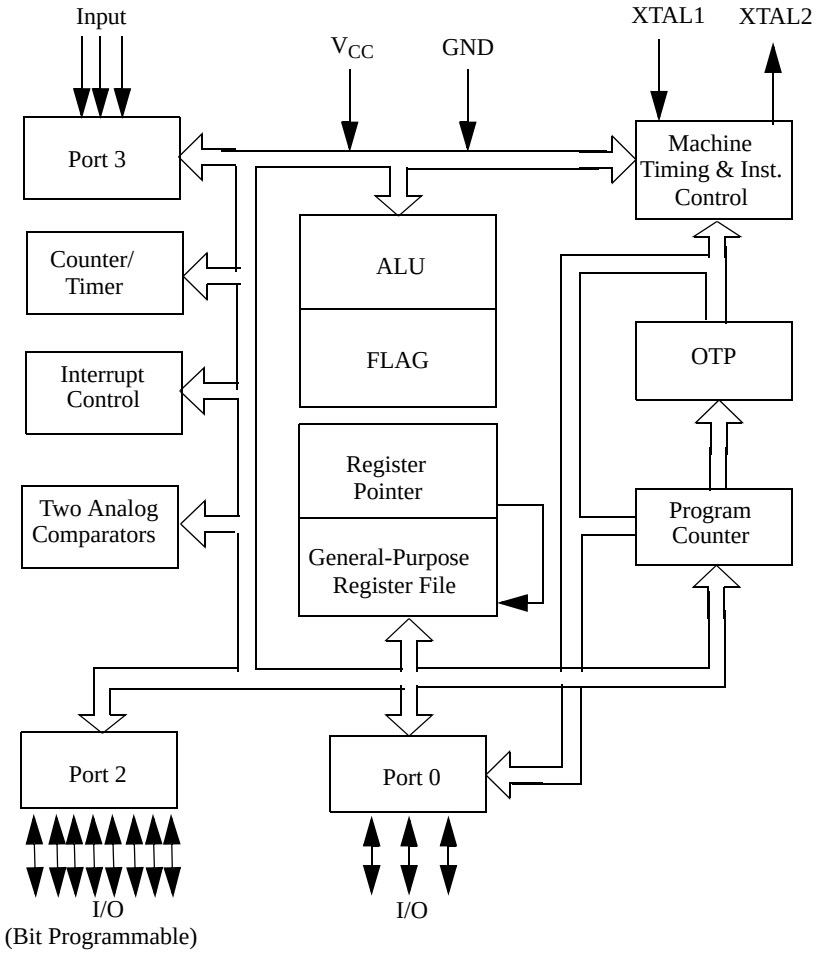

Figure 1. Functional Block Diagram

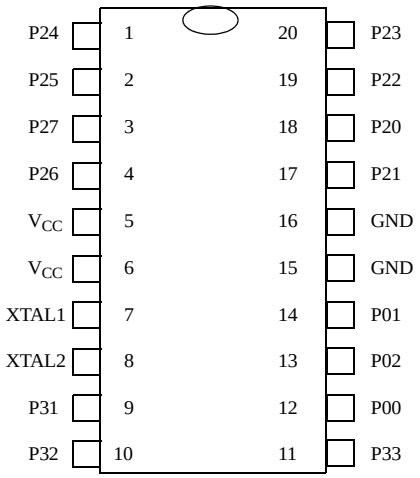

Figure 5. 20-Pin SSOP Pin Configuration, STANDARD Mode

Table 4. 20-Pin SSOP Pin Identification, STANDARD Mode

Pin #	Symbol	Function	Direction
1,2	P24-P25	Port 2, Pins 4-5	Input/Output
3	P27	Port 2, Pin 7	Input/Output
4	P26	Port 2, Pin 6	Input/Output
5	V_{CC}	Power Supply	
6	V_{CC}	Power Supply	
7	XTAL1	Crystal Oscillator Clock	Input
8	XTAL2	Crystal Oscillator Clock	Output
9	P31	Port 3, Pin 1, AN1	Input
10	P32	Port 3, Pin 2, AN2	Input
11	P33	Port 3, Pin 3, REF	Input
12	P00	Port 0, Pin 0	Input/Output
13	P02	Port 0, Pin 1	Input/Output
14	P01	Port 0, Pin 1	Input/Output
15	GND	Ground	
16	GND	Ground	
17	P21	Port 2, Pin 1	Input/Output
18	P20	Port 2, Pin 0	Input/Output
19-20	P22-P23	Port 2, Pins 2-3	Input/Output

Table 8. DC Characteristics, Standard Temperature Range (Continued)

TA = 0°C to +70°C								
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	3.5V	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}-0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}-0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}-0.3	0.2 V_{CC}	0.8	V		
		5.5V	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}-0.4		3.3	V	I_{OH} = -2.0 mA	3
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	3
		3.5V	V_{CC}-0.4		3.3	V	I_{OH} = -0.5 mA	10
		5.5V	V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	10
V_{OL1}	Output Low Voltage	3.5V		0.8	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	3
		3.5V		0.4	0.2	V	I_{OL}=1.0mA	10
		5.5V		0.4	0.1	V	I_{OL}=1.0mA	10
V_{OL2}	Output Low Voltage	3.5V		1.2	1.0	V	I_{OL} = +12 mA	3
		5.5V		1.2	0.8	V	I_{OL} = +12 mA	3
V_{LV}	V_{CC} Low Voltage Auto Reset		2.6	3.2	2.9	V	@ 4MHz Maximum Internal Clock Frequency	4
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}	

Table 8. DC Characteristics, Standard Temperature Range (Continued)

TA = 0°C to +70°C								
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1] Units**		**Conditions**	**Notes**
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} - 1.0		V		
I_{CC}	Supply Current	3.5V	3.5		1.5	mA	@ 2 MHz	3,6
		5.5V	7.0		6.8	mA	@ 2 MHz	3,6
		3.5V	8.0		3.0	mA	@ 8 MH	3,6
		5.5V	11.0		8.2	mA	@ 8 MHz	3,6
I_{CC1}	Standby Current (HALT Mode)	3.5V	2.5		0.7	mA	@ 2 MHz	3,6
		5.5V	4.0		2.5	mA	@ 2 MHz	3,6
		3.5V	4.0		1.0	mA	@ 8 MHz	3,6
		5.5V	5.0		3.0	mA	@ 8 MHz	3,6
I_{CC}	Supply Current (HALT and Low EMI Mode)	3.5V	3.5		1.5	mA	@ 1 MHz	6,10
		5.5V	7.0		6.8	mA	@ 1 MHz	6,10
		3.5V	5.8		2.5	mA	@ 2 MHz	6,10
		5.5V	9.0		7.5	mA	@ 2 MHz	6,10
		3.5V	8.0		3.0	mA	@ 4 MHz	6,10
		5.5V	11.0		8.2	mA	@ 4 MHz	6,10
I_{CC1}	Standby Current (Low EMI Mode)	3.5V	1.2		0.4	mA	@ 1 MHz	6,10
		5.5V	1.6		0.9	mA	@ 1 MHz	6,10
		3.5V	1.5		0.5	mA	@ 2 MHz	6,10
		5.5V	1.9		1.0	mA	@ 2 MHz	6,10
		3.5V	2.0		0.8	mA	@ 4 MHz	6,10
		5.5V	2.4		3.0	mA	@ 4 MHz	6,10
I_{CC2}	Standby Current (STOP Mode)	3.5V	10.0		1.0	µA	WDT is not Running	6,7,8
		5.5V	10.0		1.0	µA	WDT is not Running	6,7,8
I_{ALL}	Auto Latch Low Current	3.5V	12.0		3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	32.0		16	µA	$0V < V_{IN} < V_{CC}$	9

Table 9. DC Characteristics, Extended Temperature Range (Continued)

			TA = -40°C to +105°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Typical @ 25°C[1]**	**Units**	**Conditions**	**Notes**
I_{ALH}	Auto Latch High Current	4.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	9

1. Typical values are read at a V_{CC} of 5.0V
2. Port 2, Port 3, and Port 0 only.
3. STANDARD mode (not Low EMI mode).
4. These values apply while operating in RUN mode or HALT mode
5. These values apply while operating in STOP mode
6. All outputs are unloaded and all inputs are at the V_{CC}or V_{SS} level.
7. If the analog comparator is selected, then the comparator inputs must be at the V_{CC} level.
8. A 10-MΩ pull-up resistor is required in the circuit between the XTAL1 pin to the V_{CC} pin.
9. Auto latches are enabled.
10. Low EMI Mode (not Standard Mode)

Table 10. AC Electrical Characteristics, Standard Mode and Temperature (Continued)

			TA = 0°C to +70°C				
			8MHz				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
4	$T_WT_{IN}L$	Timer Input Low Width	3.5V	100		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	3.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	3.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	3.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	3.5V	100		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	3.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	3.5V	10		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	3.5V	4	36	ms	
			5.5V	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

STANDARD Mode at Extended Temperature

Table 11 describes timing characteristics in STANDARD mode at extended temperature for the timing diagram noted in Figure 8.

Table 11. AC Electrical Timing, Standard Mode at Extended Temperature

			TA = -40°C to +105°C				
				8MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	125	DC	ns	1
			5.5V	125	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25	ns	1
			5.5V		25	ns	1
3	T_WC	Input Clock Width	4.5V		62	ns	1
			5.5V		62	ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		ns	1
			5.5V	70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	5TpC			1
			5.5V	5TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	8TpC			1
			5.5V	8TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100	ns	1
			5.5V		100	ns	1
8	T_WIL	Interrupt Request Input Low Time	4.5V	70		ns	1,2
			5.5V	70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	4.5V	5TpC			1,2
			5.5V	5TpC			1,2
10	T_{WDT}	Watch-Dog Timer Delay Time before Time-out	4.5V	5		ms	
			5.5V	5		ms	
11	T_{POR}	Power-On Reset Time	4.5V	1	20	ms	
			5.5V	1	20	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

Table 12. AC Electrical Timing, Standard Mode at Extended Temperature (Continued)

				TA = 0°C to +70°					
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
11	T_{POR}	Power-On Reset Time	3.5V	2	18	2	18	ms	
			5.5V	2	18	2	18	ms	

1. Timing reference is 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0
2. Interrupt request through Port 3 (P33-P31)

LOW EMI Mode at Extended Temperature

Table 13 describes timing characteristics in LOW EMI mode at extended temperature for the timing diagram noted in Figure 8.

Table 13. AC Electrical Timing, Low EMI Mode at Extended Temperature

				TA = 0°C to +70°C					
				1MHz		4MHz			
No	Symbol	Parameter	Vcc	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	T_RC,T_FC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	T_WC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	3TpC		3TpC			1
			5.5V	3TpC		3TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	T_RT_{IN}, T_TT_{IN}	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option prevents accidental entry into EPROM Mode or Test Mode.

STANDARD Mode

XTAL1, XTAL2. Crystal In, Crystal Out (time-based input and output, respectively). These pins connect an external parallel-resonant crystal, resonator, RC, LC, or an external single-phase clock (8 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 9).

Auto Latch. The Auto Latch places valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch sets the ports to an undetermined state of 0 or 1. The default condition is AUTO LATCH ENABLED. The Auto Latch can be disabled by programming the AUTO LATCH DISABLE option bit.

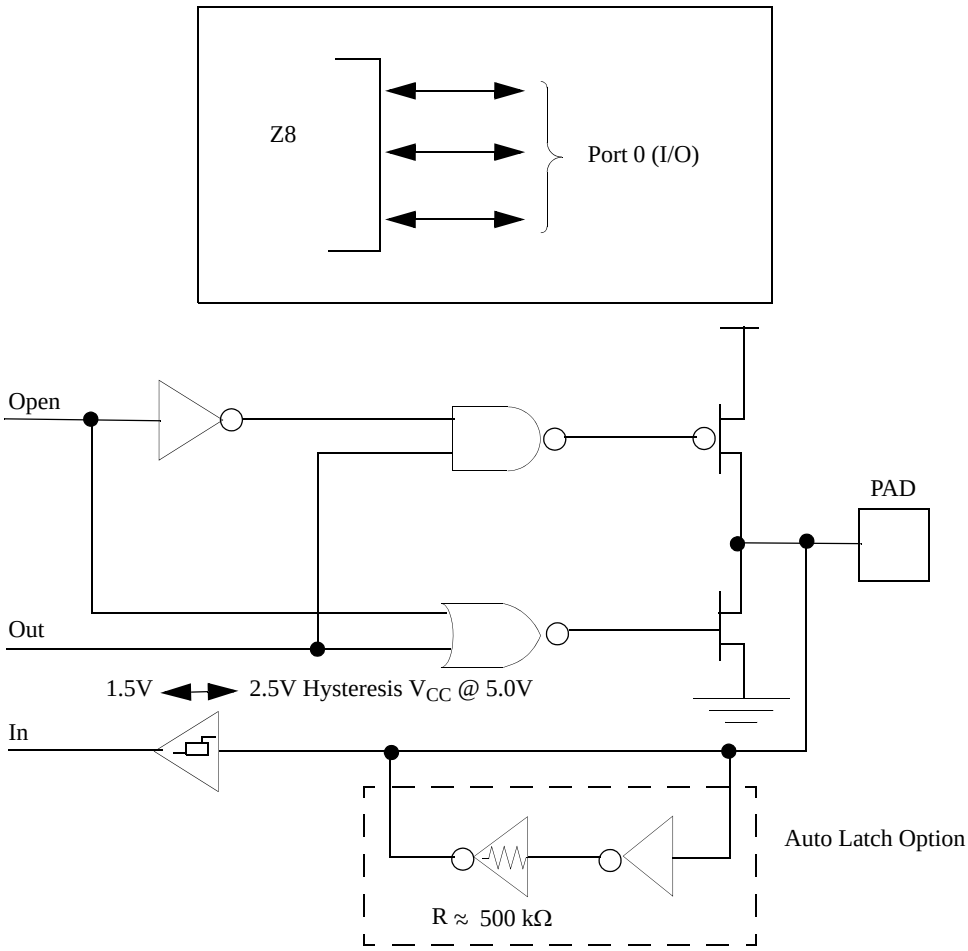

Figure 9. Port 0 Configuration

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 10).

Program Memory

The Z86E02 SL1925 addresses up to 512B of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–511 are on-chip one-time programmable EPROM.

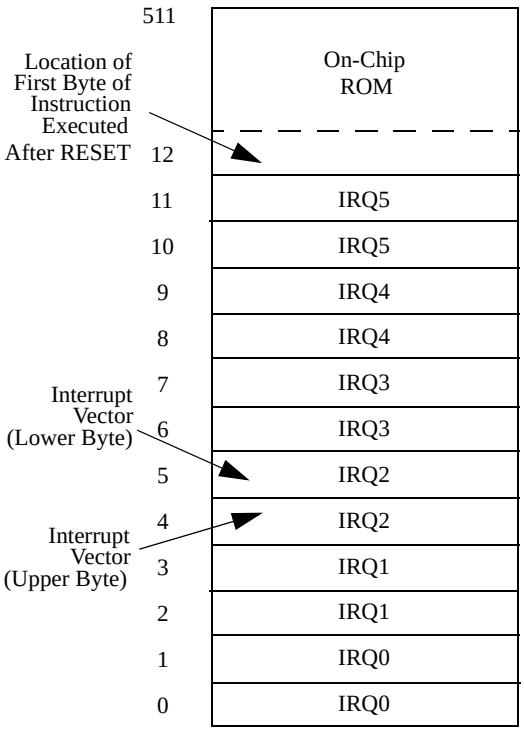

Figure 13. Program Memory Map

Register File

The Register File consists of three I/O port registers, 61 general-purpose registers, and 14 control and status registers R0, R2-R3, R4–R63, R254 and R241–R253, and R255, respectively (Figure 14). General-purpose registers occupy the 04h to 3Fh address space. I/O ports are mapped as per the existing CMOS Z8.

Location		Identifiers
255(FFh)	Stack Pointer (Bits 7-0)	SPL
254(FEh)	General-Purpose Register	GPR
253(FDh)	Register Pointer	RP
252(FCh)	Program Control Flags	Flags
251(FBh)	Interrupt Mask Register	IMR
250(FBh)	Interrupt Request Register	IRQ
249(FAh)	Interrupt Priority Register	IRP
248(F8h)	Ports 0-1 Mode	P01M
247(F7h)	Port 3 Mode	P3M
246(F6h)	Port 2 Mode	P2M
245(F5h)	Reserved	Reserved
244(F4h)	Reserved	Reserved
243(F3h)	T1 Prescaler	PRE1
242(F2h)	TimerCounter1	T1
241(F1h)	Timer Mode	TMR
240(F0h) 64(40h)	Not Implemented	
63(30h) 4(04h)	General-Purpose Registers	
3(03h)	Port 3	P3
2(02h)	Port 2	P2
1(01h)	Reserved	Reserved
0(00h)	Port 0	P0

Figure 14. Register File

The Z8® instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing short 4-bit register addressing mode using the Register Pointer.

In the 4-bit address mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 15) addresses the starting location of the active working-register group.

Counter/Timer

There is one 8-bit programmable counter/timer (T1), driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources (Figure 16).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (SINGLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO-N CONTINUOUS mode).

The counter, but not the prescaler, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The TIMER mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

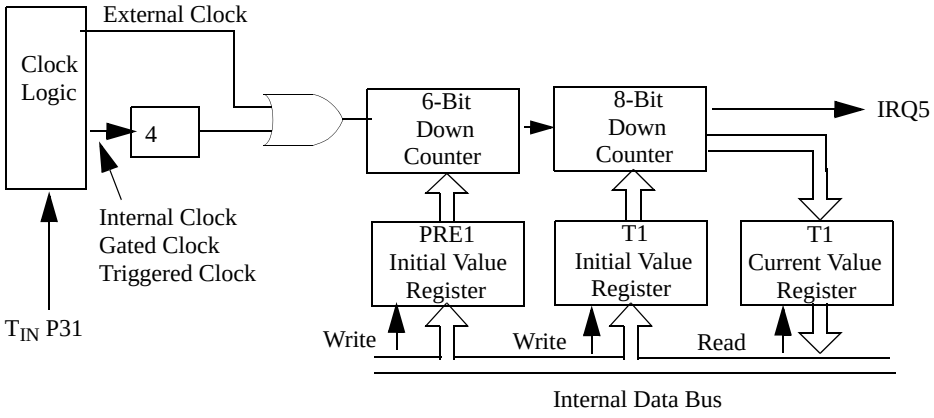

Figure 16. Counter/Timer Block Diagram

Interrupts

The Z8® features six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 17). The sources are divided as follows: the falling edge of P31 (AN 1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), by software, and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Interrupt Types, Sources, and Vectors).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8® interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted, thus disabling all subsequent interrupts, saving the Program Counter and Status Flags, and then branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests requires service.

Note: The rising edge interrupt is not supported. on the CCP emulator (a hardware/software work around must be employed).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Digital Interrupt

To emulate the P32 rising edge digital interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P3, pin 17) or (P2, pin 12) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

Hardware Work Around on the on the Z86CCP01ZEM Emulator to P32 Rising Edge Analog Interrupt

To emulate the P32 rising edge analog interrupt the emulator must be modified in the following way:

1. Connect P32 by soldering a wire jumper from either emulation socket (P2, pin 16) or (P1, pin 23) to 74HCT04 U27 pin 1.
2. Connect 74HCT04 U27 pin 2 by soldering a wire jumper from U27 pin 2 to P30 on either emulator socket (P3, pin 25) or (P2, pin 18).

The following routine must be added to the initialization of the device:

```
HSWP32AFIX      Push RP
                LD RP, #0Fh
                LD R0, #0FFh
                POP RP
```

Table 16. Typical Frequency (MHz) vs. RC Values V_{CC} = 5.0 V @ 25°C (Continued)

	Load Capacitor							
	33 pF		56 pF		100 pF		0.001 µF	
Resistor (R)	A	B	A	B	A	B	A	B
5 KΩ	7.6	1.6	3.6	1.0	2.3	0.7	0.28	0.14
2 KΩ	12.5	2.3	8.5	1.7	4.1	1.3	0.66	0.27
1 KΩ	17	3.1	13	2.5	9.5	1.8	1.2	0.42

1. A = Standard mode frequency
2. B = Low EMI mode frequency

HALT Mode

This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

Note: The device can be recovered by a WDT timeout. The WDT reset in HALT Mode generates a full reset similar to the Normal run mode (not STOP Mode).

STOP Mode

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 A. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A LOW INPUT condition on P27 releases the STOP mode. Program execution begins at location 000C (Hex). Refer to the Watch Dog Timer (WDT) section for information relating to WDT wakeup out of Stop Mode. However, when P27 is used to release STOP mode, the I/O port mode registers are not reconfigured to their default POWER-ON conditions. Thus the I/O, configured as output when the STOP instruction was executed, is prevented from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Note: X = Dependent on user's application.

Note: Any Low level detected on pin P27 takes the device out of STOP mode, even if it is configured as an output. It is not edge triggered.

To enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (Op Code = FFh) immediately before the appropriate SLEEP instruction, such as:

```
FFh     NOP     ; clear the pipeline
6Fh     STOP    ; enter STOP mode
        or
FFH     NOP     ; clear the pipeline
7Fh     HALT    ; enter HALT mode
```

Note: On the CCP emulator, a software workaround must be used to enable P27 as the Stop-Mode Recovery source. This workaround follows.

Software Work Around on the Z86CCP01ZEM Emulator to Enable P27 as Stop-Mode Recovery Source

```
SWFIXP27:   PUSH RP
            LD RP, #0Fh
            LD R012, #001101X0B     X= 1 for LOW EMI Mode
                                    X= 0 for STANDARD Mode
            POP RP
```

Watch-Dog Timer (WDT)

The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 T_{WDT} period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z = 1, S = 0, V = 0.

WDT = 5Fh

Table 21. Port 3 Mode Register, R247 P3M F7h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-2	Reserved	W	X	Reserved-must be 0
1	Port 3	W	0	**Port 3 Outputs** 0: DIGITAL Mode 1: ANALOG Mode
0	Port 2	W	0	**Port 2 Outputs** 0: Open-Drain 1: Push-Pull

Table 22. Port 0 and 1 Mode Register, R248 P01 F8h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	X	1	0	1
Note: W = Write, X = Indeterminate								

Bit Position	Bit Field	R/W	Reset Value	Description
7-5, 3	Reserved	W	X	Reserved-must be 0
4	Reserved	W	0	Reserved-must be 0
2	Reserved	W	X	Reserved-must be 1
1-0	P02-P00	W	01	**P02-P00 Mode** 0: Output 1: Input

Table 23. Interrupt Priority Register, R249 IPR F9h Bank 0h: WRITE ONLY

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X

Note: W = Write, X = Indeterminate

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	W	X	Reserved-must be 0
5	IRQ3, IRQ5	W	X	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3 1: IRQ3 < IRQ5
4, 3, 0	Interrupt	W	X	**Interrupt Group Priority** 000: Reserved* 001: C>A>B 010: A>B>C 011: A>C>B 100: B>C>A 101: C>B>A 110: B>A>C 111: Reserved
2	IRQ0, IRQ2	W	X	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0 1: IRQ0 < IRQ2
1	IRQ1, IRQ4	W	X	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4 1: IRQ4 < IRQ1

Note: *Selecting a Reserved mode causes an undefined operation.

Table 24. Interrupt Request Register, R250 IPR FAh Bank 0h: READ/WRITE

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write								

Bit Position	Bit Field	R/W	Reset Value	Description
7-6	Reserved	R/W	00	Reserved-must be 0
5	IRQ5	R/W	0	**Interrupt** IRQ5 = T1 0: No interrupt pending 1: Interrupt pending
4	IRQ4	R/W	**0**	**Interrupt** RQ4 = Software generated 0: No interrupt pending 1: Interrupt pending
3	IRQ3	R/W	**0**	**Interrupt** RQ3 = P32 Input (rising edge) 0: No interrupt pending 1: Interrupt pending
2	IRQ2	R/W	**0**	**Interrupt** RQ2 = P31 Input 0: No interrupt pending 1: Interrupt pending
1	IRQ1,	R/W	**0**	**Interrupt** RQ1 = P33 Input 0: No interrupt pending 1: Interrupt pending
0	IRQ0	R/W	**0**	**Interrupt** RQ0 = P32 Input 0: No interrupt pending 1: Interrupt pending
Note: *Selecting a Reserved mode causes an undefined operation.				