Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52230caf60

Table of Contents

List of Figures

List of Tables

1 MCF52235 Family Configurations

Table 1. MCF52235 Family Configurations

Module	52230	52231	52232	52233	52234	52235	52236
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•	•
System Clock (MHz)	60	60	50	60	60	60	50
Performance (Dhrystone 2.1 MIPS)	56	56	46	56	56	56	46
Flash / Static RAM (SRAM)	128/32 Kbytes	128/32 Kbytes	128/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes
Interrupt Controllers (INTC0/INTC1)	•	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•	•
Random Number Generator and Crypto Acceleration Unit (CAU)	—	—	—	—	—	•	—
FlexCAN 2.0B Module	—	•	—	—	•	•	—
Fast Ethernet Controller (FEC) with on-chip interface (EPHY)	•	•	•	•	•	•	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•	•
Programmable Interrupt Timer	2	2	2	2	2	2	2
Four-Channel General Purpose Timer	•	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4	4
QSPI	•	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port[1]	•	•	•	•	•	•	•
Package	80 LQFP 112 LQFP	80 LQFP 112 LQFP	80 LQFP	80 LQFP 112 LQFP	112 LQFP 121 MAPBGA	112 LQFP 121 MAPBGA	80 LQFP

[1] The full debug/trace interface is available only on the 112- and 121-pin packages. A reduced debug interface is bonded on the 80-pin package.

1.2.1 Feature Overview

The MCF52235 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 60 MHz processor core frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with 32-bit accumulator to support 16 × 16 → 32 or 32 × 32 → 32 operations
  - Cryptography Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - FIPS-140 compliant random number generator
  - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - Up to 32 Kbytes of dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - Up to 256 Kbytes of interleaved Flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
- Fast Ethernet Controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- On-chip Ethernet Transceiver (EPHY)
  - Digital adaptive equalization
  - Supports auto-negotiation
  - Baseline wander correction
  - Full-/Half-duplex support in all modes
  - Loopback modes
  - Supports MDIO preamble suppression
  - Jumbo packet
- FlexCAN 2.0B module

  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)
  - System configuration during reset
  - Selects one of three clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic

1.2.10 I²C Bus

The I²C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices on a circuit board.

1.2.11 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.12 Fast ADC

The Fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 10- or 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, perform a scan whenever triggered, or perform a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.13 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the each device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTINx signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCRn). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.14 General Purpose Timer (GPT)

The general purpose timer (GPT) is a 4-channel timer module consisting of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.15 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or can be a free-running down-counter.

1.2.16 Pulse Width Modulation (PWM) Timers

The MCF52235 has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0 to 100%. The PWM outputs have programmable polarity and can be programmed as left-aligned outputs or center-aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.17 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.18 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.19 Interrupt Controller (INTC0/INTC1)

There are two interrupt controllers on the MCF52235. These interrupt controllers are organized as seven levels with up to nine interrupt sources per level. Each interrupt source has a unique interrupt vector, and provide each peripheral with all necessary interrupts. Each internal interrupt has a programmable level [1-7] and priority within the level. The seven external interrupts have fixed levels/priorities.

1.2.20 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.21 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
UART 1[3]	$\overline{\text{UCTS1}}$	SYNCA	URXD2	PUB[3]	PDSR[15]	—	—	J3	24	16
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	PUB[2]	PDSR[14]	—	—	H3	23	15
	URXD1	—	FEC_TXD[0]	PUB[1]	PDSR[13]	PWOR[2]	—	K3	32	23
	UTXD1	—	FEC_COL	PUB[0]	PDSR[12]	PWOR[3]	—	L3	33	24
UART 2	$\overline{\text{UCTS2}}$	—	—	PUC[3]	PDSR[27]	—	—	L10	61	—
	$\overline{\text{URTS2}}$	—	—	PUC[2]	PDSR[26]	—	—	K10	60	—
	URXD2	—	—	PUC[1]	PDSR[25]	—	—	K11	62	—
	UTXD2	—	—	PUC[0]	PDSR[24]	—	—	L11	63	—
FlexCAN	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	—	27	19
VDD[5,11]	VDD	—	—	—	N/A	N/A	—	D7, E8	65,102	45,74
VDDX	VDDX	—	—	—	N/A	N/A	—	D5, D6, E6, G5, G6, G7, H6	14, 43	10, 31
VSS	VSS	—	—	—	N/A	N/A	—	E4, E5, E7,F4, F5, F6, F7, F8	64,101	44,73
VSSX	VSSX	—	—	—	N/A	N/A	—	—	15, 42	11, 30

1 The PDSR and PSSR registers are described in Chapter 14, "General Purpose I/O Module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The use of an external PHY limits ADC, interrupt, and QSPI functionality. It also disables the UART0/1 and timer pins.
4 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
5 The VDD1, VDD2, VDDPLL, and PHY_VDD pins are for decoupling only and should not have power directly applied to them.
6 For primary and GPIO functions only.
7 Only when JTAG mode is enabled.
8 For secondary and GPIO functions only.
9 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the Ethernet PHY.

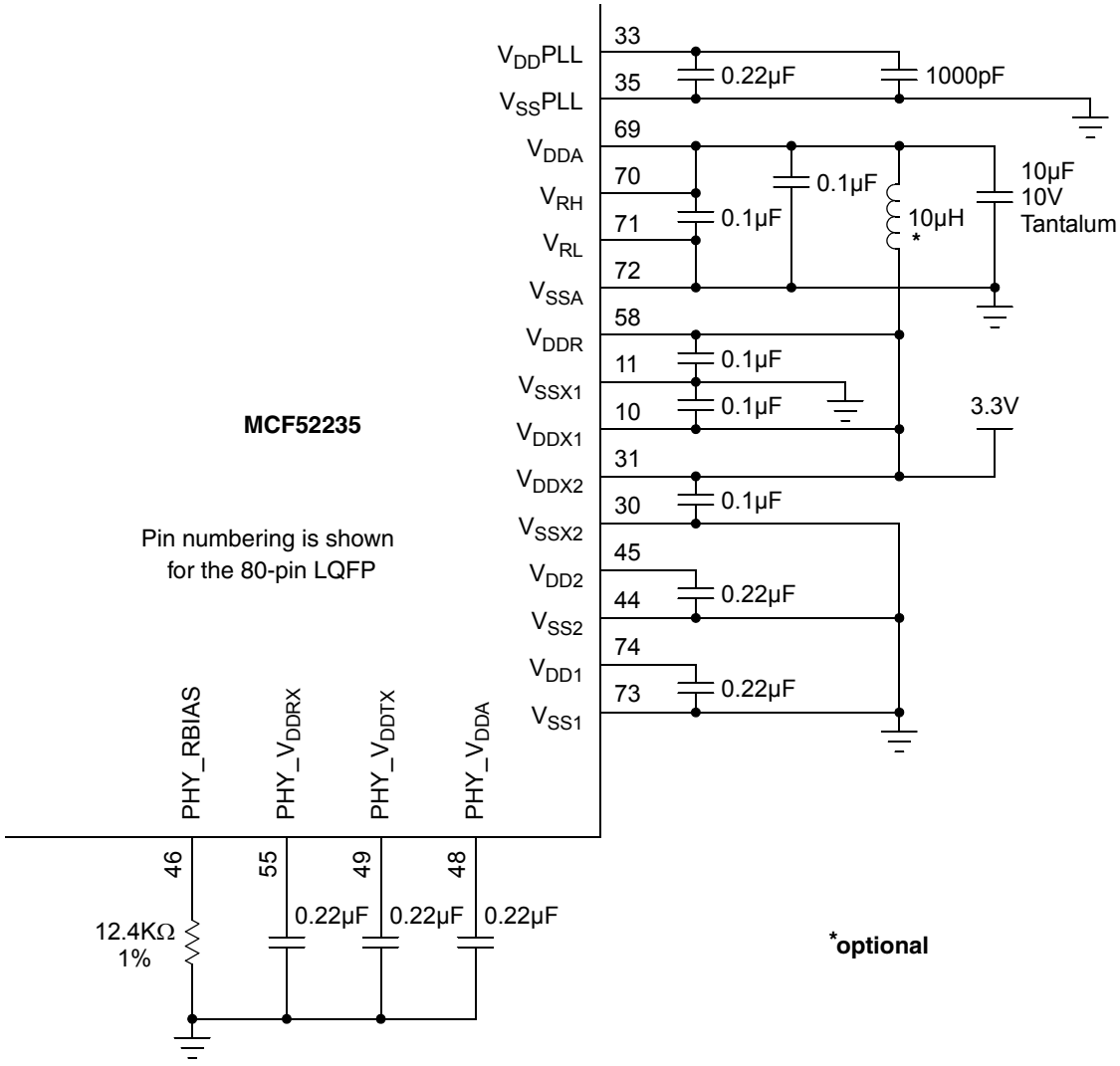


Figure 5. Suggested Connection Scheme for Power and Ground

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF52235, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3 Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

Table 20 lists thermal resistance values.

NOTE

The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

The average chip-junction temperature (T_J) in °C can be obtained from

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

where

- T_A = ambient temperature, °C
- Θ_{JMA} = package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{INT} + P_{I/O}$
- P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
- $P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications, PI/O < P_{INT} and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \Theta_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.2 ESD Protection

Table 21. ESD Protection Characteristics[1]

Characteristic	Symbol	Value	Units
ESD target for Human Body Model	HBM	1500 (ADC and EPHY pins) 2000 (All other pins)	V
ESD target for Charged Device Model	CDM	250	V
HBM circuit description	R_{series}	1500	ohms
	C	100	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (CDM) positive pulses negative pulses	 — —	 3 3	—
Interval of pulses (HBM)	—	1.0	sec
Interval of pulses (CDM)	—	0.2	sec

[1] A device is defined as a failure if the device no longer meets the device specification requirements after exposure to ESD pulses. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.3 DC Electrical Specifications

Table 22. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, input-only pins	I_{in}	–1.0	1.0	µA
High impedance (off-state) leakage current $V_{in} = V_{DD}$ or V_{SS}, all input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Weak internal pull-up device current, tested at V_{IL} max.[2]	I_{APU}	–10	–130	µA
Input capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load capacitance[4] Low drive strength High drive strength	C_L		 25 50	pF
DC injection current [3, 5, 6, 7] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single pin limit Total MCU limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10	 1.0 10	mA

1 Refer to Table 25 for additional PLL specifications.

2 Refer to Table 3 for pins with internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

5 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, the system clock is not present during the power-up sequence until the PLL has attained lock.

2.4 Phase Lock Loop Electrical Specifications

Table 25. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 0.5 0	 25.0 60.0	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [2] External clock mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 60 60	MHz
Loss of reference frequency [3, 5]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [4, 5]	f_{SCM}	1	5	MHz
Crystal start-up time [5, 6]	t_{cst}	—	10	ms
EXTAL input high voltage Crystal reference External reference	V_{IHEXT}	 V_{DD}- 1.0 2.0	 V_{DD} 3.0[7]	V
EXTAL input low voltage Crystal reference External reference	V_{ILEXT}	 V_{SS} V_{SS}	 1.0 0.8	V
XTAL output high voltage I_{OH} = 1.0 mA	V_{OL}	 V_{DD} –1.0	 —	V
XTAL output low voltage I_{OL} = 1.0 mA	V_{OL}	 —	 0.5	V
XTAL load capacitance[8]		—	—	pF
PLL lock time[5,9]	t_{lpll}	—	500	µs
Power-up to lock time [5, 7,9] With crystal reference Without crystal reference	t_{lplk}	 — —	 10.5 500	 ms µs
Duty cycle of reference [5]	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{sys}
Frequency LOCK range	fLCK	–0.75	0.75	% f_{sys}
CLKOUT period Jitter [5, 6, 8, 10,11], measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over 2 ms interval)	C_{jitter}	 — —	 10 0.01	% f_{sys}

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 All internal registers retain data at 0 Hz.

3 Loss of reference frequency is the reference frequency detected internally that transitions the PLL into self-clocked mode.

4 Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

2.6 Reset Timing

Table 27. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT high	t_{RVCH}	9	—	ns
R2	CLKOUT high to $\overline{\text{RSTI}}$ input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT high to $\overline{\text{RSTO}}$ valid	t_{CHROV}	—	10	ns

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Therefore, $\overline{\text{RSTI}}$ must be held a minimum of 100ns.

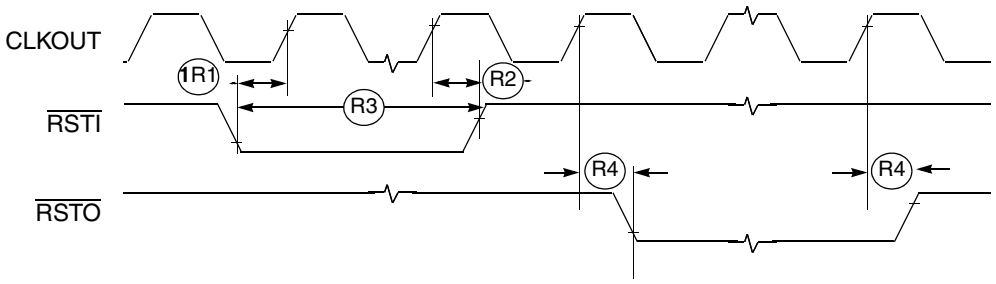


Figure 7. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.7 I²C Input/Output Timing Specifications

Table 28 lists specifications for the I²C input timing parameters shown in Figure 8.

Table 28. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 × t_{CYC}	—	ns
I2	Clock low period	8 × t_{CYC}	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4 × t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 × t_{CYC}	—	ns
I9	Stop condition setup time	2 × t_{CYC}	—	ns

Table 29 lists specifications for the I²C output timing parameters shown in Figure 8.

Table 29. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1 [1]	Start condition hold time	6 × t_{CYC}	—	ns
I2 [1]	Clock low period	10 × t_{CYC}	—	ns
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7 × t_{CYC}	—	ns
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10 × t_{CYC}	—	ns
I7 [1]	Data setup time	2 × t_{CYC}	—	ns
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 29. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 29 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 8 shows timing for the values in Table 28 and Table 29.

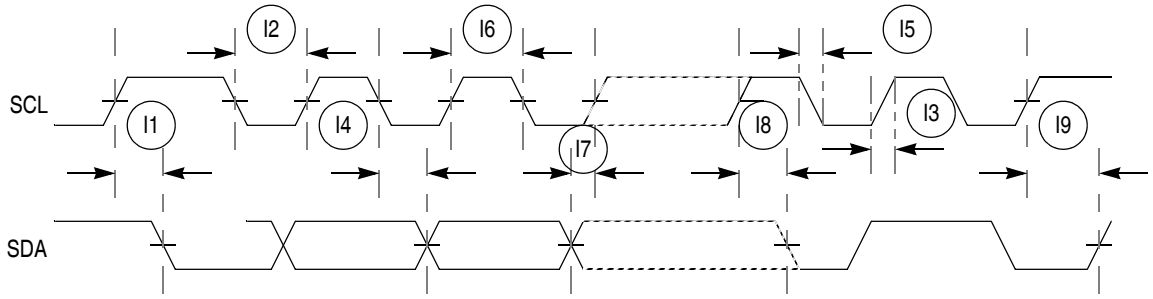


Figure 8. I²C Input/Output Timings

2.8.4 Transceiver Characteristics

Table 33. 10BASE-T Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Peak differential output voltage	V_{OP}	2.2	2.5	2.8	V	With specified transformer and line replaced by 100 Ω(±1%) load
Transmit timing jitter	—	0	2	11	ns	Using line model specified in the IEEE 802.3
Receive dc input impedance	Z_{in}	—	10	—	kΩ	0.0 < V_{in} < 3.3 V
Receive differential squelch level	$V_{squelch}$	300	400	585	mV	3.3 MHz sine wave input

Table 34. 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Transmit Peak Differential Output Voltage	V_{OP}	0.95	1.00	1.05	V	With specified transformer and line replaced by 100 Ω(±1%) load
Transmit Signal Amplitude Symmetry	V_{sym}	98	100	102	%	With specified transformer and line replaced by 100 Ω (±1%) load
Transmit Rise/Fall Time	t_{rf}	3	4	5	ns	With specified transformer and line replaced by 100 Ω (±1%) load
Transmit Rise/Fall Time Symmetry	t_{rfs}	–0.5	0	+0.5	ns	See IEEE 802.3 for details
Transmit Overshoot/UnderShoot	V_{osh}	—	2.5	5	%	
Transmit Jitter	—	0	.6	1.4	ns	
Receive Common Mode Voltage	V_{cm}	—	1.6	—	V	V_{DDRX} = 2.5 V
Receiver Maximum Input Voltage	V_{max}	—	—	4.7	V	V_{DDRX} = 2.5 V. Internal circuits protected by divider in shutdown

2.9 Analog-to-Digital Converter (ADC) Parameters

Table 35 lists specifications for the analog-to-digital converter.

Table 35. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	Analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
	Monotonicity	Guaranteed			

2.14 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 19.

Table 40. Debug AC Timing Specification

Num	Characteristic	60 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 [1]	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT Rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT Rise	1.5	—	ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 18 shows real-time trace timing for the values in Table 40.

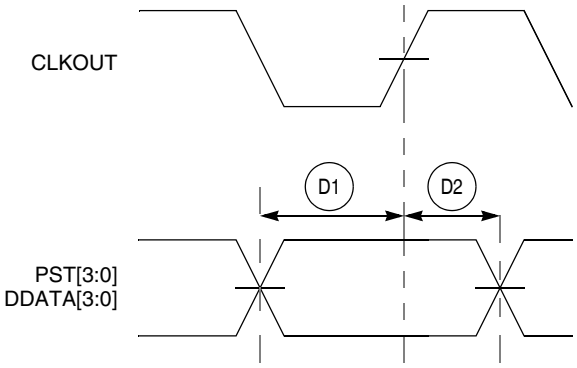


Figure 18. Real-Time Trace AC Timing

Figure 19 shows BDM serial port AC timing for the values in Table 40.

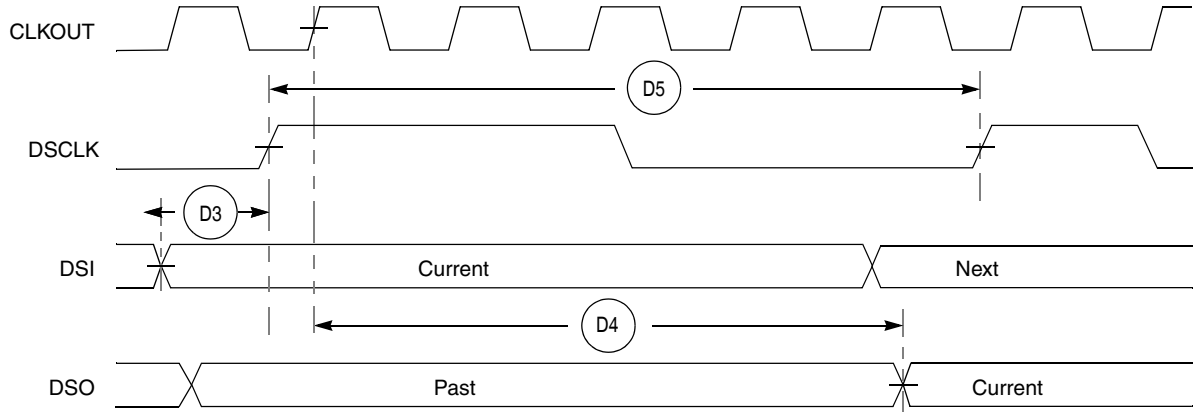
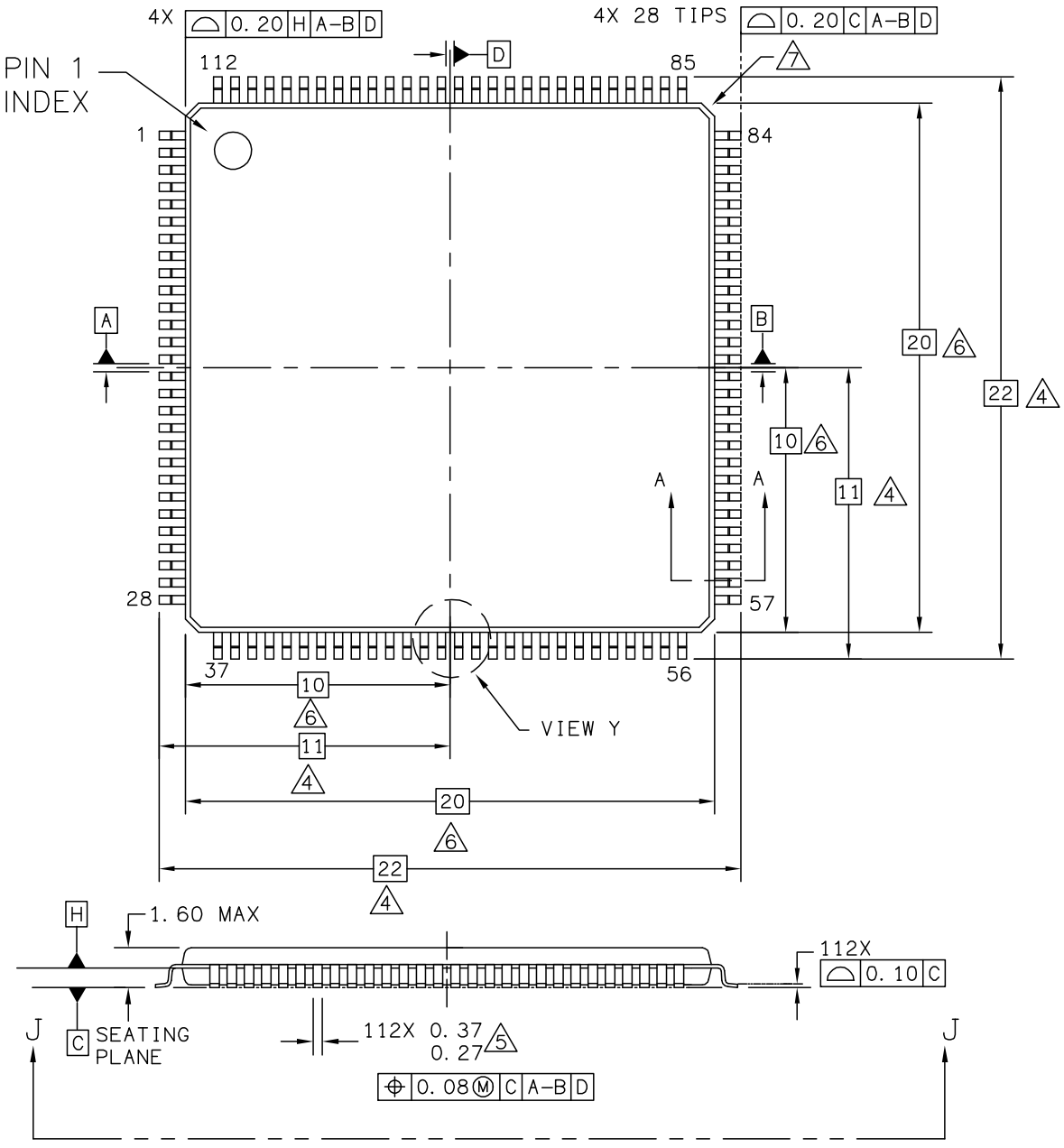
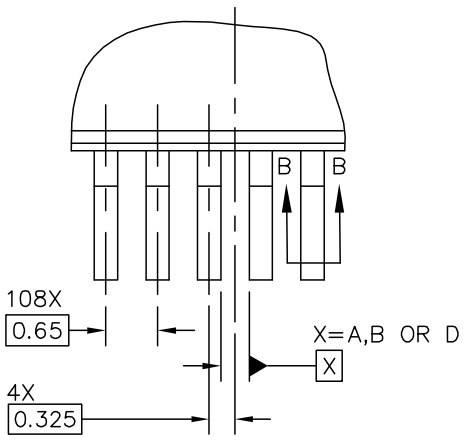


Figure 19. BDM Serial Port AC Timing

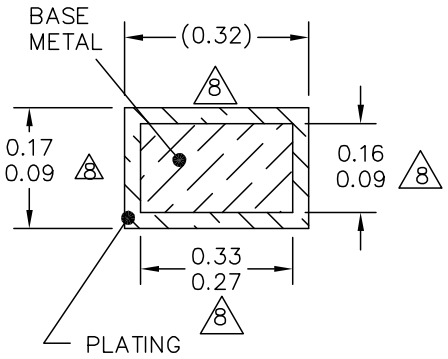
3.2 112-pin LQFP Package



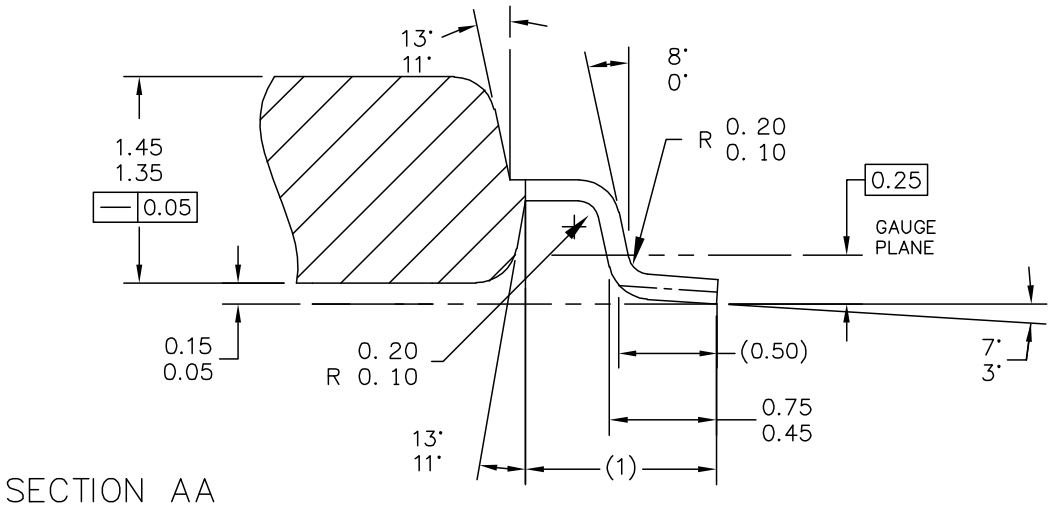
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987-02	25 MAY 2005
	STANDARD: JEDEC MS-026 BFA	



VIEW Y



SECTION B–B



SECTION AA

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

4 Revision History

Table 41. Revision History

Revision	Description
2 (Jul 2006)	• Updated available packages. • Inserted mechanical drawings. • Corrected signal pinouts and table.
3 (Feb 2007)	• Changed signal names TIN to DTIN and TOUT to DTOUT to match the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added overbars to extend over entire $\overline{\text{UCTSn}}$ and $\overline{\text{URTSn}}$ signal name. • Added revision history. • Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Deleted the “PSTCLK cycle time” row from the “Debug AC Timing Specifications” table. • Added “EPHY Timing” section. • Deleted the “RAM standby supply voltage” entry from Table 19. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • In the “Pin Functions by Primary and Alternate Purpose” table, changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was “—”, is 41). • Updated the “Thermal characteristics” table to include proper thermal resistance values. • Added two tables, “Active Current Consumption Specifications” and “Current Consumption Specifications in Low-Power Modes”, containing the latest current consumption information. • Changed the value of T_j in the “Thermal Characteristics” table (was 105 °C, is 130 °C for all packages). • Added the following note to and above the “Thermal Characteristics” table: “The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.” • Added the value for Ψ_{jt} for the 121MAPBGA package (2.0 °C/W).
4 (May 2007)	• Formatting, layout, spelling, and grammar corrections. • Added load test condition information to the “General Purpose I/O Timing” section. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table.
5 (Sep 2007)	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52232 and MCF52236 devices. • Revised the part number table to include full Freescale orderable part numbers. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in the device reference manual and data sheet. • Added specifications for V_{REFL}, V_{REFH}, and V_{DDA} to the “ADC Parameters” table. • Added several EPHY specifications.
6 (Oct 2007)	• Formatting, layout, spelling, and grammar corrections. • Changed the data sheet classification (was “Product Preview”, is “Advance Information”). • Added the “EzPort Electrical Specifications” section. • Updated the “ESD Protection” section.
7 (Aug 2008)	• Changed document type from Advance Information to Technical Data. • Added supported device list in subtitle. • Removed preliminary text from electrical specifications section as device is fully characterized. • Corrected I_{VREFH}, VREFH current unit from “m” to “mA” in ADC specification table. • Changed V_{OFFSET} from TBD to — in ADC specification table.
8 (Jun 2009)	• Updated Orderable Part Number Summary table to include MCF52233CAL60A, MCF52235CAL60A, and MCF52236AF50A parts