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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	73
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52231cal60

  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0–8 bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused Message Buffer space can be used as general purpose RAM space
  - Listen only mode capability
  - Content-related addressing
  - No read/write semaphores required
  - Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O

- Four 32-bit DMA timers
  - 17-ns resolution at 60 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timers
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low power mode support
- Clock Generation Features
  - Crystal input
  - On-chip PLL
  - Provides clock for integrated EPHY
- Dual Interrupt Controllers (INTC0/INTC1)
  - Support for multiple interrupt sources organized as follows:
    - Fully-programmable interrupt sources for each peripheral
    - 7 fixed-level interrupt sources
    - Seven external interrupt signals

pipeline, optimized for 16×16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, access debug information and real-time tracing capability is provided on 112-and 121-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. The MCF52235 implements revision B+ of the ColdFire Debug Architecture.

The MCF52235's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event, thereby ensuring that the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF52235 includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 112 and 121-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The MCF52235 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF52235 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF52235 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF52235 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 16- or 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 16- or 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM

1.2.24 Package Pinouts

Figure 2 shows the pinout configuration for the 80-pin LQFP.

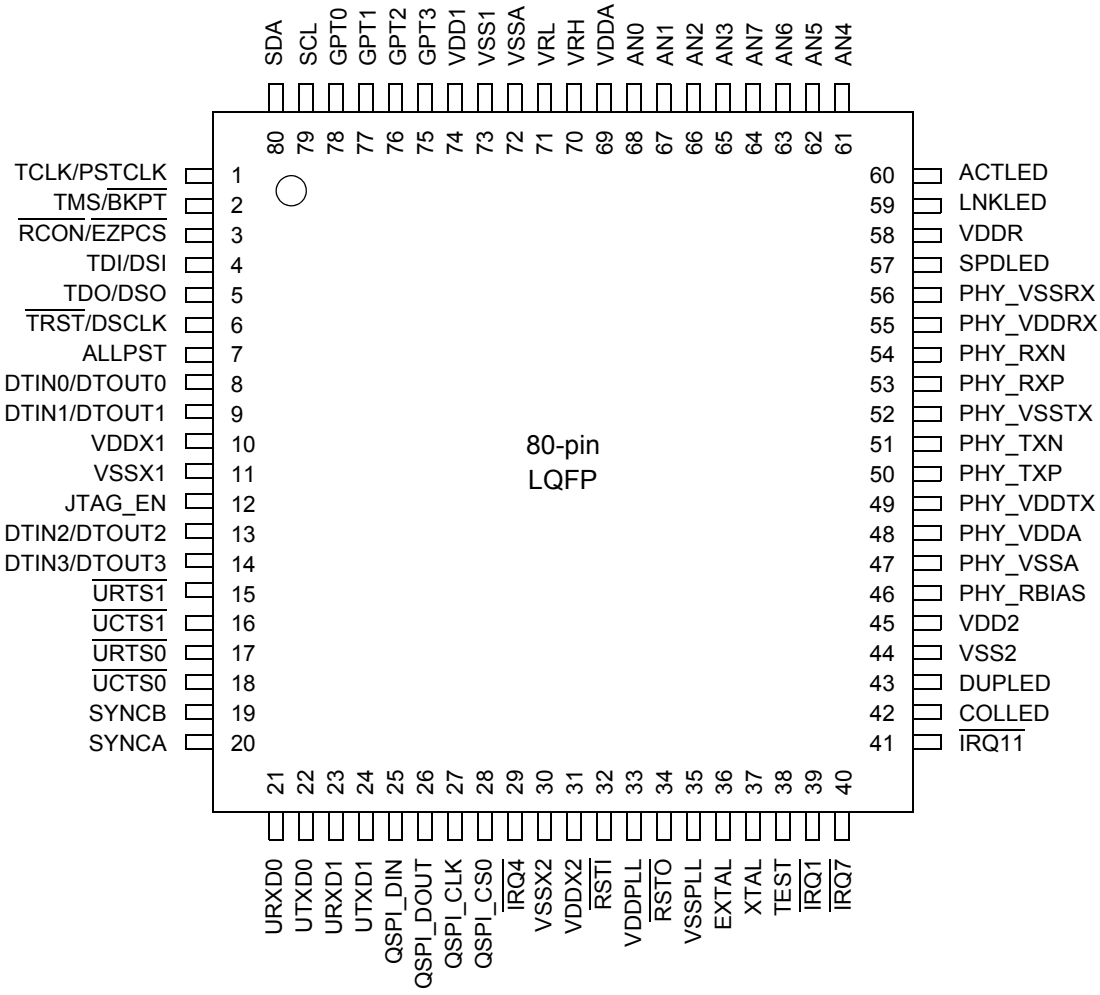


Figure 2. 80-pin LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 112-pin LQFP.

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
Ethernet LEDs	ACTLED	—	—	PLD[0]	PDSR[32]	PWOR[8]	—	C11	84	60
	COLLED	—	—	PLD[4]	PDSR[36]	PWOR[12]	—	J9	58	42
	DUPLED	—	—	PLD[3]	PDSR[35]	PWOR[11]	—	J10	59	43
	LNKLED	—	—	PLD[1]	PDSR[33]	PWOR[9]	—	C10	83	59
	SPDLED	—	—	PLD[2]	PDSR[34]	PWOR[10]	—	D11	81	57
	RXLED	—	—	PLD[5]	PDSR[37]	PWOR[13]	—	H9	52	—
	TXLED	—	—	PLD[6]	PDSR[38]	PWOR[14]	—	H8	51	—
	VDDR	—	—	—	—	—	—	D8	82	58
Ethernet PHY	PHY_RBIAS	—	—	—	—	—		J11	66	46
	PHY_RXN	—	—	—	—	—		E11	74	54
	PHY_RXP	—	—	—	—	—		F11	73	53
	PHY_TXN	—	—	—	—	—		H11	71	51
	PHY_TXP	—	—	—	—	—		G11	70	50
	PHY_VDDA[5]	—	—	—		N/A		H10	68	48
	PHY_VDDRX[5]	—	—	—		N/A		F10	75	55
	PHY_VDDTX[5]	—	—	—		N/A		G10	69	49
	PHY_VSSA	—	—	—		N/A		G8	67	47
	PHY_VSSRX	—	—	—		N/A		F9	76	56
	PHY_VSSTX	—	—	—		N/A		G9	72	52
I^2C	SCL	CANTX[4]	UTXD2	PAS[0]	PDSR[0]	—	Pull-Up[6]	A3	111	79
	SDA	CANRX[4]	URXD2	PAS[1]	PDSR[0]	—	Pull-Up[6]	A2	112	80
Interrupts[3]	IRQ15	—	—	PGP[7]	PSDR[47]	—	Pull-Up[6]	A4	106	—
	IRQ14	—	—	PGP[6]	PSDR[46]	—	Pull-Up[6]	A5	105	—
	IRQ13	—	—	PGP[5]	PSDR[45]	—	Pull-Up[6]	A6	98	—
	IRQ12	—	—	PGP[4]	PSDR[44]	—	Pull-Up[6]	C7	97	—

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock. Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint. Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status signals (PST[3:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input. Internally synchronized input that provides data input for the serial communication port to the debug module after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output. Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock. Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, PST, and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be re-enabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]	O

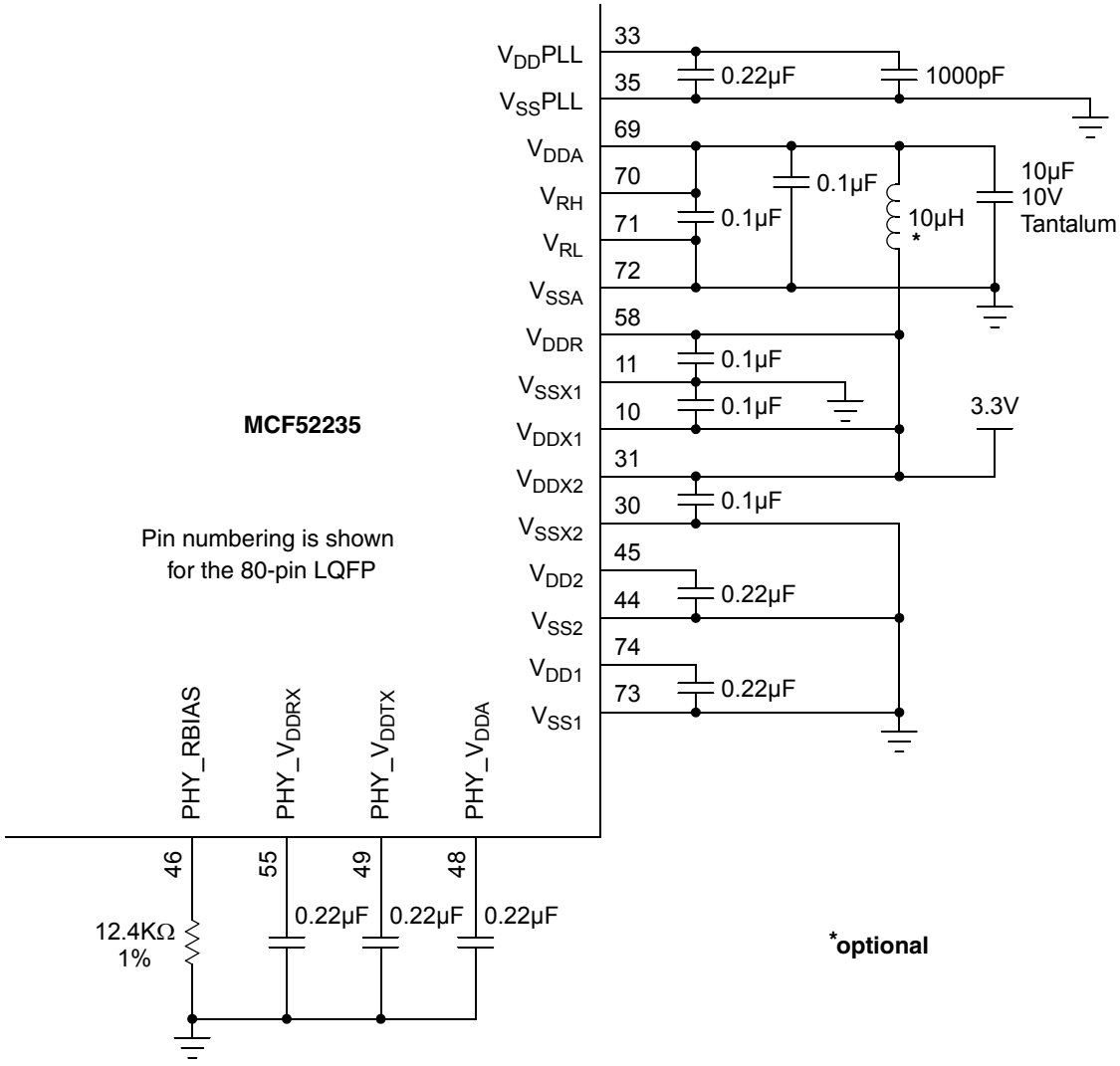


Figure 5. Suggested Connection Scheme for Power and Ground

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF52235, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3 Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

Table 20 lists thermal resistance values.

NOTE

The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

The average chip-junction temperature (T_J) in °C can be obtained from

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

where

- T_A = ambient temperature, °C
- Θ_{JMA} = package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{INT} + P_{I/O}$
- P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
- $P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications, PI/O < P_{INT} and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \Theta_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.2 ESD Protection

Table 21. ESD Protection Characteristics[1]

Characteristic	Symbol	Value	Units
ESD target for Human Body Model	HBM	1500 (ADC and EPHY pins) 2000 (All other pins)	V
ESD target for Charged Device Model	CDM	250	V
HBM circuit description	R_{series}	1500	ohms
	C	100	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (CDM) positive pulses negative pulses	 — —	 3 3	—
Interval of pulses (HBM)	—	1.0	sec
Interval of pulses (CDM)	—	0.2	sec

[1] A device is defined as a failure if the device no longer meets the device specification requirements after exposure to ESD pulses. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.3 DC Electrical Specifications

Table 22. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, input-only pins	I_{in}	–1.0	1.0	µA
High impedance (off-state) leakage current $V_{in} = V_{DD}$ or V_{SS}, all input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Weak internal pull-up device current, tested at V_{IL} max.[2]	I_{APU}	–10	–130	µA
Input capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load capacitance[4] Low drive strength High drive strength	C_L		 25 50	pF
DC injection current [3, 5, 6, 7] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single pin limit Total MCU limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10	 1.0 10	mA

1 Refer to Table 25 for additional PLL specifications.

2 Refer to Table 3 for pins with internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

5 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, the system clock is not present during the power-up sequence until the PLL has attained lock.

Table 23. Active Current Consumption Specifications

Characteristic	Symbol	Typical				Peak	Unit
		Running from SRAM, EPHY Off	Running from Flash, EPHY Off	Running from Flash, EPHY 10BaseT	Running from Flash, EPHY 100BaseT		
Active current, core and I/O PLL @25 MHz PLL @60 MHz	$I_{DDR}+I_{DDX}+I_{DDA}$	 75 130	 82 138	 150 220	 260 310	 290 340	 mA
Analog supply current Normal operation Low-power STOP	I_{DDA}	 20 15	 20 15	 20 15	 20 15	 30 50	 mA μA

Table 24. Current Consumption Specifications in Low-Power Modes[1]

Mode[2]	PLL @25 MHz (typical)[3]	PLL @60 MHz (typical)[3]	PLL @60 MHz (peak)[4]	Unit
STOP mode 3 (STPMD[1:0]=11)	0.2		1.0	mA
STOP mode 2 (STPMD[1:0]=10)	7		—	
STOP mode 1 (STPMD[1:0]=01)	10	12	—	
STOP mode 0 (STPMD[1:0]=00)	10	12	—	
WAIT	16	27	—	
DOZE	16	27	—	
RUN	25	45	—	

1 All values are measured with a 3.30 V power supply.

2 Refer to the “Power Management” chapter in the *MCF52235 ColdFire® Integrated Microcontroller Reference Manual* for more information on low-power modes.

3 These values were obtained with CLKOUT and all peripheral clocks except for the CFM clock disabled prior to entering low-power mode. The tests were performed at room temperature. All code was executed from flash memory; running code from SRAM further reduces power consumption.

4 These values were obtained with CLKOUT and all peripheral clocks enabled. All code was executed from flash memory.

[7] This value has been updated

[8] Load capacitance determined from crystal manufacturer specifications and include circuit board parasitics.

[9] Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDPLL} are valid to $\overline{RSTO}$ negating. If the crystal oscillator is the reference for the PLL, the crystal start up time must be added to the PLL lock time to determine the total start-up time.

[10] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval

[11] Based on slow system clock of 40 MHz measured at f_{sys} max.

2.5 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, timers, UARTs, FEC, and interrupts. When in GPIO mode, the timing specification for these pins is given in Table 26 and Figure 6.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

Table 26. GPIO Timing

Num	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT high to GPIO output valid	t_{CHPOV}	—	10	ns
G2	CLKOUT high to GPIO output invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO input valid to CLKOUT high	t_{PVCH}	9	—	ns
G4	CLKOUT high to GPIO input invalid	t_{CHPI}	1.5	—	ns

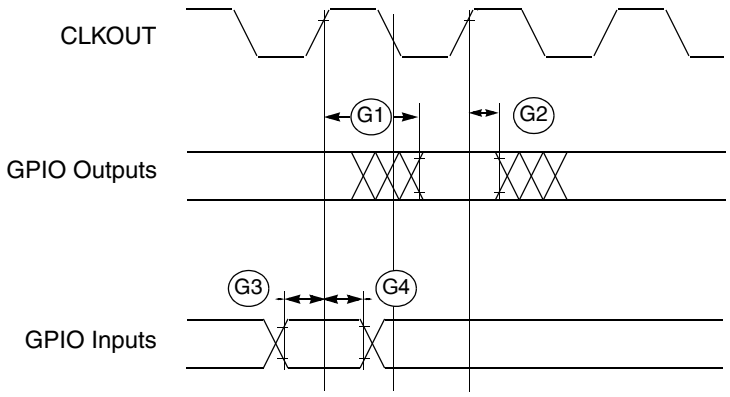


Figure 6. GPIO Timing

2.8 EPHY Parameters

2.8.1 EPHY Timing

Table 30 and Figure 9 show the relevant EPHY timing parameters.

Table 30. EPHY Timing Parameters

Num	Characteristic	Symbol	Value	Unit
E1	EPHY startup time	$t_{Start-Up}$	360	µs

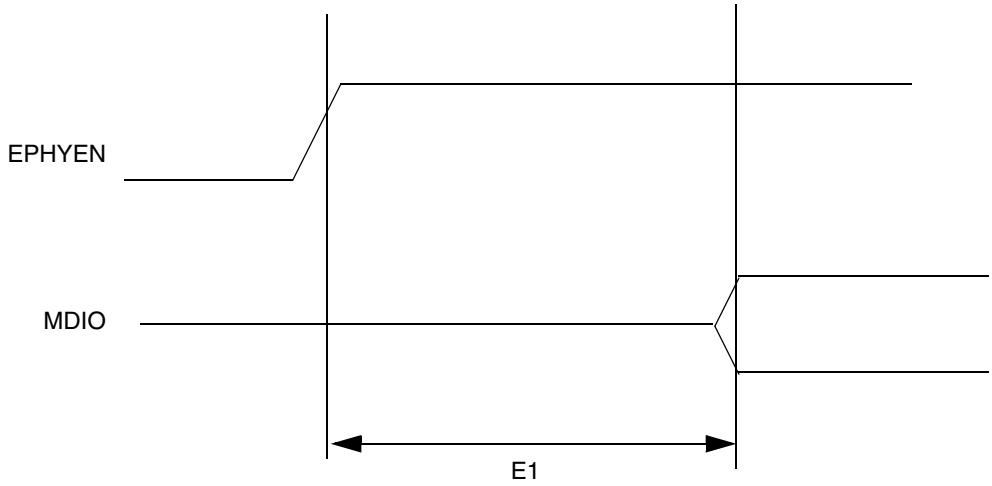


Figure 9. EPHY Timing

2.8.2 10BASE-T SQE (Heartbeat) Timing

Table 31 and Figure 10 show the relevant 10BASE-T SQE (heartbeat) timing parameters.

Table 31. 10BASE-T SQE (Heartbeat) Timing Parameters

Characteristic	Symbol	Min	Typ[1]	Max	Units
COL (SQE) delay after TXEN off	t1	—	1.0	—	µs
COL (SQE) pulse duration	t2	—	1.0	—	µs

[1] Typical values are at 25°C.

2.8.4 Transceiver Characteristics

Table 33. 10BASE-T Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Peak differential output voltage	V_{OP}	2.2	2.5	2.8	V	With specified transformer and line replaced by 100 Ω(±1%) load
Transmit timing jitter	—	0	2	11	ns	Using line model specified in the IEEE 802.3
Receive dc input impedance	Z_{in}	—	10	—	kΩ	0.0 < V_{in} < 3.3 V
Receive differential squelch level	$V_{squelch}$	300	400	585	mV	3.3 MHz sine wave input

Table 34. 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Transmit Peak Differential Output Voltage	V_{OP}	0.95	1.00	1.05	V	With specified transformer and line replaced by 100 Ω(±1%) load
Transmit Signal Amplitude Symmetry	V_{sym}	98	100	102	%	With specified transformer and line replaced by 100 Ω (±1%) load
Transmit Rise/Fall Time	t_{rf}	3	4	5	ns	With specified transformer and line replaced by 100 Ω (±1%) load
Transmit Rise/Fall Time Symmetry	t_{rfs}	–0.5	0	+0.5	ns	See IEEE 802.3 for details
Transmit Overshoot/UnderShoot	V_{osh}	—	2.5	5	%	
Transmit Jitter	—	0	.6	1.4	ns	
Receive Common Mode Voltage	V_{cm}	—	1.6	—	V	V_{DDRX} = 2.5 V
Receiver Maximum Input Voltage	V_{max}	—	—	4.7	V	V_{DDRX} = 2.5 V. Internal circuits protected by divider in shutdown

2.9 Analog-to-Digital Converter (ADC) Parameters

Table 35 lists specifications for the analog-to-digital converter.

Table 35. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	Analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
	Monotonicity	Guaranteed			

2.13 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

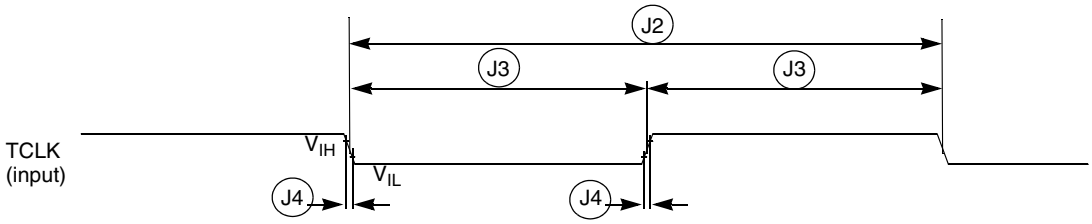
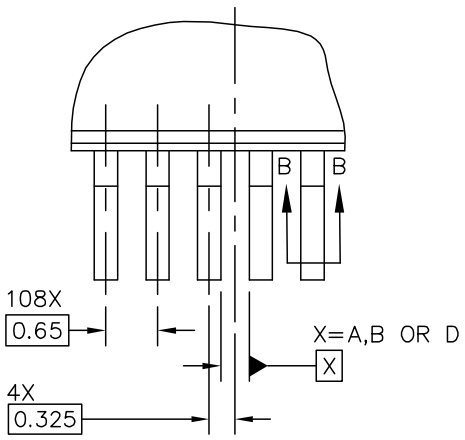
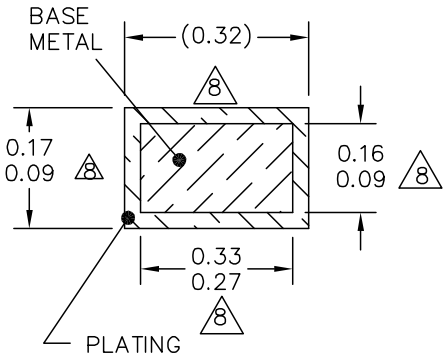


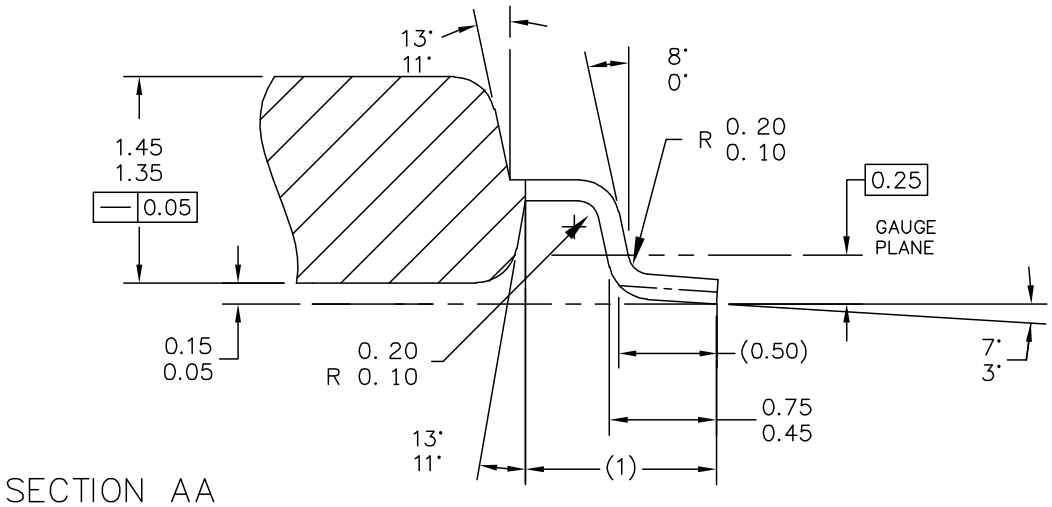
Figure 14. Test Clock Input Timing



VIEW Y



SECTION B–B



SECTION AA

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D	REV: O
	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

4 Revision History

Table 41. Revision History

Revision	Description
2 (Jul 2006)	• Updated available packages. • Inserted mechanical drawings. • Corrected signal pinouts and table.
3 (Feb 2007)	• Changed signal names TIN to DTIN and TOUT to DTOUT to match the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added overbars to extend over entire $\overline{\text{UCTSn}}$ and $\overline{\text{URTSn}}$ signal name. • Added revision history. • Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Deleted the “PSTCLK cycle time” row from the “Debug AC Timing Specifications” table. • Added “EPHY Timing” section. • Deleted the “RAM standby supply voltage” entry from Table 19. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • In the “Pin Functions by Primary and Alternate Purpose” table, changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was “—”, is 41). • Updated the “Thermal characteristics” table to include proper thermal resistance values. • Added two tables, “Active Current Consumption Specifications” and “Current Consumption Specifications in Low-Power Modes”, containing the latest current consumption information. • Changed the value of T_j in the “Thermal Characteristics” table (was 105 °C, is 130 °C for all packages). • Added the following note to and above the “Thermal Characteristics” table: “The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.” • Added the value for Ψ_{jt} for the 121MAPBGA package (2.0 °C/W).
4 (May 2007)	• Formatting, layout, spelling, and grammar corrections. • Added load test condition information to the “General Purpose I/O Timing” section. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table.
5 (Sep 2007)	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52232 and MCF52236 devices. • Revised the part number table to include full Freescale orderable part numbers. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in the device reference manual and data sheet. • Added specifications for V_{REFL}, V_{REFH}, and V_{DDA} to the “ADC Parameters” table. • Added several EPHY specifications.
6 (Oct 2007)	• Formatting, layout, spelling, and grammar corrections. • Changed the data sheet classification (was “Product Preview”, is “Advance Information”). • Added the “EzPort Electrical Specifications” section. • Updated the “ESD Protection” section.
7 (Aug 2008)	• Changed document type from Advance Information to Technical Data. • Added supported device list in subtitle. • Removed preliminary text from electrical specifications section as device is fully characterized. • Corrected I_{VREFH}, VREFH current unit from “m” to “mA” in ADC specification table. • Changed V_{OFFSET} from TBD to — in ADC specification table.
8 (Jun 2009)	• Updated Orderable Part Number Summary table to include MCF52233CAL60A, MCF52235CAL60A, and MCF52236AF50A parts

Table 41. Revision History (continued)

Revision	Description
8 Sep 2009	• Updated Table 25 — PLL Electrical Specifications.
8 April 2010	• Updated Table 37— EzPort Electrical Specifications
22 Mar 2011	• Updated Table Oscillator and PLL Electrical Specification. In EXTAL input high voltage updated VDD to 3.0
23-Mar-2011	• Changed EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, add a note this value has been updated. • Updated clock generation feature