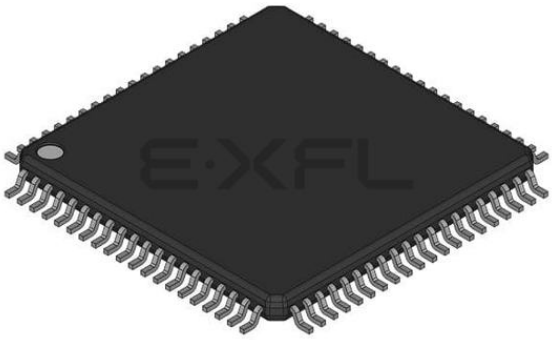

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52232af50

Table of Contents

List of Figures

List of Tables

  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0–8 bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused Message Buffer space can be used as general purpose RAM space
  - Listen only mode capability
  - Content-related addressing
  - No read/write semaphores required
  - Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O

module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32 K×16-bit flash arrays to generate 256 Kbytes of 32-bit flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle flash arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash programming interface that allows the flash to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips. This allows easy device programming via Automated Test Equipment or bulk programming tools.

1.2.6 Cryptography Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The MCF52235 incorporates several low-power modes of operation which are entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

1.2.9 UARTs

The MCF52235 has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

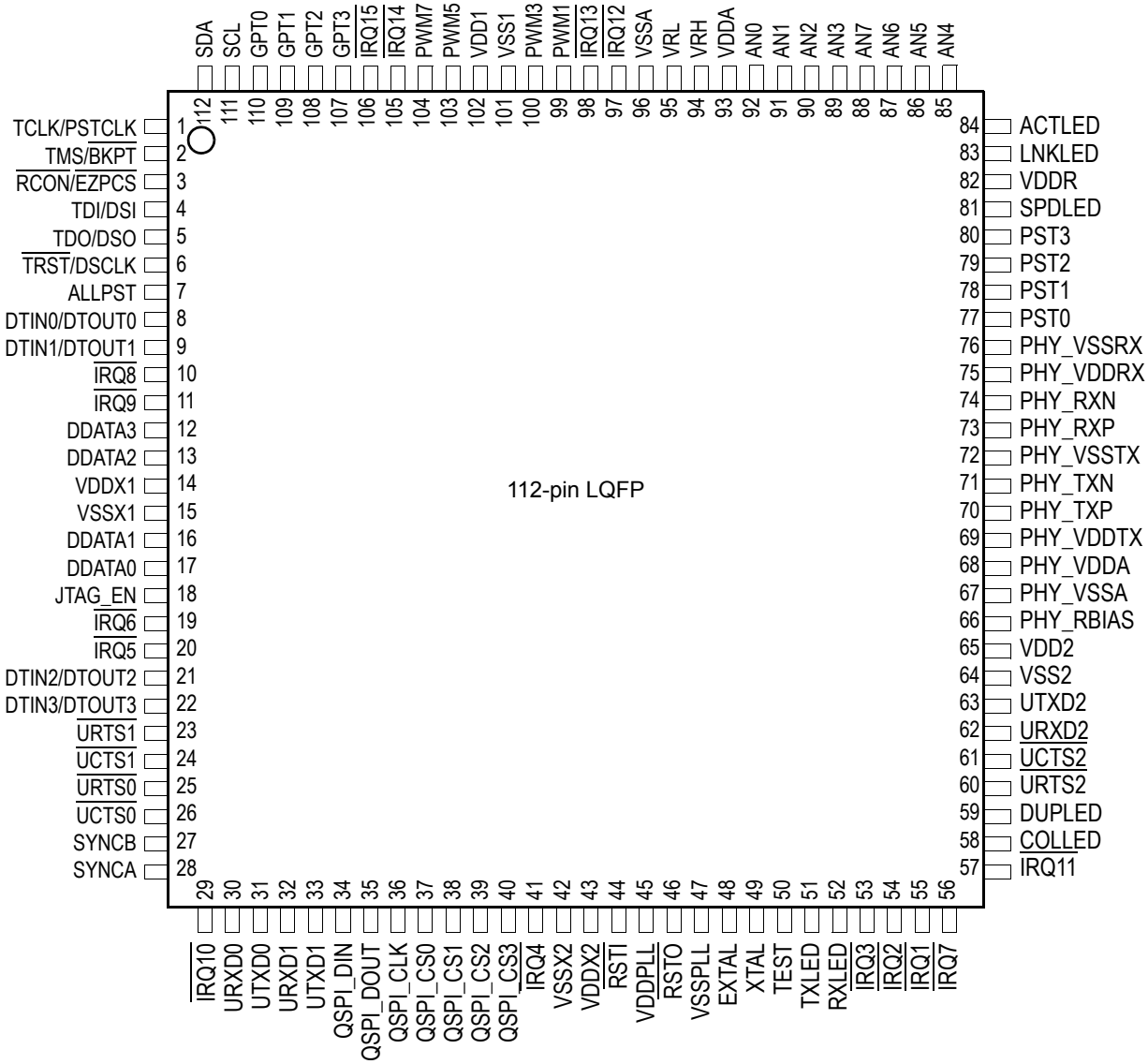


Figure 3. 112-pin LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 121 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11
A	TCLK	SDA	SCL	$\overline{\text{IRQ15}}$	$\overline{\text{IRQ14}}$	$\overline{\text{IRQ13}}$	VSSA	VDDA	AN1	AN7	AN5
B	TMS	$\overline{\text{RCON}}$	GPT0	GPT3	PWM5	PWM1	VRL	VRH	AN2	AN6	AN4
C	$\overline{\text{TRST}}$	TDO	TDI	GPT2	PWM7	PWM3	$\overline{\text{IRQ12}}$	AN0	AN3	LNKLED	ACTLED
D	DTIN1	DTIN0	ALLPST	GPT1	VDDX	VDDX	VDD	VDDR	PST2	PST3	SPDLED
E	DDATA3	$\overline{\text{IRQ9}}$	$\overline{\text{IRQ8}}$	VSS	VSS	VDDX	VSS	VDD	PST0	PST1	PHY_RXN
F	DDATA0	DDATA1	DDATA2	VSS	VSS	VSS	VSS	VSS	PHY_VSSRX	PHY_VDDRX	PHY_RXP
G	DTIN2	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	JTAG_EN	VDDX	VDDX	VDDX	PHY_VSSA	PHY_VSSTX	PHY_VDDTX	PHY_TXP
H	DTIN3	$\overline{\text{URTS0}}$	$\overline{\text{URTS1}}$	QSPI_DIN	QSPI_CS1	VDDX	TEST	TXLED	RXLED	PHY_VDDA	PHY_TXN
J	SYNCB	$\overline{\text{UCTS0}}$	$\overline{\text{UCTS1}}$	QSPI_DOUT	QSPI_CS2	$\overline{\text{RSTI}}$	XTAL	$\overline{\text{IRQ1}}$	COLLED	DUPLED	PHY_RBIAS
K	SYNCA	URXD0	URXD1	QSPI_CLK	QSPI_CS3	VDDPLL	VSSPLL	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ11}}$	$\overline{\text{URTS2}}$	URXD2
L	$\overline{\text{IRQ10}}$	UTXD0	UTXD1	QSPI_CS0	$\overline{\text{IRQ4}}$	$\overline{\text{RSTO}}$	EXTAL	$\overline{\text{IRQ3}}$	$\overline{\text{IRQ7}}$	$\overline{\text{UCTS2}}$	UTXD2

Figure 4. 121 MAPBGA Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
UART 1[3]	$\overline{\text{UCTS1}}$	SYNCA	URXD2	PUB[3]	PDSR[15]	—	—	J3	24	16
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	PUB[2]	PDSR[14]	—	—	H3	23	15
	URXD1	—	FEC_TXD[0]	PUB[1]	PDSR[13]	PWOR[2]	—	K3	32	23
	UTXD1	—	FEC_COL	PUB[0]	PDSR[12]	PWOR[3]	—	L3	33	24
UART 2	$\overline{\text{UCTS2}}$	—	—	PUC[3]	PDSR[27]	—	—	L10	61	—
	$\overline{\text{URTS2}}$	—	—	PUC[2]	PDSR[26]	—	—	K10	60	—
	URXD2	—	—	PUC[1]	PDSR[25]	—	—	K11	62	—
	UTXD2	—	—	PUC[0]	PDSR[24]	—	—	L11	63	—
FlexCAN	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	—	27	19
VDD[5,11]	VDD	—	—	—	N/A	N/A	—	D7, E8	65,102	45,74
VDDX	VDDX	—	—	—	N/A	N/A	—	D5, D6, E6, G5, G6, G7, H6	14, 43	10, 31
VSS	VSS	—	—	—	N/A	N/A	—	E4, E5, E7,F4, F5, F6, F7, F8	64,101	44,73
VSSX	VSSX	—	—	—	N/A	N/A	—	—	15, 42	11, 30

1 The PDSR and PSSR registers are described in Chapter 14, "General Purpose I/O Module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The use of an external PHY limits ADC, interrupt, and QSPI functionality. It also disables the UART0/1 and timer pins.
4 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
5 The VDD1, VDD2, VDDPLL, and PHY_VDD pins are for decoupling only and should not have power directly applied to them.
6 For primary and GPIO functions only.
7 Only when JTAG mode is enabled.
8 For secondary and GPIO functions only.
9 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the Ethernet PHY.

1.3 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 512 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input.	I
Crystal	XTAL	Crystal oscillator output.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 6 describes signals used in mode selection, Table 6 describes particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device.	—
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

1.6 External Interrupt Signals

Table 7 describes the external interrupt signals.

Table 7. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[15:1]	External interrupt sources.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock. Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint. Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status signals (PST[3:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input. Internally synchronized input that provides data input for the serial communication port to the debug module after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output. Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock. Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, PST, and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be re-enabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]	O

1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK	O

1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.	I
Positive Supply	VDD	These pins supply positive power to the core logic.	I
Ground	VSS	This pin is the negative supply (ground) to the chip.	—

Some of the V_{DD} and V_{SS} pins on the device are only to be used for noise bypass. Figure 5 shows a typical connection diagram. Pay particular attention to those pins which show only capacitor connections. Do not connect power supply voltage directly to these pins.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3 Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

Table 20 lists thermal resistance values.

NOTE

The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

Table 20. Thermal Characteristics

Characteristic	Symbol	Package[1]	Value	Unit
Junction to ambient, natural convection	θ_{JA}	80-pin LQFP, four-layer board	36.0[2,3]	°C/W
		112-pin LQFP, four-layer board	35.0	
		121 MAPBGA, four-layer board	32	
		80-pin LQFP, one-layer board[1]	49.0[1]	
		121 MAPBGA, one-layer board[1]	56[1]	
		112-pin LQFP, one-layer board[1]	44.0[1]	
Junction to ambient (@200 ft/min)	θ_{JMA}	80-pin LQFP, four-layer board	30.0	°C/W
		112-pin LQFP, four-layer board	29.0	
		121 MAPBGA, four-layer board	28	
		80-pin LQFP, one-layer board[1]	39.0[1]	
		112-pin LQFP, one-layer board[1]	35.0[1]	
		121 MAPBGA, one-layer board[1]	46[1]	
Junction to board	θ_{JB}	80-pin LQFP	22.0[4]	°C/W
		112-pin LQFP	23.0	
		121 MAPBGA, four-layer board	18	
Junction to case	θ_{JC}	80-pin LQFP	6.0[5]	°C/W
		112-pin LQFP	6.0	
		121 MAPBGA	10	
Junction to top of package, natural convection	Ψ_{jt}	80-pin LQFP	2.0[6]	°C/W
		112-pin LQFP	2.0[6]	
		121 MAPBGA	2.0[6]	
Maximum operating junction temperature	T_j	All	130	°C

1 The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

2 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JMA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

2.4 Phase Lock Loop Electrical Specifications

Table 25. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 0.5 0	 25.0 60.0	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [2] External clock mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 60 60	MHz
Loss of reference frequency [3, 5]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [4, 5]	f_{SCM}	1	5	MHz
Crystal start-up time [5, 6]	t_{cst}	—	10	ms
EXTAL input high voltage Crystal reference External reference	V_{IHEXT}	 V_{DD}- 1.0 2.0	 V_{DD} 3.0[7]	V
EXTAL input low voltage Crystal reference External reference	V_{ILEXT}	 V_{SS} V_{SS}	 1.0 0.8	V
XTAL output high voltage I_{OH} = 1.0 mA	V_{OL}	 V_{DD} –1.0	 —	V
XTAL output low voltage I_{OL} = 1.0 mA	V_{OL}	 —	 0.5	V
XTAL load capacitance[8]		—	—	pF
PLL lock time[5,9]	t_{lpll}	—	500	µs
Power-up to lock time [5, 7,9] With crystal reference Without crystal reference	t_{lplk}	 — —	 10.5 500	 ms µs
Duty cycle of reference [5]	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{sys}
Frequency LOCK range	fLCK	–0.75	0.75	% f_{sys}
CLKOUT period Jitter [5, 6, 8, 10,11], measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over 2 ms interval)	C_{jitter}	 — —	 10 0.01	% f_{sys}

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 All internal registers retain data at 0 Hz.

3 Loss of reference frequency is the reference frequency detected internally that transitions the PLL into self-clocked mode.

4 Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

Table 37. EzPort Electrical Specifications (continued)

Name	Characteristic	Min	Max	Unit
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.12 QSPI Electrical Specifications

Table 38 lists QSPI timings.

Table 38. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (input hold)	9	—	ns

The values in Table 38 correspond to Figure 13.

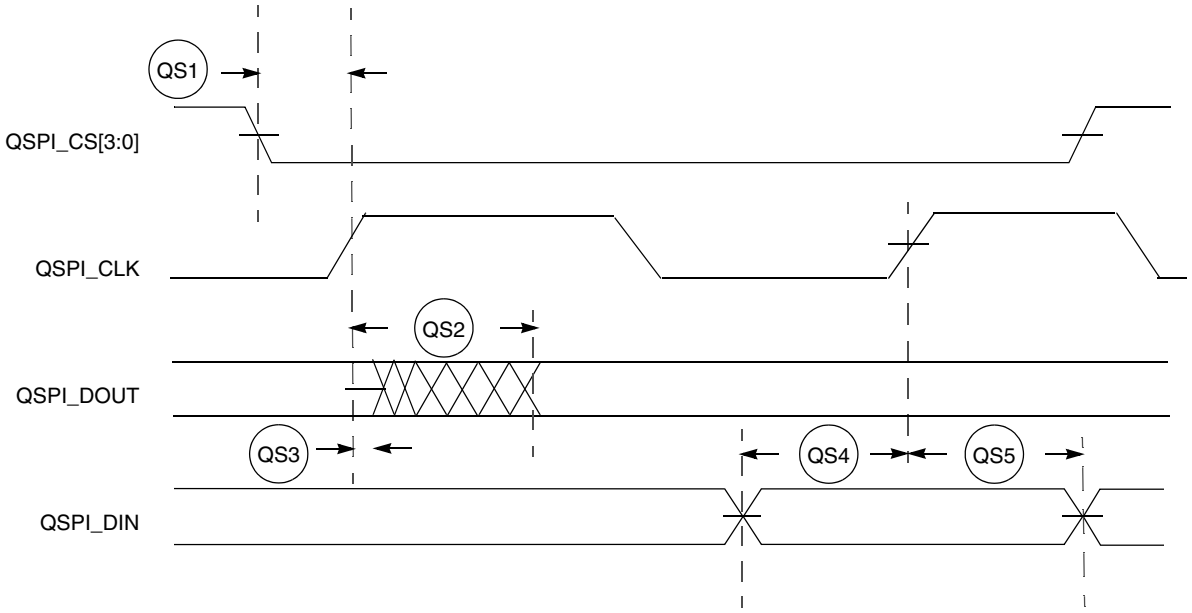


Figure 13. QSPI Timing

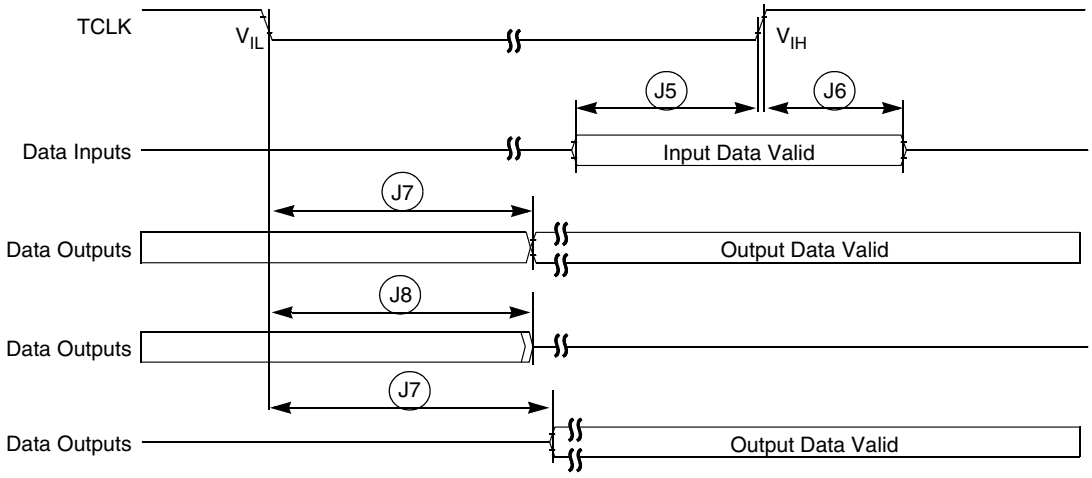


Figure 15. Boundary Scan (JTAG) Timing

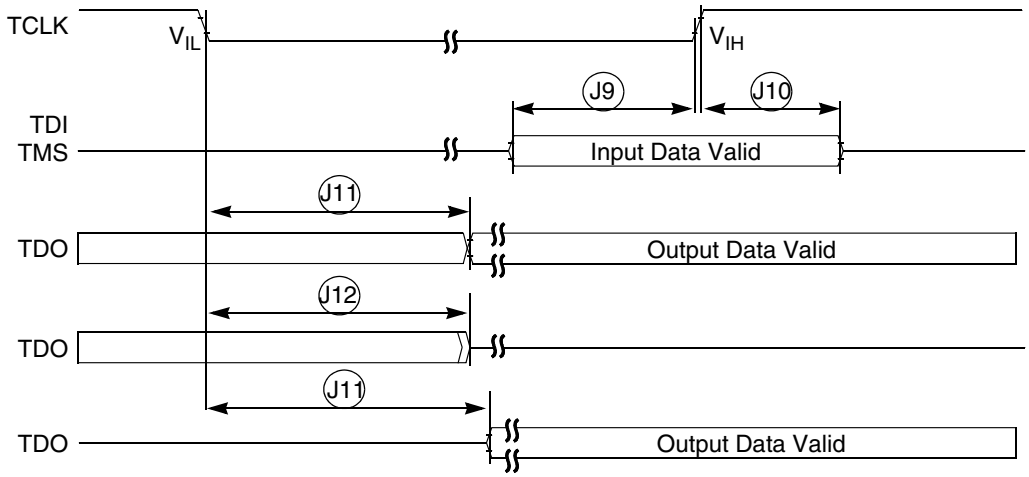


Figure 16. Test Access Port Timing

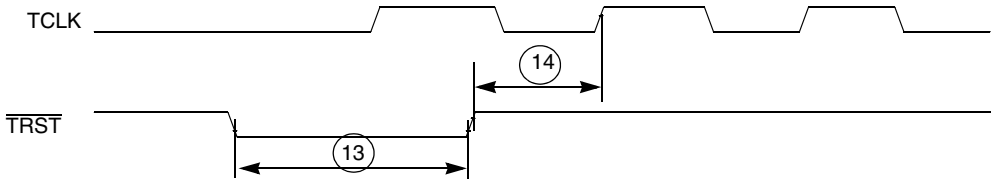


Figure 17. TRST Timing

2.14 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 19.

Table 40. Debug AC Timing Specification

Num	Characteristic	60 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 [1]	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT Rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT Rise	1.5	—	ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 18 shows real-time trace timing for the values in Table 40.

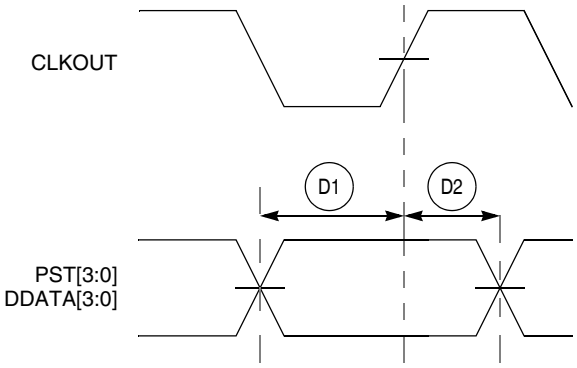


Figure 18. Real-Time Trace AC Timing

Figure 19 shows BDM serial port AC timing for the values in Table 40.

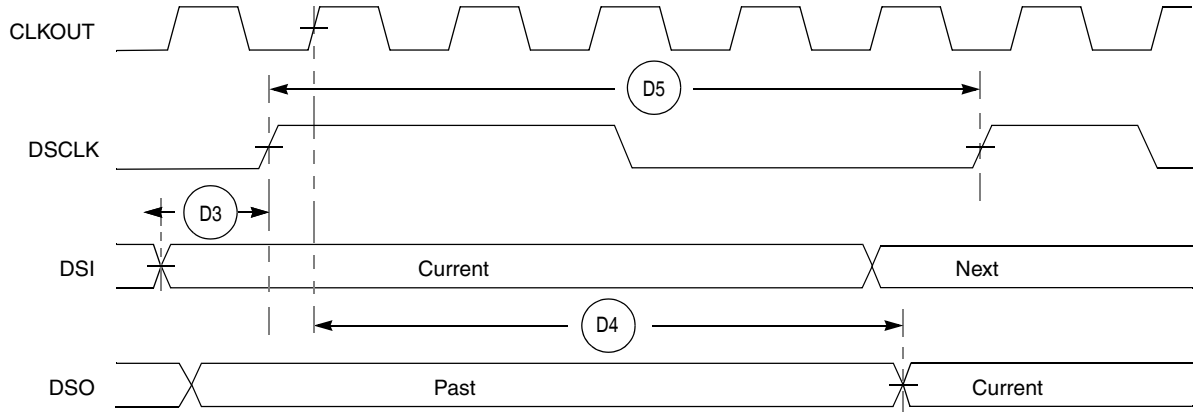
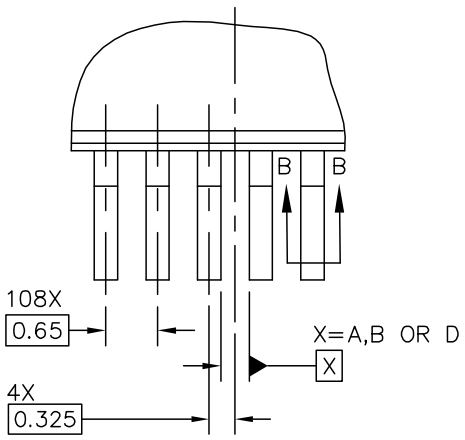
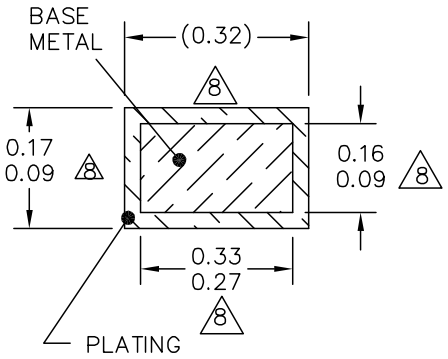


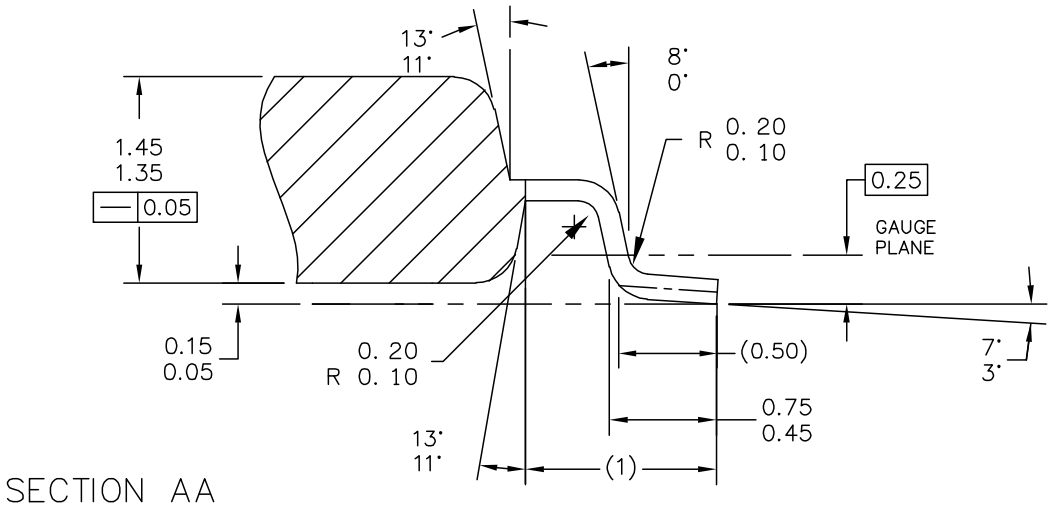
Figure 19. BDM Serial Port AC Timing



VIEW Y



SECTION B–B



SECTION AA

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TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D	REV: O
	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

4 Revision History

Table 41. Revision History

Revision	Description
2 (Jul 2006)	• Updated available packages. • Inserted mechanical drawings. • Corrected signal pinouts and table.
3 (Feb 2007)	• Changed signal names TIN to DTIN and TOUT to DTOUT to match the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added overbars to extend over entire $\overline{\text{UCTSn}}$ and $\overline{\text{URTSn}}$ signal name. • Added revision history. • Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Deleted the “PSTCLK cycle time” row from the “Debug AC Timing Specifications” table. • Added “EPHY Timing” section. • Deleted the “RAM standby supply voltage” entry from Table 19. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • In the “Pin Functions by Primary and Alternate Purpose” table, changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was “—”, is 41). • Updated the “Thermal characteristics” table to include proper thermal resistance values. • Added two tables, “Active Current Consumption Specifications” and “Current Consumption Specifications in Low-Power Modes”, containing the latest current consumption information. • Changed the value of T_j in the “Thermal Characteristics” table (was 105 °C, is 130 °C for all packages). • Added the following note to and above the “Thermal Characteristics” table: “The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.” • Added the value for Ψ_{jt} for the 121MAPBGA package (2.0 °C/W).
4 (May 2007)	• Formatting, layout, spelling, and grammar corrections. • Added load test condition information to the “General Purpose I/O Timing” section. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table.
5 (Sep 2007)	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52232 and MCF52236 devices. • Revised the part number table to include full Freescale orderable part numbers. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in the device reference manual and data sheet. • Added specifications for V_{REFL}, V_{REFH}, and V_{DDA} to the “ADC Parameters” table. • Added several EPHY specifications.
6 (Oct 2007)	• Formatting, layout, spelling, and grammar corrections. • Changed the data sheet classification (was “Product Preview”, is “Advance Information”). • Added the “EzPort Electrical Specifications” section. • Updated the “ESD Protection” section.
7 (Aug 2008)	• Changed document type from Advance Information to Technical Data. • Added supported device list in subtitle. • Removed preliminary text from electrical specifications section as device is fully characterized. • Corrected I_{VREFH}, VREFH current unit from “m” to “mA” in ADC specification table. • Changed V_{OFFSET} from TBD to — in ADC specification table.
8 (Jun 2009)	• Updated Orderable Part Number Summary table to include MCF52233CAL60A, MCF52235CAL60A, and MCF52236AF50A parts

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