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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52232caf50

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  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)
  - System configuration during reset
  - Selects one of three clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic

	1	2	3	4	5	6	7	8	9	10	11
A	TCLK	SDA	SCL	$\overline{\text{IRQ15}}$	$\overline{\text{IRQ14}}$	$\overline{\text{IRQ13}}$	VSSA	VDDA	AN1	AN7	AN5
B	TMS	$\overline{\text{RCON}}$	GPT0	GPT3	PWM5	PWM1	VRL	VRH	AN2	AN6	AN4
C	$\overline{\text{TRST}}$	TDO	TDI	GPT2	PWM7	PWM3	$\overline{\text{IRQ12}}$	AN0	AN3	LNKLED	ACTLED
D	DTIN1	DTIN0	ALLPST	GPT1	VDDX	VDDX	VDD	VDDR	PST2	PST3	SPDLED
E	DDATA3	$\overline{\text{IRQ9}}$	$\overline{\text{IRQ8}}$	VSS	VSS	VDDX	VSS	VDD	PST0	PST1	PHY_RXN
F	DDATA0	DDATA1	DDATA2	VSS	VSS	VSS	VSS	VSS	PHY_VSSRX	PHY_VDDRX	PHY_RXP
G	DTIN2	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	JTAG_EN	VDDX	VDDX	VDDX	PHY_VSSA	PHY_VSSTX	PHY_VDDTX	PHY_TXP
H	DTIN3	$\overline{\text{URTS0}}$	$\overline{\text{URTS1}}$	QSPI_DIN	QSPI_CS1	VDDX	TEST	TXLED	RXLED	PHY_VDDA	PHY_TXN
J	SYNCB	$\overline{\text{UCTS0}}$	$\overline{\text{UCTS1}}$	QSPI_DOUT	QSPI_CS2	$\overline{\text{RSTI}}$	XTAL	$\overline{\text{IRQ1}}$	COLLED	DUPLED	PHY_RBIAS
K	SYNCA	URXD0	URXD1	QSPI_CLK	QSPI_CS3	VDDPLL	VSSPLL	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ11}}$	$\overline{\text{URTS2}}$	URXD2
L	$\overline{\text{IRQ10}}$	UTXD0	UTXD1	QSPI_CS0	$\overline{\text{IRQ4}}$	$\overline{\text{RSTO}}$	EXTAL	$\overline{\text{IRQ3}}$	$\overline{\text{IRQ7}}$	$\overline{\text{UCTS2}}$	UTXD2

Figure 4. 121 MAPBGA Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
Continued Interrupts[3]	IRQ11	—	—	PGP[3]	PSDR[43]	—	Pull-Up[6]	K9	57	41
	IRQ10	—	—	PGP[2]	PSDR[42]	—	Pull-Up[6]	L1	29	—
	IRQ9	—	—	PGP[1]	PSDR[41]	—	Pull-Up[6]	E2	11	—
	IRQ8	—	—	PGP[0]	PSDR[40]	—	Pull-Up	E3	10	—
	IRQ7	—	—	PNQ[7]	Low	—	Pull-Up[6]	L9	56	40
	IRQ6	—	FEC_RXER	PNQ[6]	Low	—	Pull-Up[6]	G3	19	—
	IRQ5	—	FEC_RXD[1]	PNQ[5]	Low	—	Pull-Up[6]	G2	20	—
	IRQ4	—	—	PNQ[4]	Low	—	Pull-Up[6]	L5	41	29
	IRQ3	—	FEC_RXD[2]	PNQ[3]	Low	—	Pull-Up[6]	L8	53	—
	IRQ2	—	FEC_RXD[3]	PNQ[2]	Low	—	Pull-Up[6]	K8	54	—
	IRQ1	SYNCA	PWM1	PNQ[1]	High	—	Pull-Up[6]	J8	55	39
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	G4	18	12
	TCLK/ PSTCLK	CLKOUT	—	—	High	—	Pull-Up[7]	A1	1	1
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up[7]	C3	4	4
	TDO/DSO	—	—	—	High	N/A	—	C2	5	5
	TMS/$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	Pull-Up[7]	B1	2	2
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up	C1	6	6
Mode Selection	$\overline{\text{RCON}}$/EZPCS	—	—	—	N/A	N/A	Pull-Up	B2	3	3
PWM	PWM7	—	—	PTD[3]	PDSR[31]	—	—	C5	104	—
	PWM5	—	—	PTD[2]	PDSR[30]	—	—	B5	103	—
	PWM3	—	—	PTD[1]	PDSR[29]	—	—	C6	100	—
	PWM1	—	—	PTD[0]	PDSR[28]	—	—	B6	99	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
QSPI[3]	QSPI_DIN/ EZPD	CANRX[4]	URXD1	PQS[1]	PDSR[2]	PWOR[4]	—	H4	34	25
	QSPI_DOUT/EZPQ	CANTX[4]	UTXD1	PQS[0]	PDSR[1]	PWOR[5]	—	J4	35	26
	QSPI_CLK/ EZPCK	SCL	URTS1	PQS[2]	PDSR[3]	PWOR[6]	Pull-Up[8]	K4	36	27
	QSPI_CS3	SYNCA	SYNCB	PQS[6]	PDSR[7]	—	—	K5	40	—
	QSPI_CS2	—	FEC_TXCLK	PQS[5]	PDSR[6]	—	—	J5	39	—
	QSPI_CS1	—	FEC_TXEN	PQS[4]	PDSR[5]	—	—	H5	38	—
	QSPI_CS0	SDA	UCTS1	PQS[3]	PDSR[4]	PWOR[7]	Pull-Up[8]	L4	37	28
Reset[9]	RSTI	—	—	—	N/A	N/A	Pull-Up[9]	J6	44	32
	RSTO	—	—	—	high	—	—	L6	46	34
Test	TEST	—	—	—	N/A	N/A	Pull-Down	H7	50	38
Timers, 16-bit[3]	GPT3	FEC_TXD[3]	PWM7	PTA[3]	PDSR[23]	—	Pull-Up[10]	B4	107	75
	GPT2	FEC_TXD[2]	PWM5	PTA[2]	PDSR[22]	—	Pull-Up[10]	C4	108	76
	GPT1	FEC_TXD[1]	PWM3	PTA[1]	PDSR[21]	—	Pull-Up[10]	D4	109	77
	GPT0	FEC_TXER	PWM1	PTA[0]	PDSR[20]	—	Pull-Up[10]	B3	110	78
Timers, 32-bit	DTIN3	DTOUT3	PWM6	PTC[3]	PDSR[19]	—	—	H1	22	14
	DTIN2	DTOUT2	PWM4	PTC[2]	PDSR[18]	—	—	G1	21	13
	DTIN1	DTOUT1	PWM2	PTC[1]	PDSR[17]	—	—	D1	9	9
	DTIN0	DTOUT0	PWM0	PTC[0]	PDSR[16]	—	—	D2	8	8
UART 0[3]	$\overline{\text{UCTS0}}$	CANRX[4]	FEC_RXCLK	PUA[3]	PDSR[11]	—	—	J2	26	18
	$\overline{\text{URTS0}}$	CANTX[4]	FEC_RXDV	PUA[2]	PDSR[10]	—	—	H2	25	17
	URXD0	—	FEC_RXD[0]	PUA[1]	PDSR[9]	PWOR[0]	—	K2	30	21
	UTXD0	—	FEC_CRS	PUA[0]	PDSR[8]	PWOR[1]	—	L2	31	22

1.7 Queued Serial Peripheral Interface (QSPI)

Table 8 describes QSPI signals.

Table 8. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip selects that can be programmed to be active high or low.	O

1.8 Fast Ethernet Controller EPHY Signals

Table 9 describes the Fast Ethernet Controller (FEC) signals.

Table 9. Fast Ethernet Controller (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Twisted Pair Input +	RXP	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Input -	RXN	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Output +	TXN	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Twisted Pair Output -	TXP	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Bias Control Resistor	RBIAS	Connect a 12.4 kΩ (1.0%) external resistor, RBIAS, between the PHY_RBIAS pin and analog ground. Place this resistor as near to the chip pin as possible. Stray capacitance must be kept to less than 10 pF (>50 pF causes instability). No high-speed signals can be permitted in the region of RBIAS.	I
Activity LED	ACT_LED	Indicates when the EPHY is transmitting or receiving	O
Link LED	LINK_LED	Indicates when the EPHY has a valid link	O
Speed LED	SPD_LED	Indicates the speed of the EPHY connection	O
Duplex LED	DUPLED	Indicates the duplex (full or half) of the EPHY connection	O
Collision LED	COLLED	Indicates if the EPHY detects a collision	O
Transmit LED	TXLED	Indicates if the EPHY is transmitting	O
Receive LED	RXLED	Indicates if the EPHY is receiving	O

1.9 I²C I/O Signals

Table 10 describes the I²C serial interface module signals.

Table 10. I²C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I²C interface. Either it is driven by the I²C module when the bus is in master mode or it becomes the clock input when the I²C is in slave mode.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I²C interface.	I/O

1.10 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{\text{UCTS}n}$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}n}$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.11 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN*n*	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT*n*	Programmable output from the DMA timer modules.	O

1.12 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the A-to-D converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise	—
	V_{SSA}		—

1.13 General Purpose Timer Signals

Table 14 describes the General Purpose Timer Signals.

Table 14. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purppose timer module	I/O

1.14 Pulse Width Modulator Signals

Table 15 describes the PWM signals.

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels	O

1.15 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and also to interface to the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset	I
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock. Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint. Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status signals (PST[3:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input. Internally synchronized input that provides data input for the serial communication port to the debug module after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output. Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock. Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, PST, and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be re-enabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]	O

1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK	O

1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.	I
Positive Supply	VDD	These pins supply positive power to the core logic.	I
Ground	VSS	This pin is the negative supply (ground) to the chip.	—

Some of the V_{DD} and V_{SS} pins on the device are only to be used for noise bypass. Figure 5 shows a typical connection diagram. Pay particular attention to those pins which show only capacitor connections. Do not connect power supply voltage directly to these pins.

Table 20. Thermal Characteristics

Characteristic	Symbol	Package[1]	Value	Unit
Junction to ambient, natural convection	θ_{JA}	80-pin LQFP, four-layer board	36.0[2,3]	°C/W
		112-pin LQFP, four-layer board	35.0	
		121 MAPBGA, four-layer board	32	
		80-pin LQFP, one-layer board[1]	49.0[1]	
		121 MAPBGA, one-layer board[1]	56[1]	
		112-pin LQFP, one-layer board[1]	44.0[1]	
Junction to ambient (@200 ft/min)	θ_{JMA}	80-pin LQFP, four-layer board	30.0	°C/W
		112-pin LQFP, four-layer board	29.0	
		121 MAPBGA, four-layer board	28	
		80-pin LQFP, one-layer board[1]	39.0[1]	
		112-pin LQFP, one-layer board[1]	35.0[1]	
		121 MAPBGA, one-layer board[1]	46[1]	
Junction to board	θ_{JB}	80-pin LQFP	22.0[4]	°C/W
		112-pin LQFP	23.0	
		121 MAPBGA, four-layer board	18	
Junction to case	θ_{JC}	80-pin LQFP	6.0[5]	°C/W
		112-pin LQFP	6.0	
		121 MAPBGA	10	
Junction to top of package, natural convection	Ψ_{jt}	80-pin LQFP	2.0[6]	°C/W
		112-pin LQFP	2.0[6]	
		121 MAPBGA	2.0[6]	
Maximum operating junction temperature	T_j	All	130	°C

1 The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

2 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JMA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

Table 23. Active Current Consumption Specifications

Characteristic	Symbol	Typical				Peak	Unit
		Running from SRAM, EPHY Off	Running from Flash, EPHY Off	Running from Flash, EPHY 10BaseT	Running from Flash, EPHY 100BaseT		
Active current, core and I/O PLL @25 MHz PLL @60 MHz	$I_{DDR}+I_{DDX}+I_{DDA}$	 75 130	 82 138	 150 220	 260 310	 290 340	 mA
Analog supply current Normal operation Low-power STOP	I_{DDA}	 20 15	 20 15	 20 15	 20 15	 30 50	 mA μA

Table 24. Current Consumption Specifications in Low-Power Modes[1]

Mode[2]	PLL @25 MHz (typical)[3]	PLL @60 MHz (typical)[3]	PLL @60 MHz (peak)[4]	Unit
STOP mode 3 (STPMD[1:0]=11)	0.2		1.0	mA
STOP mode 2 (STPMD[1:0]=10)	7		—	
STOP mode 1 (STPMD[1:0]=01)	10	12	—	
STOP mode 0 (STPMD[1:0]=00)	10	12	—	
WAIT	16	27	—	
DOZE	16	27	—	
RUN	25	45	—	

1 All values are measured with a 3.30 V power supply.

2 Refer to the “Power Management” chapter in the *MCF52235 ColdFire® Integrated Microcontroller Reference Manual* for more information on low-power modes.

3 These values were obtained with CLKOUT and all peripheral clocks except for the CFM clock disabled prior to entering low-power mode. The tests were performed at room temperature. All code was executed from flash memory; running code from SRAM further reduces power consumption.

4 These values were obtained with CLKOUT and all peripheral clocks enabled. All code was executed from flash memory.

2.4 Phase Lock Loop Electrical Specifications

Table 25. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 0.5 0	 25.0 60.0	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [2] External clock mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 60 60	MHz
Loss of reference frequency [3, 5]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [4, 5]	f_{SCM}	1	5	MHz
Crystal start-up time [5, 6]	t_{cst}	—	10	ms
EXTAL input high voltage Crystal reference External reference	V_{IHEXT}	 V_{DD}- 1.0 2.0	 V_{DD} 3.0[7]	V
EXTAL input low voltage Crystal reference External reference	V_{ILEXT}	 V_{SS} V_{SS}	 1.0 0.8	V
XTAL output high voltage I_{OH} = 1.0 mA	V_{OL}	 V_{DD} –1.0	 —	V
XTAL output low voltage I_{OL} = 1.0 mA	V_{OL}	 —	 0.5	V
XTAL load capacitance[8]		—	—	pF
PLL lock time[5,9]	t_{lpll}	—	500	µs
Power-up to lock time [5, 7,9] With crystal reference Without crystal reference	t_{lplk}	 — —	 10.5 500	 ms µs
Duty cycle of reference [5]	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{sys}
Frequency LOCK range	fLCK	–0.75	0.75	% f_{sys}
CLKOUT period Jitter [5, 6, 8, 10,11], measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over 2 ms interval)	C_{jitter}	 — —	 10 0.01	% f_{sys}

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 All internal registers retain data at 0 Hz.

3 Loss of reference frequency is the reference frequency detected internally that transitions the PLL into self-clocked mode.

4 Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

2.13 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

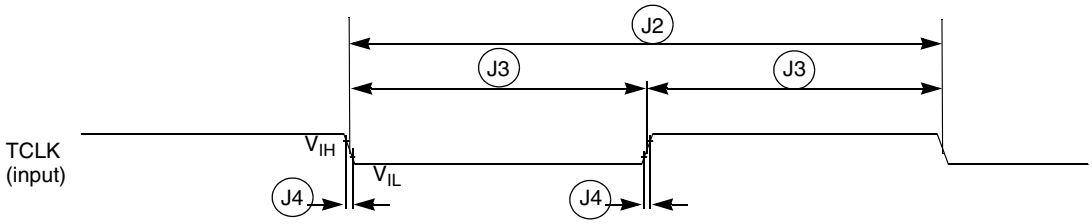

Figure 14. Test Clock Input Timing

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

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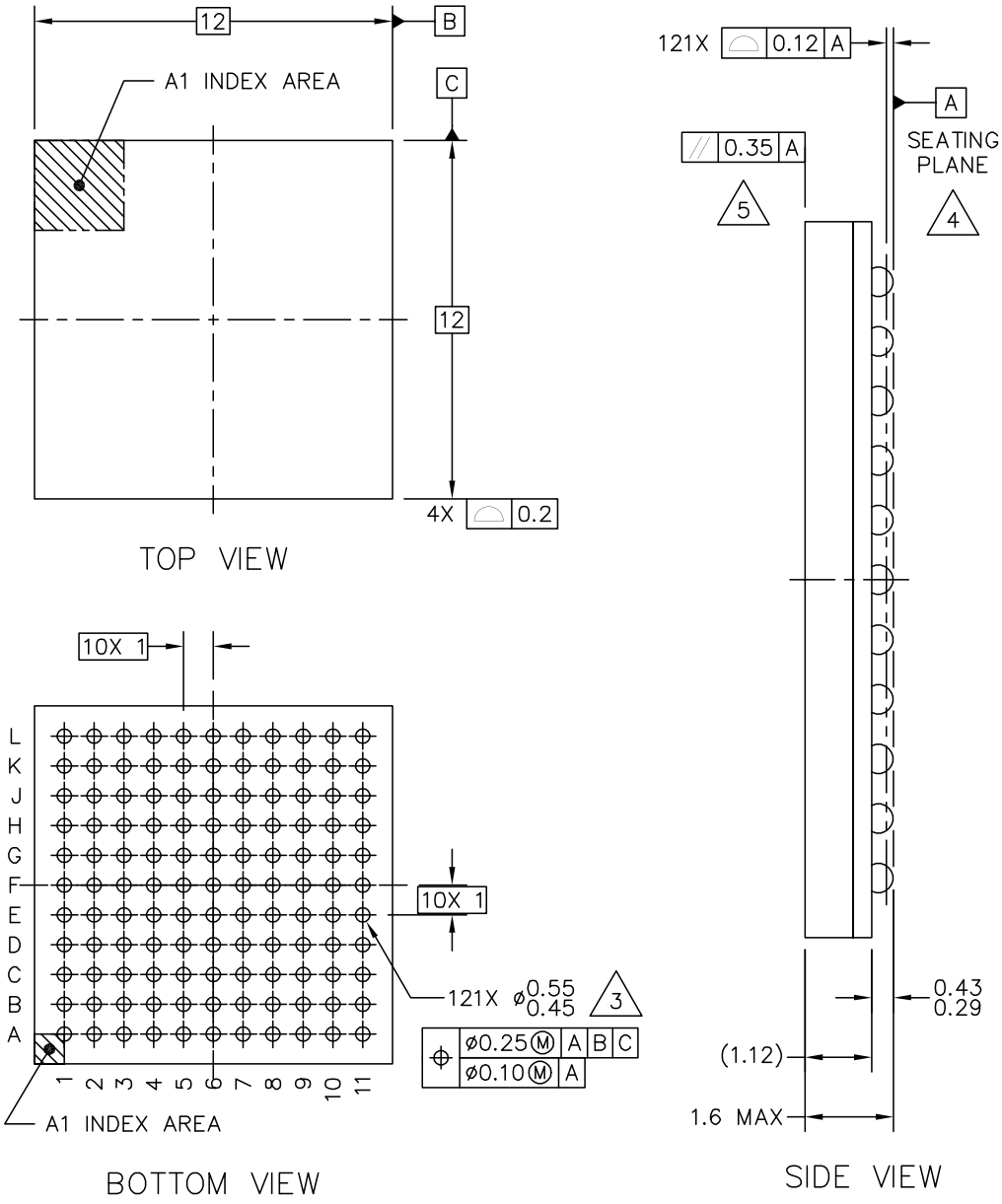
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

3.3 121 MAPBGA Package



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TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D	REV: O
	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D	REV: O
	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

4 Revision History

Table 41. Revision History

Revision	Description
2 (Jul 2006)	• Updated available packages. • Inserted mechanical drawings. • Corrected signal pinouts and table.
3 (Feb 2007)	• Changed signal names TIN to DTIN and TOUT to DTOUT to match the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added overbars to extend over entire $\overline{\text{UCTSn}}$ and $\overline{\text{URTSn}}$ signal name. • Added revision history. • Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Deleted the “PSTCLK cycle time” row from the “Debug AC Timing Specifications” table. • Added “EPHY Timing” section. • Deleted the “RAM standby supply voltage” entry from Table 19. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • In the “Pin Functions by Primary and Alternate Purpose” table, changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was “—”, is 41). • Updated the “Thermal characteristics” table to include proper thermal resistance values. • Added two tables, “Active Current Consumption Specifications” and “Current Consumption Specifications in Low-Power Modes”, containing the latest current consumption information. • Changed the value of T_j in the “Thermal Characteristics” table (was 105 °C, is 130 °C for all packages). • Added the following note to and above the “Thermal Characteristics” table: “The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.” • Added the value for Ψ_{jt} for the 121MAPBGA package (2.0 °C/W).
4 (May 2007)	• Formatting, layout, spelling, and grammar corrections. • Added load test condition information to the “General Purpose I/O Timing” section. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table.
5 (Sep 2007)	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52232 and MCF52236 devices. • Revised the part number table to include full Freescale orderable part numbers. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in the device reference manual and data sheet. • Added specifications for V_{REFL}, V_{REFH}, and V_{DDA} to the “ADC Parameters” table. • Added several EPHY specifications.
6 (Oct 2007)	• Formatting, layout, spelling, and grammar corrections. • Changed the data sheet classification (was “Product Preview”, is “Advance Information”). • Added the “EzPort Electrical Specifications” section. • Updated the “ESD Protection” section.
7 (Aug 2008)	• Changed document type from Advance Information to Technical Data. • Added supported device list in subtitle. • Removed preliminary text from electrical specifications section as device is fully characterized. • Corrected I_{VREFH}, VREFH current unit from “m” to “mA” in ADC specification table. • Changed V_{OFFSET} from TBD to — in ADC specification table.
8 (Jun 2009)	• Updated Orderable Part Number Summary table to include MCF52233CAL60A, MCF52235CAL60A, and MCF52236AF50A parts

Table 41. Revision History (continued)

Revision	Description
8 Sep 2009	• Updated Table 25 — PLL Electrical Specifications.
8 April 2010	• Updated Table 37— EzPort Electrical Specifications
22 Mar 2011	• Updated Table Oscillator and PLL Electrical Specification. In EXTAL input high voltage updated VDD to 3.0
23-Mar-2011	• Changed EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, add a note this value has been updated. • Updated clock generation feature

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