Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	73
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52233caf60

Table of Contents

List of Figures

List of Tables

module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor’s high-speed local bus. The CFM is constructed with four banks of 32 K×16-bit flash arrays to generate 256 Kbytes of 32-bit flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle flash arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash programming interface that allows the flash to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips. This allows easy device programming via Automated Test Equipment or bulk programming tools.

1.2.6 Cryptography Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The MCF52235 incorporates several low-power modes of operation which are entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

1.2.9 UARTs

The MCF52235 has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.24 Package Pinouts

Figure 2 shows the pinout configuration for the 80-pin LQFP.

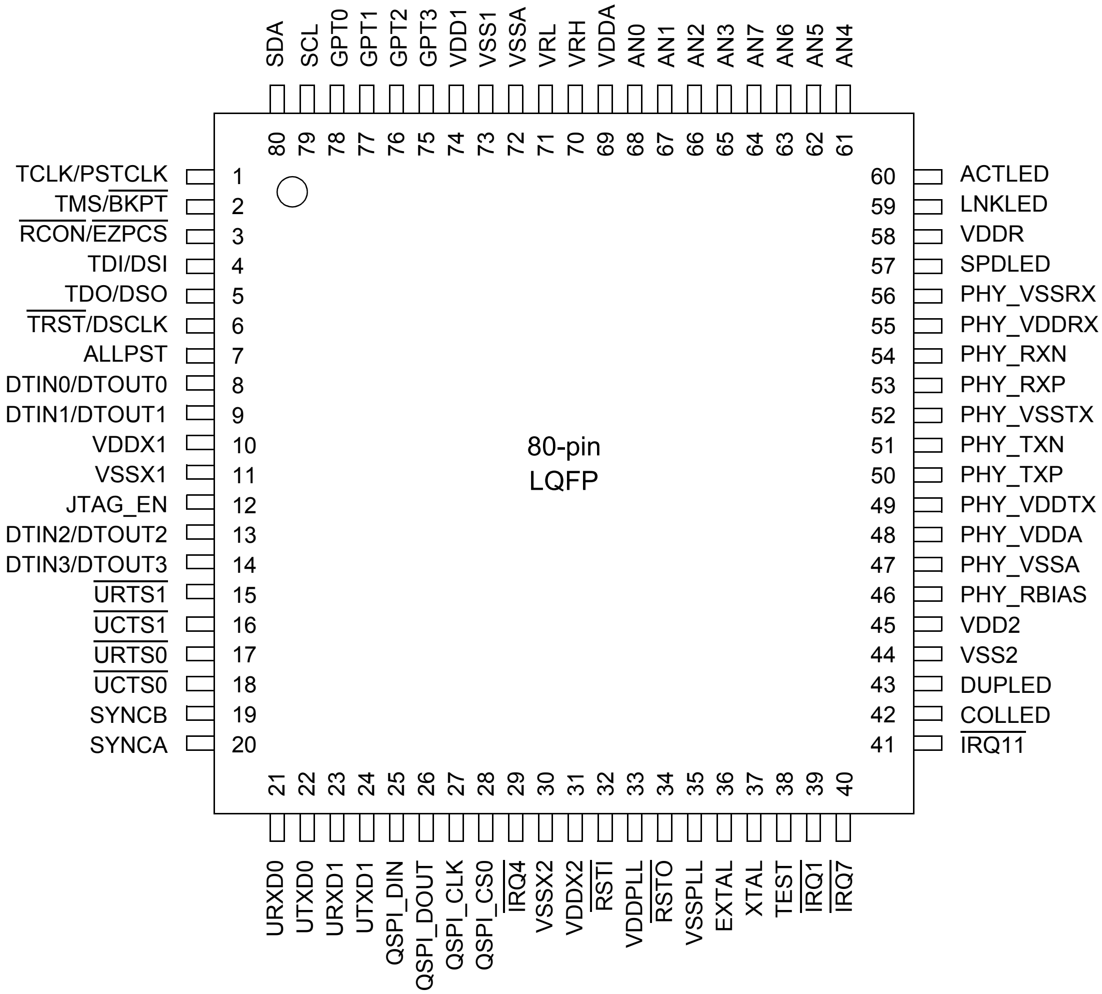


Figure 2. 80-pin LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 112-pin LQFP.

	1	2	3	4	5	6	7	8	9	10	11
A	TCLK	SDA	SCL	$\overline{\text{IRQ15}}$	$\overline{\text{IRQ14}}$	$\overline{\text{IRQ13}}$	VSSA	VDDA	AN1	AN7	AN5
B	TMS	$\overline{\text{RCON}}$	GPT0	GPT3	PWM5	PWM1	VRL	VRH	AN2	AN6	AN4
C	$\overline{\text{TRST}}$	TDO	TDI	GPT2	PWM7	PWM3	$\overline{\text{IRQ12}}$	AN0	AN3	LNKLED	ACTLED
D	DTIN1	DTIN0	ALLPST	GPT1	VDDX	VDDX	VDD	VDDR	PST2	PST3	SPDLED
E	DDATA3	$\overline{\text{IRQ9}}$	$\overline{\text{IRQ8}}$	VSS	VSS	VDDX	VSS	VDD	PST0	PST1	PHY_RXN
F	DDATA0	DDATA1	DDATA2	VSS	VSS	VSS	VSS	VSS	PHY_VSSRX	PHY_VDDRX	PHY_RXP
G	DTIN2	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	JTAG_EN	VDDX	VDDX	VDDX	PHY_VSSA	PHY_VSSTX	PHY_VDDTX	PHY_TXP
H	DTIN3	$\overline{\text{URTS0}}$	$\overline{\text{URTS1}}$	QSPI_DIN	QSPI_CS1	VDDX	TEST	TXLED	RXLED	PHY_VDDA	PHY_TXN
J	SYNCB	$\overline{\text{UCTS0}}$	$\overline{\text{UCTS1}}$	QSPI_DOUT	QSPI_CS2	$\overline{\text{RSTI}}$	XTAL	$\overline{\text{IRQ1}}$	COLLED	DUPLED	PHY_RBIAS
K	SYNCA	URXD0	URXD1	QSPI_CLK	QSPI_CS3	VDDPLL	VSSPLL	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ11}}$	$\overline{\text{URTS2}}$	URXD2
L	$\overline{\text{IRQ10}}$	UTXD0	UTXD1	QSPI_CS0	$\overline{\text{IRQ4}}$	$\overline{\text{RSTO}}$	EXTAL	$\overline{\text{IRQ3}}$	$\overline{\text{IRQ7}}$	$\overline{\text{UCTS2}}$	UTXD2

Figure 4. 121 MAPBGA Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	SecondaryF unction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
ADC[3]	AN7	—	—	PAN[7]	Low	—	—	A10	88	64
	AN6	—	—	PAN[6]	Low	—	—	B10	87	63
	AN5	—	—	PAN[5]	Low	—	—	A11	86	62
	AN4	—	—	PAN[4]	Low	—	—	B11	85	61
	AN3	—	—	PAN[3]	Low	—	—	C9	89	65
	AN2	—	—	PAN[2]	Low	—	—	B9	90	66
	AN1	—	—	PAN[1]	Low	—	—	A9	91	67
	AN0	—	—	PAN[0]	Low	—	—	C8	92	68
	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	K1	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	J1	27	19
	VDDA	—	—	—	N/A	N/A	—	A8	93	69
	VSSA	—	—	—	N/A	N/A	—	A7	96	72
	VRH	—	—	—	N/A	N/A	—	B8	94	70
	VRL	—	—	—	N/A	N/A	—	B7	95	71
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	L7	48	36
	XTAL	—	—	—	N/A	N/A	—	J7	49	37
	VDDPLL[5]	—	—	—	N/A	N/A	—	K6	45	33
	VSSPLL	—	—	—	N/A	N/A	—	K7	47	35
Debug Data	ALLPST	—	—	—	High	—	—	D3	7	7
	DDATA[3:0]	—	—	PDD[7:4]	High	—	—	E1, F3,F2, F1	12,13,16,17	—
	PST[3:0]	—	—	PDD[3:0]	High	—	—	D10, D9, E10, E9	80,79,78,77	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryF unction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
Ethernet LEDs	ACTLED	—	—	PLD[0]	PDSR[32]	PWOR[8]	—	C11	84	60
	COLLED	—	—	PLD[4]	PDSR[36]	PWOR[12]	—	J9	58	42
	DUPLED	—	—	PLD[3]	PDSR[35]	PWOR[11]	—	J10	59	43
	LNKLED	—	—	PLD[1]	PDSR[33]	PWOR[9]	—	C10	83	59
	SPDLED	—	—	PLD[2]	PDSR[34]	PWOR[10]	—	D11	81	57
	RXLED	—	—	PLD[5]	PDSR[37]	PWOR[13]	—	H9	52	—
	TXLED	—	—	PLD[6]	PDSR[38]	PWOR[14]	—	H8	51	—
	VDDR	—	—	—	—	—	—	D8	82	58
Ethernet PHY	PHY_RBIAS	—	—	—	—	—		J11	66	46
	PHY_RXN	—	—	—	—	—		E11	74	54
	PHY_RXP	—	—	—	—	—		F11	73	53
	PHY_TXN	—	—	—	—	—		H11	71	51
	PHY_TXP	—	—	—	—	—		G11	70	50
	PHY_VDDA[5]	—	—	—		N/A		H10	68	48
	PHY_VDDRX[5]	—	—	—		N/A		F10	75	55
	PHY_VDDTX[5]	—	—	—		N/A		G10	69	49
	PHY_VSSA	—	—	—		N/A		G8	67	47
	PHY_VSSRX	—	—	—		N/A		F9	76	56
	PHY_VSSTX	—	—	—		N/A		G9	72	52
I^{2}C	SCL	CANTX[4]	UTXD2	PAS[0]	PDSR[0]	—	Pull-Up[6]	A3	111	79
	SDA	CANRX[4]	URXD2	PAS[1]	PDSR[0]	—	Pull-Up[6]	A2	112	80
Interrupts[3]	IRQ15	—	—	PGP[7]	PSDR[47]	—	Pull-Up[6]	A4	106	—
	IRQ14	—	—	PGP[6]	PSDR[46]	—	Pull-Up[6]	A5	105	—
	IRQ13	—	—	PGP[5]	PSDR[45]	—	Pull-Up[6]	A6	98	—
	IRQ12	—	—	PGP[4]	PSDR[44]	—	Pull-Up[6]	C7	97	—

1.3 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 512 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input.	I
Crystal	XTAL	Crystal oscillator output.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 6 describes signals used in mode selection, Table 6 describes particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device.	—
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

1.6 External Interrupt Signals

Table 7 describes the external interrupt signals.

Table 7. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[15:1]	External interrupt sources.	I

1.7 Queued Serial Peripheral Interface (QSPI)

Table 8 describes QSPI signals.

Table 8. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip selects that can be programmed to be active high or low.	O

1.8 Fast Ethernet Controller EPHY Signals

Table 9 describes the Fast Ethernet Controller (FEC) signals.

Table 9. Fast Ethernet Controller (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Twisted Pair Input +	RXP	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Input -	RXN	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Output +	TXN	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Twisted Pair Output -	TXP	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Bias Control Resistor	RBIAS	Connect a 12.4 kΩ (1.0%) external resistor, RBIAS, between the PHY_RBIAS pin and analog ground. Place this resistor as near to the chip pin as possible. Stray capacitance must be kept to less than 10 pF (>50 pF causes instability). No high-speed signals can be permitted in the region of RBIAS.	I
Activity LED	ACT_LED	Indicates when the EPHY is transmitting or receiving	O
Link LED	LINK_LED	Indicates when the EPHY has a valid link	O
Speed LED	SPD_LED	Indicates the speed of the EPHY connection	O
Duplex LED	DUPLED	Indicates the duplex (full or half) of the EPHY connection	O
Collision LED	COLLED	Indicates if the EPHY detects a collision	O
Transmit LED	TXLED	Indicates if the EPHY is transmitting	O
Receive LED	RXLED	Indicates if the EPHY is receiving	O

1.9 I^{2}C I/O Signals

Table 10 describes the I^{2}C serial interface module signals.

Table 10. I^{2}C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I^{2}C interface. Either it is driven by the I^{2}C module when the bus is in master mode or it becomes the clock input when the I^{2}C is in slave mode.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I^{2}C interface.	I/O

1.10 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{\text{UCTS}n}$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}n}$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.11 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN*n*	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT*n*	Programmable output from the DMA timer modules.	O

1.12 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the A-to-D converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise	—
	V_{SSA}		—

1.13 General Purpose Timer Signals

Table 14 describes the General Purpose Timer Signals.

Table 14. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purppose timer module	I/O

1.14 Pulse Width Modulator Signals

Table 15 describes the PWM signals.

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels	O

1.15 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and also to interface to the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset	I
Test Reset	$\overline{TRST}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1. Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
3. Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
5. The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

Table 20 lists thermal resistance values.

NOTE

The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

The average chip-junction temperature (T_J) in °C can be obtained from

$$T_J = T_A + (P_D \times \Theta_{JMA}) \qquad \textbf{Eqn. 1}$$

where

- T_A = ambient temperature, °C
- Θ_{JMA} = package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{INT} + P_{I/O}$
- P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
- $P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications, PI/O < P_{INT} and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textbf{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \Theta_{JMA} \times P_D^{\ 2} \qquad \textbf{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.2 ESD Protection

Table 21. ESD Protection Characteristics[1]

Characteristic	Symbol	Value	Units
ESD target for Human Body Model	HBM	1500 (ADC and EPHY pins) 2000 (All other pins)	V
ESD target for Charged Device Model	CDM	250	V
HBM circuit description	R_{series}	1500	ohms
	C	100	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (CDM) positive pulses negative pulses	 — —	 3 3	—
Interval of pulses (HBM)	—	1.0	sec
Interval of pulses (CDM)	—	0.2	sec

[1] A device is defined as a failure if the device no longer meets the device specification requirements after exposure to ESD pulses. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.4 Phase Lock Loop Electrical Specifications

Table 25. Oscillator and PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External[1]	 $f_{crystal}$ f_{ext}	 0.5 0	 25.0 60.0	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency [2] External clock mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 60 60	MHz
Loss of reference frequency [3, 5]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [4, 5]	f_{SCM}	1	5	MHz
Crystal start-up time [5, 6]	t_{cst}	—	10	ms
EXTAL input high voltage Crystal reference External reference	V_{IHEXT}	 V_{DD}- 1.0 2.0	 V_{DD} 3.0[7]	V
EXTAL input low voltage Crystal reference External reference	V_{ILEXT}	 V_{SS} V_{SS}	 1.0 0.8	V
XTAL output high voltage I_{OH} = 1.0 mA	V_{OL}	 V_{DD} –1.0	 —	V
XTAL output low voltage I_{OL} = 1.0 mA	V_{OL}	 —	 0.5	V
XTAL load capacitance[8]		—	—	pF
PLL lock time[5,9]	t_{lpll}	—	500	µs
Power-up to lock time [5, 7,9] With crystal reference Without crystal reference	t_{lplk}	 — —	 10.5 500	 ms µs
Duty cycle of reference [5]	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK range	f_{UL}	–1.5	1.5	% f_{sys}
Frequency LOCK range	fLCK	–0.75	0.75	% f_{sys}
CLKOUT period Jitter [5, 6, 8, 10,11], measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over 2 ms interval)	C_{jitter}	 — —	 10 0.01	 % f_{sys}

1 In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

2 All internal registers retain data at 0 Hz.

3 Loss of reference frequency is the reference frequency detected internally that transitions the PLL into self-clocked mode.

4 Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

[7] This value has been updated

[8] Load capacitance determined from crystal manufacturer specifications and include circuit board parasitics.

[9] Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDPLL} are valid to $\overline{RSTO}$ negating. If the crystal oscillator is the reference for the PLL, the crystal start up time must be added to the PLL lock time to determine the total start-up time.

[10] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval

[11] Based on slow system clock of 40 MHz measured at f_{sys} max.

2.5 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, timers, UARTs, FEC, and interrupts. When in GPIO mode, the timing specification for these pins is given in Table 26 and Figure 6.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

Table 26. GPIO Timing

Num	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT high to GPIO output valid	t_{CHPOV}	—	10	ns
G2	CLKOUT high to GPIO output invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO input valid to CLKOUT high	t_{PVCH}	9	—	ns
G4	CLKOUT high to GPIO input invalid	t_{CHPI}	1.5	—	ns

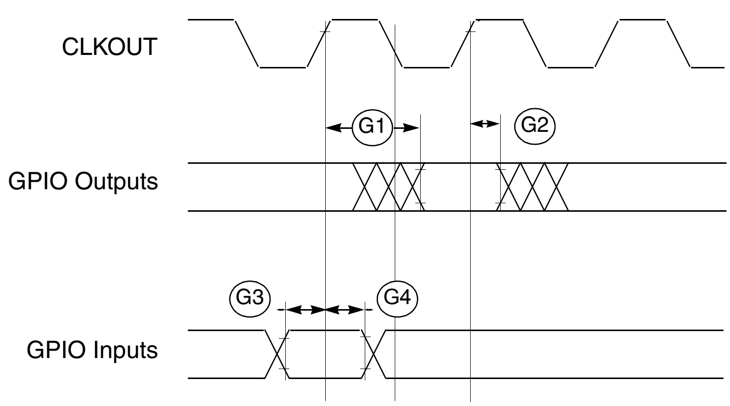


Figure 6. GPIO Timing

2.8 EPHY Parameters

2.8.1 EPHY Timing

Table 30 and Figure 9 show the relevant EPHY timing parameters.

Table 30. EPHY Timing Parameters

Num	Characteristic	Symbol	Value	Unit
E1	EPHY startup time	$t_{Start\text{-}Up}$	360	µs

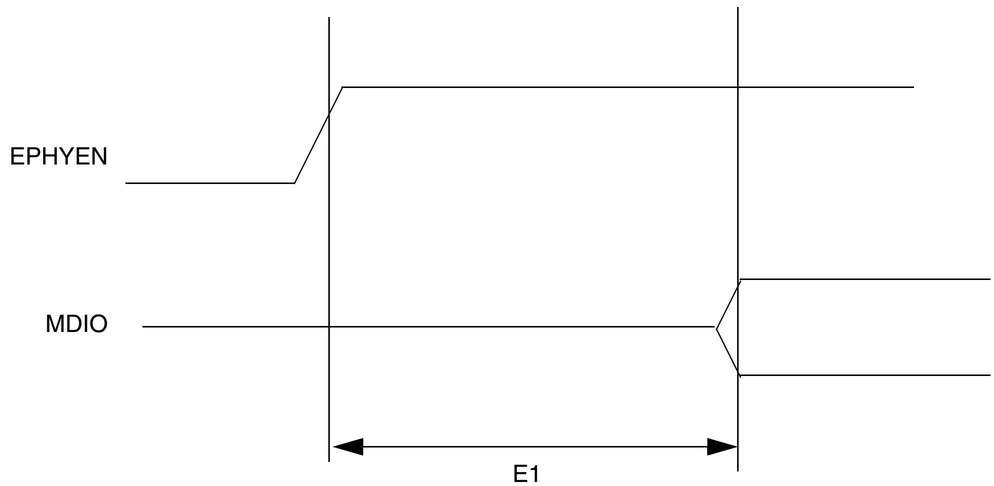


Figure 9. EPHY Timing

2.8.2 10BASE-T SQE (Heartbeat) Timing

Table 31 and Figure 10 show the relevant 10BASE-T SQE (heartbeat) timing parameters.

Table 31. 10BASE-T SQE (Heartbeat) Timing Parameters

Characteristic	Symbol	Min	Typ[1]	Max	Units
COL (SQE) delay after TXEN off	t1	—	1.0	—	µs
COL (SQE) pulse duration	t2	—	1.0	—	µs

[1] Typical values are at 25°C.

Table 35. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 12	—	pF
X_{IN}	Input impedance	—	See Figure 12	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±11	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	—	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	75	—	dB
SINAD	Signal-to-noise plus distortion	—	65	—	dB
ENOB	Effective number OF bits	9.1	10.6	—	Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
3 LSB = Least Significant Bit
4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
5 Includes power-up of ADC and V_{REF}
6 ADC clock cycles
7 The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.9.1 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}\text{-}V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}\text{-}V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an ongoing input current, which is a function of the analog input voltage, V_{REF}, and the ADC clock frequency.

Table 37. EzPort Electrical Specifications (continued)

Name	Characteristic	Min	Max	Unit
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.12 QSPI Electrical Specifications

Table 38 lists QSPI timings.

Table 38. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (input hold)	9	—	ns

The values in Table 38 correspond to Figure 13.

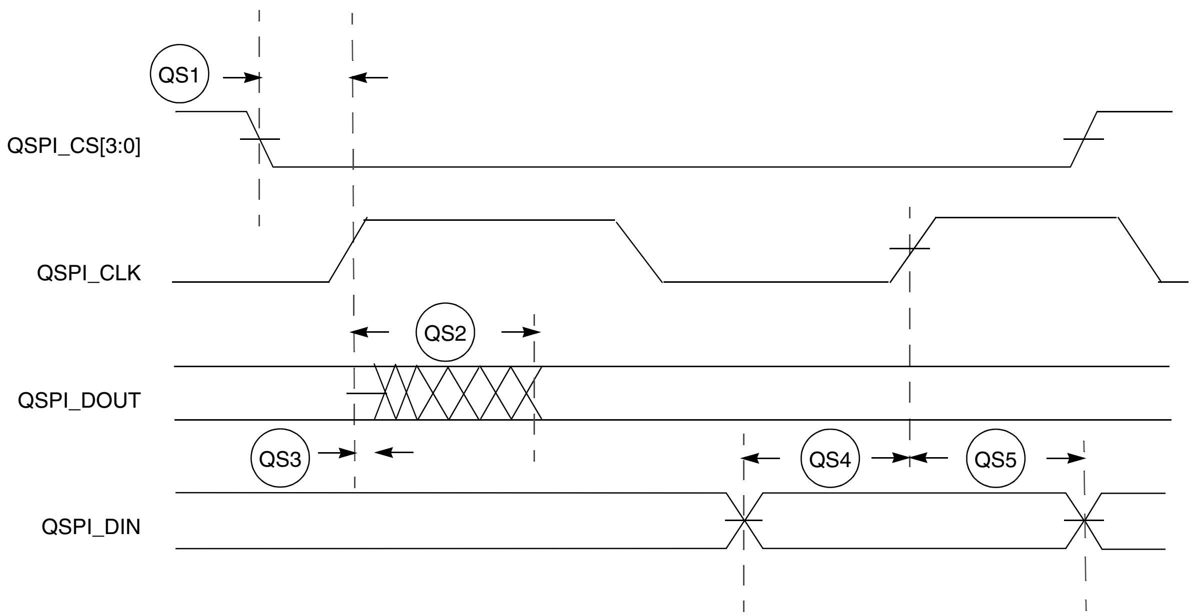
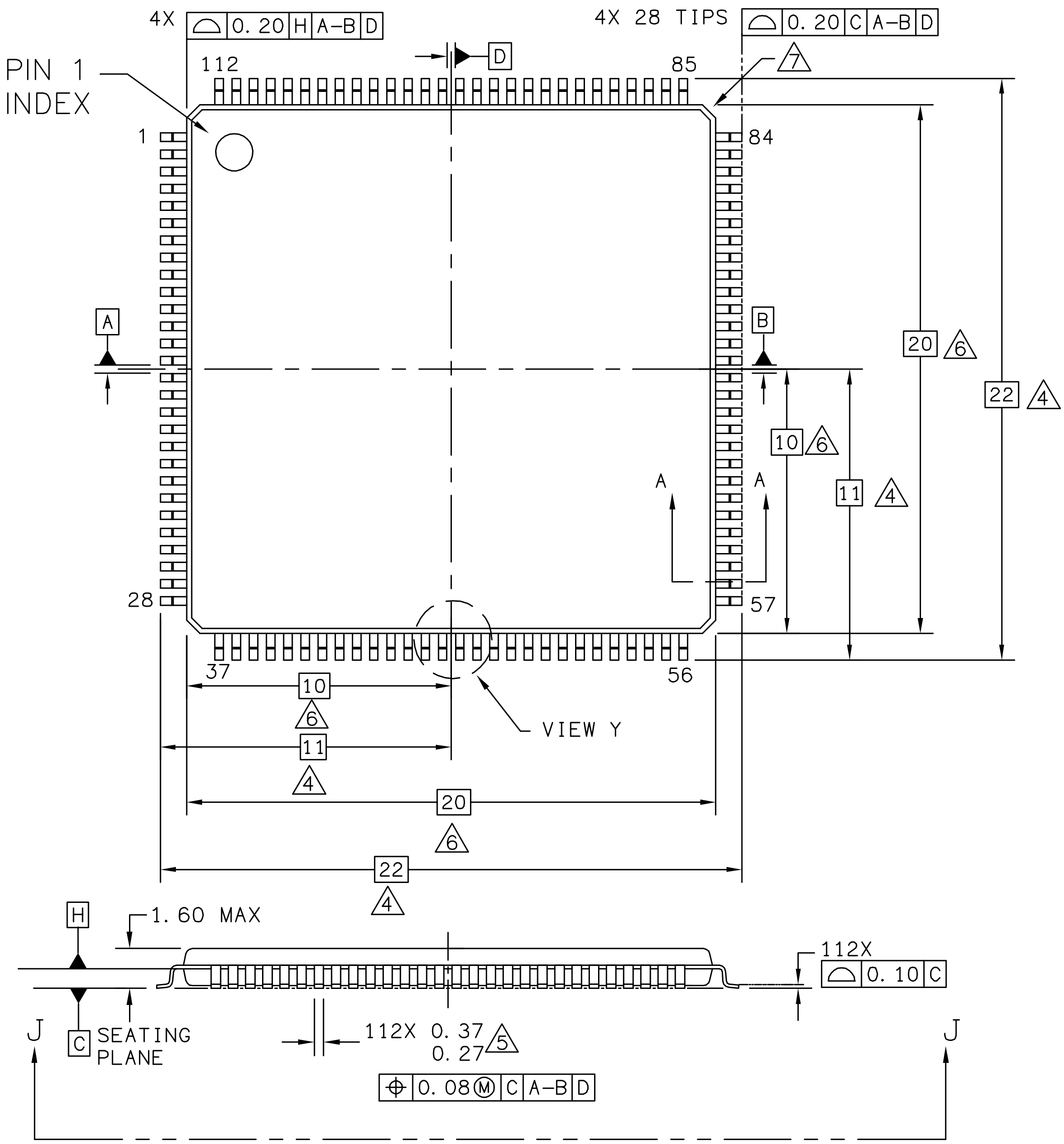


Figure 13. QSPI Timing

3.2 112-pin LQFP Package



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E	
	CASE NUMBER: 987–02	25 MAY 2005	
	STANDARD: JEDEC MS–026 BFA		

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, LOW PROFILE, 121 I/O, 12 X 12 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ARE10645D		REV: O
	CASE NUMBER: 1817–01		15 NOV 2005
	STANDARD: NON–JEDEC		