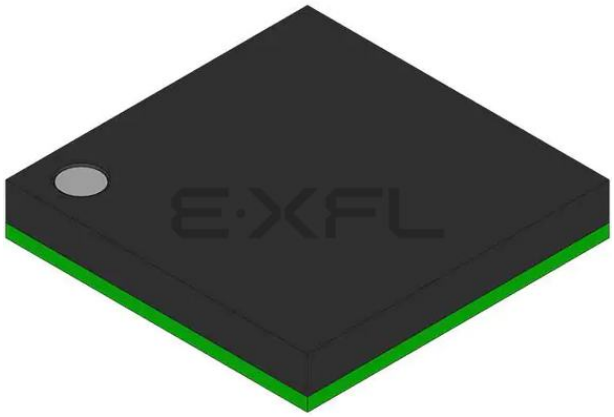

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LBGA
Supplier Device Package	121-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52234cvm60j

1.1 Block Diagram

The MCF52235 (or its variants) comes in 80- and 112-pin low-profile quad flat pack packages (LQFP) and a 121 MAPBGA, and operates in single-chip mode only. Figure 1 shows a top-level block diagram of the MCF52235.

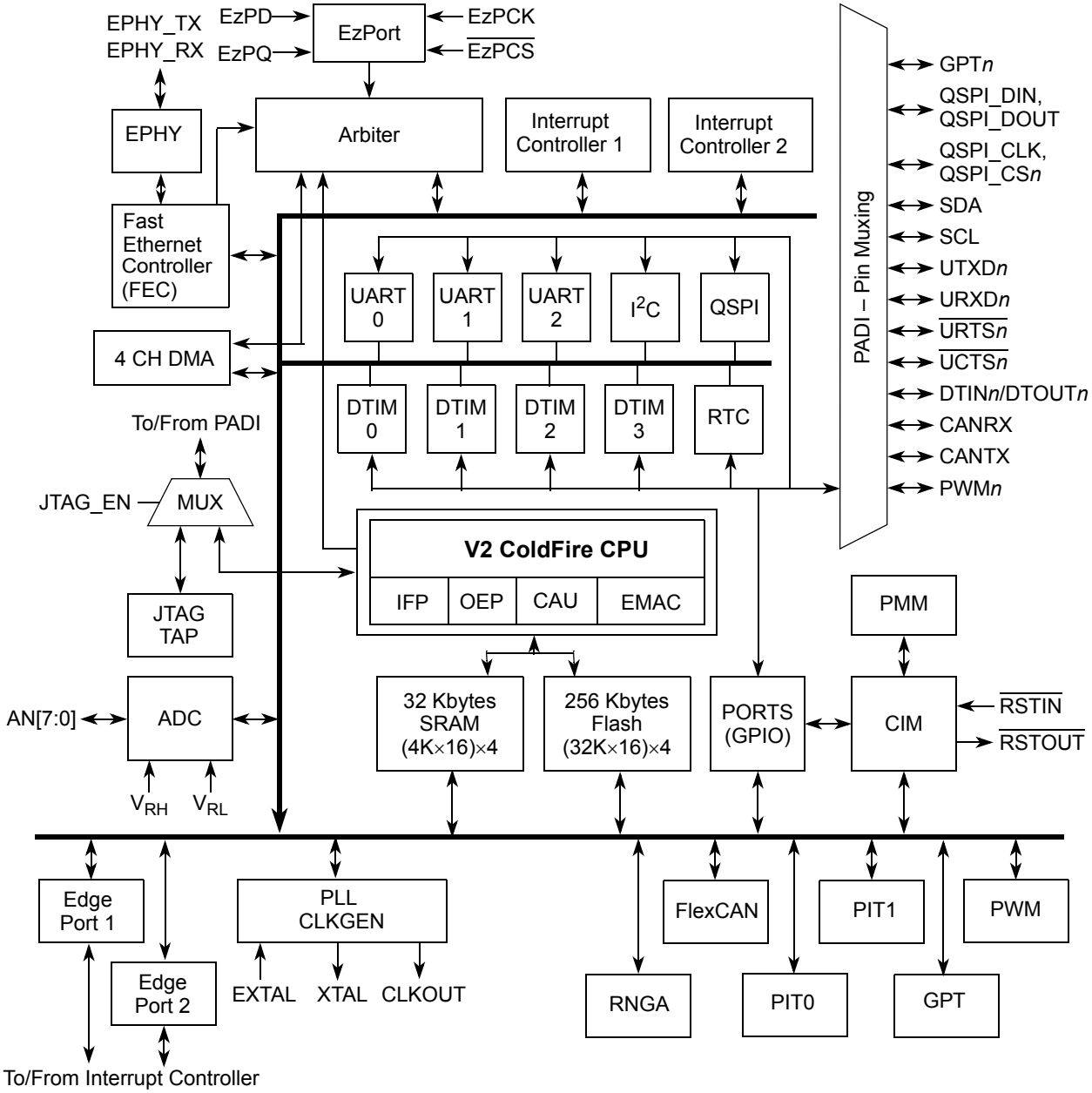


Figure 1. MCF52235 Block Diagram

1.2 Features

This document contains information on a new product under development. Freescale reserves the right to change or discontinue this product without notice. Specifications and information herein are subject to change without notice.

- Four 32-bit DMA timers
  - 17-ns resolution at 60 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timers
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low power mode support
- Clock Generation Features
  - Crystal input
  - On-chip PLL
  - Provides clock for integrated EPHY
- Dual Interrupt Controllers (INTC0/INTC1)
  - Support for multiple interrupt sources organized as follows:
    - Fully-programmable interrupt sources for each peripheral
    - 7 fixed-level interrupt sources
    - Seven external interrupt signals

  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)
  - System configuration during reset
  - Selects one of three clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic

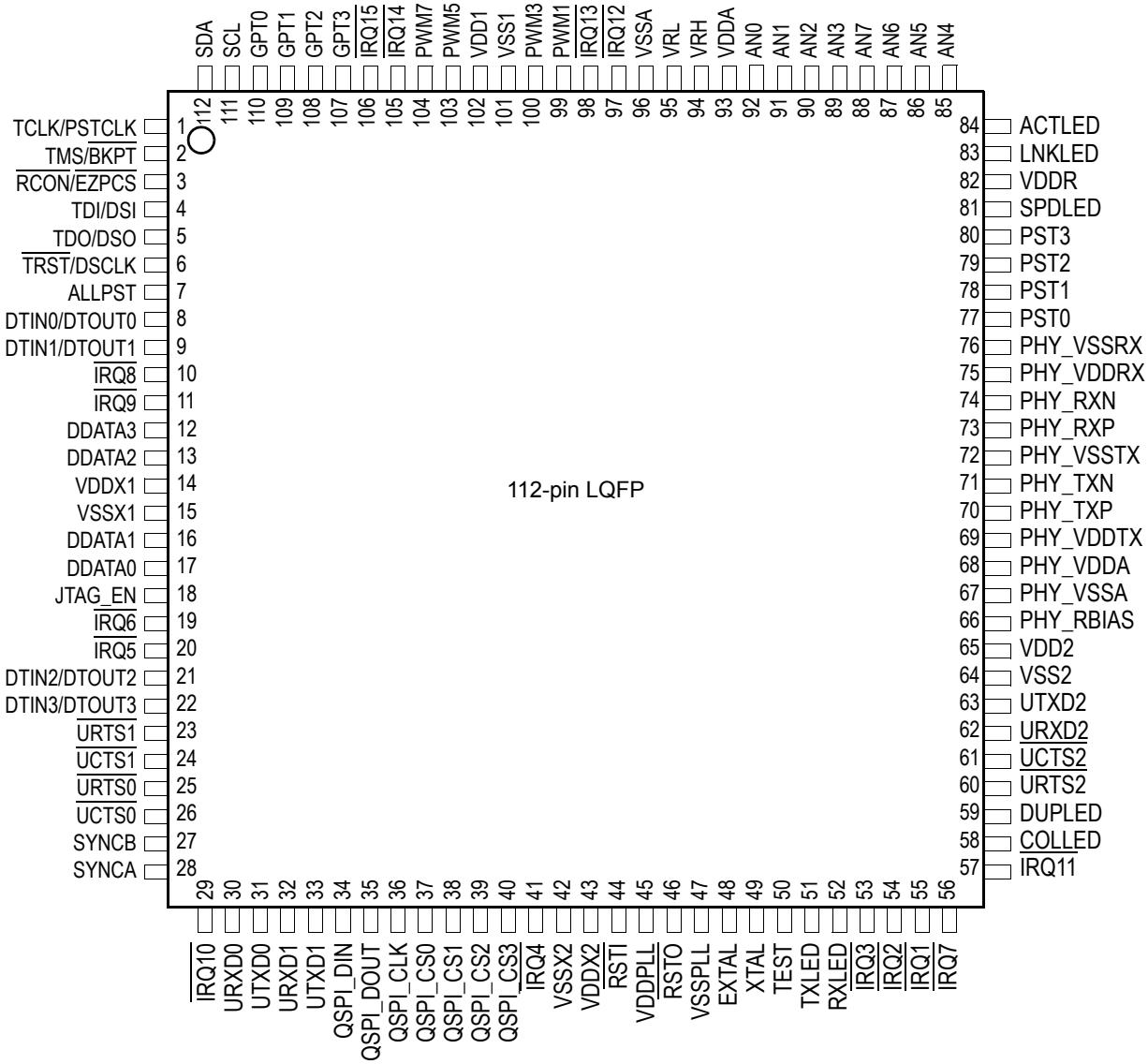


Figure 3. 112-pin LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 121 MAPBGA.

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
ADC[3]	AN7	—	—	PAN[7]	Low	—	—	A10	88	64
	AN6	—	—	PAN[6]	Low	—	—	B10	87	63
	AN5	—	—	PAN[5]	Low	—	—	A11	86	62
	AN4	—	—	PAN[4]	Low	—	—	B11	85	61
	AN3	—	—	PAN[3]	Low	—	—	C9	89	65
	AN2	—	—	PAN[2]	Low	—	—	B9	90	66
	AN1	—	—	PAN[1]	Low	—	—	A9	91	67
	AN0	—	—	PAN[0]	Low	—	—	C8	92	68
	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	K1	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	J1	27	19
	VDDA	—	—	—	N/A	N/A	—	A8	93	69
	VSSA	—	—	—	N/A	N/A	—	A7	96	72
	VRH	—	—	—	N/A	N/A	—	B8	94	70
	VRL	—	—	—	N/A	N/A	—	B7	95	71
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	L7	48	36
	XTAL	—	—	—	N/A	N/A	—	J7	49	37
	VDDPLL[5]	—	—	—	N/A	N/A	—	K6	45	33
	VSSPLL	—	—	—	N/A	N/A	—	K7	47	35
Debug Data	ALLPST	—	—	—	High	—	—	D3	7	7
	DDATA[3:0]	—	—	PDD[7:4]	High	—	—	E1, F3,F2, F1	12,13,16,17	—
	PST[3:0]	—	—	PDD[3:0]	High	—	—	D10, D9, E10, E9	80,79,78,77	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
Continued Interrupts[3]	IRQ11	—	—	PGP[3]	PSDR[43]	—	Pull-Up[6]	K9	57	41
	IRQ10	—	—	PGP[2]	PSDR[42]	—	Pull-Up[6]	L1	29	—
	IRQ9	—	—	PGP[1]	PSDR[41]	—	Pull-Up[6]	E2	11	—
	IRQ8	—	—	PGP[0]	PSDR[40]	—	Pull-Up	E3	10	—
	IRQ7	—	—	PNQ[7]	Low	—	Pull-Up[6]	L9	56	40
	IRQ6	—	FEC_RXER	PNQ[6]	Low	—	Pull-Up[6]	G3	19	—
	IRQ5	—	FEC_RXD[1]	PNQ[5]	Low	—	Pull-Up[6]	G2	20	—
	IRQ4	—	—	PNQ[4]	Low	—	Pull-Up[6]	L5	41	29
	IRQ3	—	FEC_RXD[2]	PNQ[3]	Low	—	Pull-Up[6]	L8	53	—
	IRQ2	—	FEC_RXD[3]	PNQ[2]	Low	—	Pull-Up[6]	K8	54	—
	IRQ1	SYNCA	PWM1	PNQ[1]	High	—	Pull-Up[6]	J8	55	39
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	G4	18	12
	TCLK/ PSTCLK	CLKOUT	—	—	High	—	Pull-Up[7]	A1	1	1
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up[7]	C3	4	4
	TDO/DSO	—	—	—	High	N/A	—	C2	5	5
	TMS/$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	Pull-Up[7]	B1	2	2
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up	C1	6	6
Mode Selection	$\overline{\text{RCON}}$/EZPCS	—	—	—	N/A	N/A	Pull-Up	B2	3	3
PWM	PWM7	—	—	PTD[3]	PDSR[31]	—	—	C5	104	—
	PWM5	—	—	PTD[2]	PDSR[30]	—	—	B5	103	—
	PWM3	—	—	PTD[1]	PDSR[29]	—	—	C6	100	—
	PWM1	—	—	PTD[0]	PDSR[28]	—	—	B6	99	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
UART 1[3]	$\overline{\text{UCTS1}}$	SYNCA	URXD2	PUB[3]	PDSR[15]	—	—	J3	24	16
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	PUB[2]	PDSR[14]	—	—	H3	23	15
	URXD1	—	FEC_TXD[0]	PUB[1]	PDSR[13]	PWOR[2]	—	K3	32	23
	UTXD1	—	FEC_COL	PUB[0]	PDSR[12]	PWOR[3]	—	L3	33	24
UART 2	$\overline{\text{UCTS2}}$	—	—	PUC[3]	PDSR[27]	—	—	L10	61	—
	$\overline{\text{URTS2}}$	—	—	PUC[2]	PDSR[26]	—	—	K10	60	—
	URXD2	—	—	PUC[1]	PDSR[25]	—	—	K11	62	—
	UTXD2	—	—	PUC[0]	PDSR[24]	—	—	L11	63	—
FlexCAN	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	—	27	19
VDD[5,11]	VDD	—	—	—	N/A	N/A	—	D7, E8	65,102	45,74
VDDX	VDDX	—	—	—	N/A	N/A	—	D5, D6, E6, G5, G6, G7, H6	14, 43	10, 31
VSS	VSS	—	—	—	N/A	N/A	—	E4, E5, E7,F4, F5, F6, F7, F8	64,101	44,73
VSSX	VSSX	—	—	—	N/A	N/A	—	—	15, 42	11, 30

1 The PDSR and PSSR registers are described in Chapter 14, "General Purpose I/O Module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The use of an external PHY limits ADC, interrupt, and QSPI functionality. It also disables the UART0/1 and timer pins.
4 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
5 The VDD1, VDD2, VDDPLL, and PHY_VDD pins are for decoupling only and should not have power directly applied to them.
6 For primary and GPIO functions only.
7 Only when JTAG mode is enabled.
8 For secondary and GPIO functions only.
9 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the Ethernet PHY.

1.9 I²C I/O Signals

Table 10 describes the I²C serial interface module signals.

Table 10. I²C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I²C interface. Either it is driven by the I²C module when the bus is in master mode or it becomes the clock input when the I²C is in slave mode.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I²C interface.	I/O

1.10 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{\text{UCTS}n}$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}n}$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.11 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN*n*	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT*n*	Programmable output from the DMA timer modules.	O

2.3 DC Electrical Specifications

Table 22. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, input-only pins	I_{in}	–1.0	1.0	µA
High impedance (off-state) leakage current $V_{in} = V_{DD}$ or V_{SS}, all input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Weak internal pull-up device current, tested at V_{IL} max.[2]	I_{APU}	–10	–130	µA
Input capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load capacitance[4] Low drive strength High drive strength	C_L		 25 50	pF
DC injection current [3, 5, 6, 7] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single pin limit Total MCU limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10	 1.0 10	mA

1 Refer to Table 25 for additional PLL specifications.

2 Refer to Table 3 for pins with internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

5 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, the system clock is not present during the power-up sequence until the PLL has attained lock.

Table 23. Active Current Consumption Specifications

Characteristic	Symbol	Typical				Peak	Unit
		Running from SRAM, EPHY Off	Running from Flash, EPHY Off	Running from Flash, EPHY 10BaseT	Running from Flash, EPHY 100BaseT		
Active current, core and I/O PLL @25 MHz PLL @60 MHz	$I_{DDR}+I_{DDX}+I_{DDA}$	 75 130	 82 138	 150 220	 260 310	 290 340	 mA
Analog supply current Normal operation Low-power STOP	I_{DDA}	 20 15	 20 15	 20 15	 20 15	 30 50	 mA μA

Table 24. Current Consumption Specifications in Low-Power Modes[1]

Mode[2]	PLL @25 MHz (typical)[3]	PLL @60 MHz (typical)[3]	PLL @60 MHz (peak)[4]	Unit
STOP mode 3 (STPMD[1:0]=11)	0.2		1.0	mA
STOP mode 2 (STPMD[1:0]=10)	7		—	
STOP mode 1 (STPMD[1:0]=01)	10	12	—	
STOP mode 0 (STPMD[1:0]=00)	10	12	—	
WAIT	16	27	—	
DOZE	16	27	—	
RUN	25	45	—	

1 All values are measured with a 3.30 V power supply.

2 Refer to the “Power Management” chapter in the *MCF52235 ColdFire® Integrated Microcontroller Reference Manual* for more information on low-power modes.

3 These values were obtained with CLKOUT and all peripheral clocks except for the CFM clock disabled prior to entering low-power mode. The tests were performed at room temperature. All code was executed from flash memory; running code from SRAM further reduces power consumption.

4 These values were obtained with CLKOUT and all peripheral clocks enabled. All code was executed from flash memory.

2.6 Reset Timing

Table 27. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT high	t_{RVCH}	9	—	ns
R2	CLKOUT high to $\overline{\text{RSTI}}$ input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT high to $\overline{\text{RSTO}}$ valid	t_{CHROV}	—	10	ns

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Therefore, $\overline{\text{RSTI}}$ must be held a minimum of 100ns.

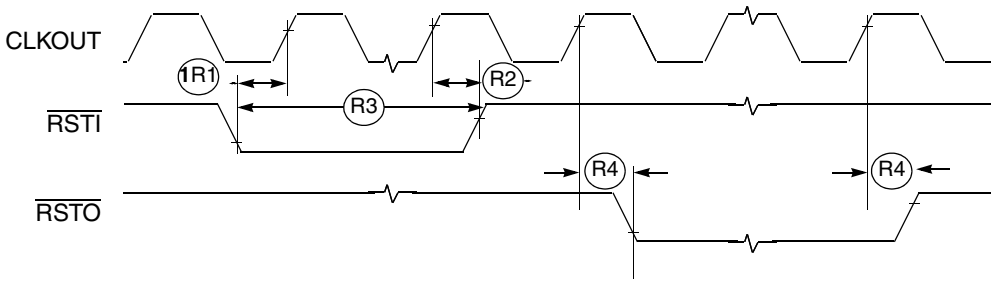


Figure 7. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.7 I²C Input/Output Timing Specifications

Table 28 lists specifications for the I²C input timing parameters shown in Figure 8.

Table 28. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 × t_{CYC}	—	ns
I2	Clock low period	8 × t_{CYC}	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4 × t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 × t_{CYC}	—	ns
I9	Stop condition setup time	2 × t_{CYC}	—	ns

Table 29 lists specifications for the I²C output timing parameters shown in Figure 8.

2.8 EPHY Parameters

2.8.1 EPHY Timing

Table 30 and Figure 9 show the relevant EPHY timing parameters.

Table 30. EPHY Timing Parameters

Num	Characteristic	Symbol	Value	Unit
E1	EPHY startup time	$t_{Start-Up}$	360	µs

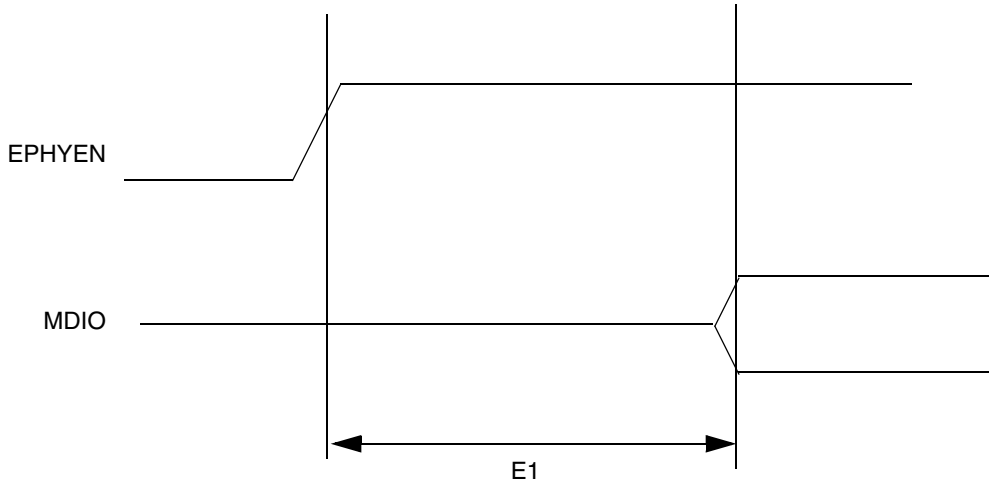


Figure 9. EPHY Timing

2.8.2 10BASE-T SQE (Heartbeat) Timing

Table 31 and Figure 10 show the relevant 10BASE-T SQE (heartbeat) timing parameters.

Table 31. 10BASE-T SQE (Heartbeat) Timing Parameters

Characteristic	Symbol	Min	Typ[1]	Max	Units
COL (SQE) delay after TXEN off	t1	—	1.0	—	µs
COL (SQE) pulse duration	t2	—	1.0	—	µs

[1] Typical values are at 25°C.

Table 35. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 12	—	pF
X_{IN}	Input impedance	—	See Figure 12	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±11	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	—	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	75	—	dB
SINAD	Signal-to-noise plus distortion	—	65	—	dB
ENOB	Effective number OF bits	9.1	10.6	—	Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

5 Includes power-up of ADC and V_{REF}

6 ADC clock cycles

7 The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.9.1 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an ongoing input current, which is a function of the analog input voltage, V_{REF}, and the ADC clock frequency.

Table 37. EzPort Electrical Specifications (continued)

Name	Characteristic	Min	Max	Unit
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.12 QSPI Electrical Specifications

Table 38 lists QSPI timings.

Table 38. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (input hold)	9	—	ns

The values in Table 38 correspond to Figure 13.

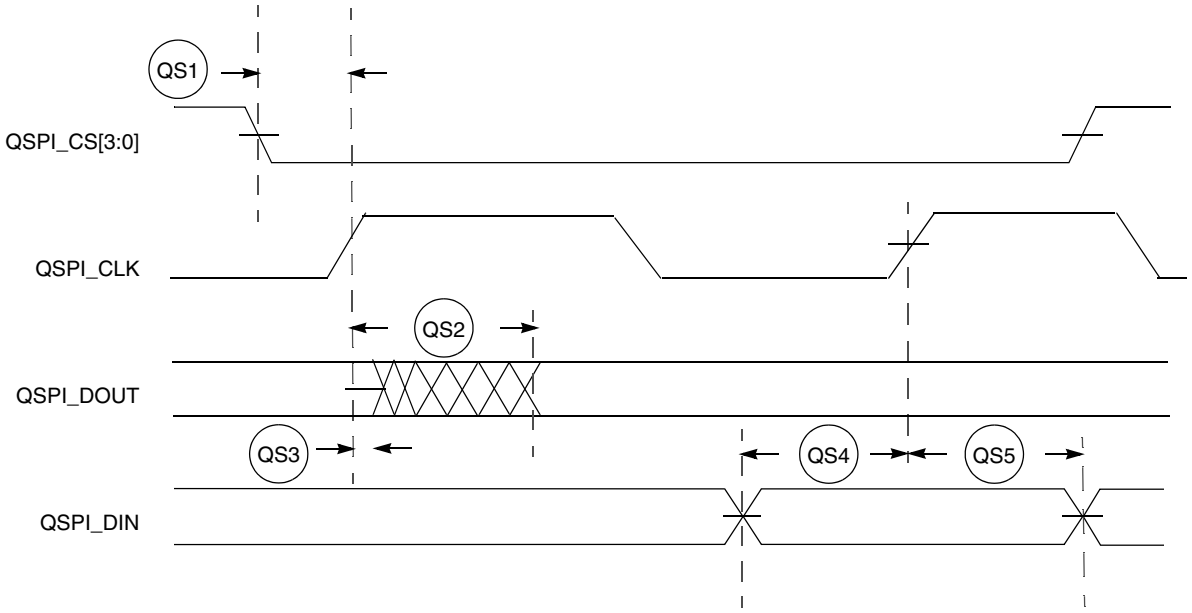


Figure 13. QSPI Timing

2.13 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

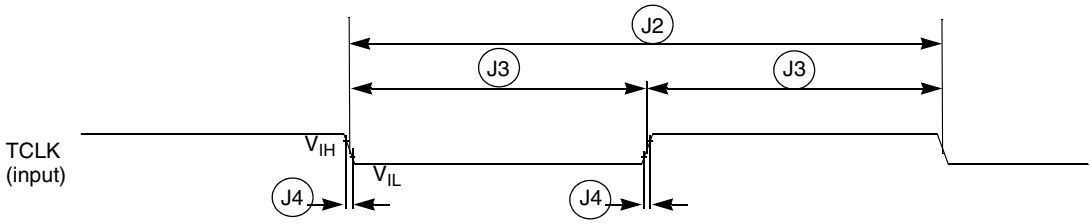


Figure 14. Test Clock Input Timing

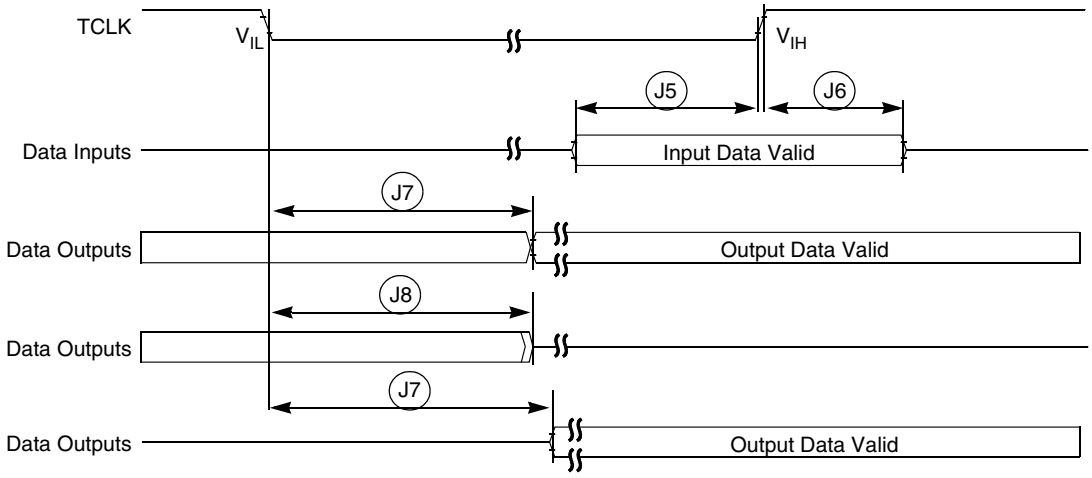


Figure 15. Boundary Scan (JTAG) Timing

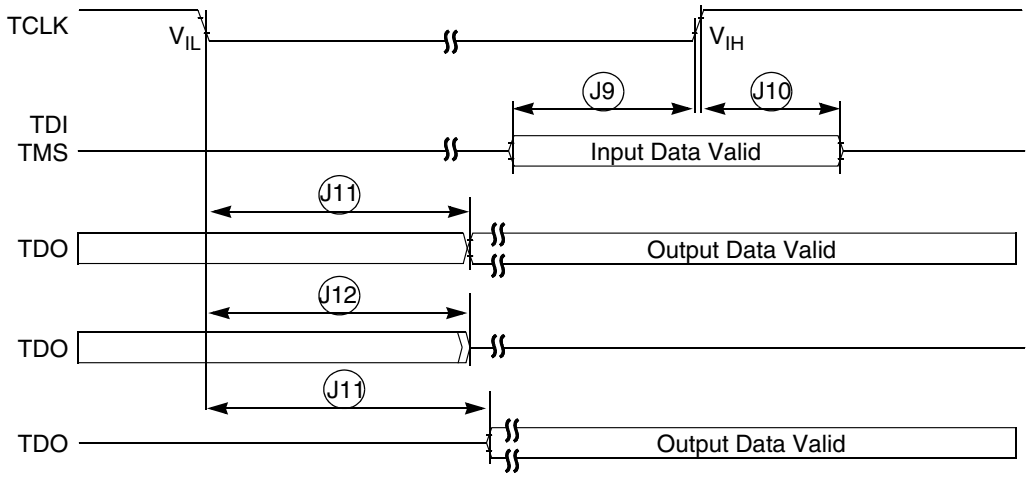


Figure 16. Test Access Port Timing

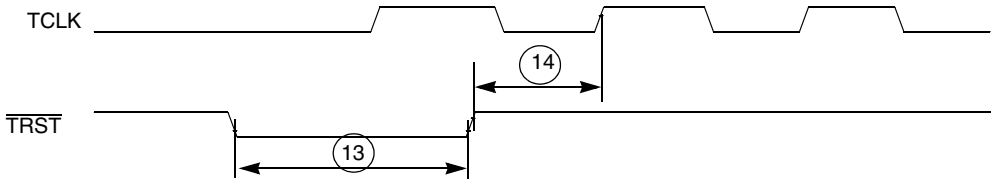
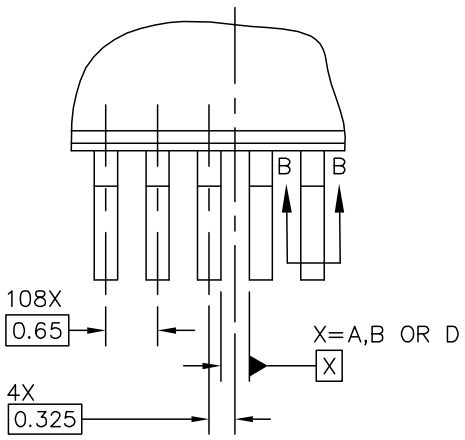
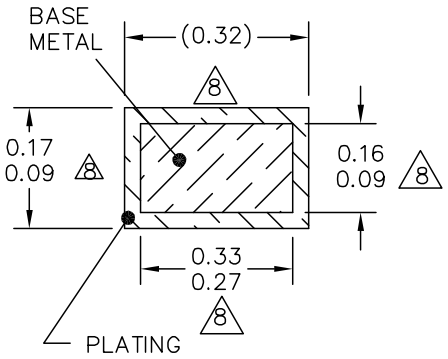


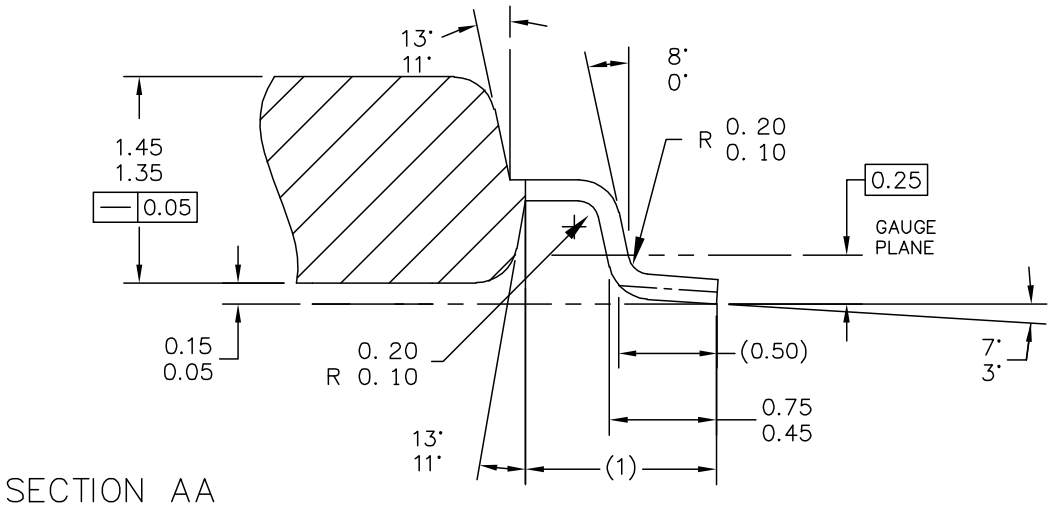
Figure 17. TRST Timing



VIEW Y



SECTION B–B



SECTION AA

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TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 112LD LQFP, 20 X 20 X 1.4 PKG, 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

4 Revision History

Table 41. Revision History

Revision	Description
2 (Jul 2006)	• Updated available packages. • Inserted mechanical drawings. • Corrected signal pinouts and table.
3 (Feb 2007)	• Changed signal names TIN to DTIN and TOUT to DTOUT to match the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Added overbars to extend over entire $\overline{\text{UCTSn}}$ and $\overline{\text{URTSn}}$ signal name. • Added revision history. • Formatting, layout, spelling, and grammar corrections. • Updated block diagram and feature information to match Revision 3 of the MCF52235 ColdFire® Integrated Microcontroller Reference Manual. • Deleted the “PSTCLK cycle time” row from the “Debug AC Timing Specifications” table. • Added “EPHY Timing” section. • Deleted the “RAM standby supply voltage” entry from Table 19. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • In the “Pin Functions by Primary and Alternate Purpose” table, changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was “—”, is 41). • Updated the “Thermal characteristics” table to include proper thermal resistance values. • Added two tables, “Active Current Consumption Specifications” and “Current Consumption Specifications in Low-Power Modes”, containing the latest current consumption information. • Changed the value of T_j in the “Thermal Characteristics” table (was 105 °C, is 130 °C for all packages). • Added the following note to and above the “Thermal Characteristics” table: “The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.” • Added the value for Ψ_{jt} for the 121MAPBGA package (2.0 °C/W).
4 (May 2007)	• Formatting, layout, spelling, and grammar corrections. • Added load test condition information to the “General Purpose I/O Timing” section. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table.
5 (Sep 2007)	• Formatting, layout, spelling, and grammar corrections. • Added information about the MCF52232 and MCF52236 devices. • Revised the part number table to include full Freescale orderable part numbers. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in the device reference manual and data sheet. • Added specifications for V_{REFL}, V_{REFH}, and V_{DDA} to the “ADC Parameters” table. • Added several EPHY specifications.
6 (Oct 2007)	• Formatting, layout, spelling, and grammar corrections. • Changed the data sheet classification (was “Product Preview”, is “Advance Information”). • Added the “EzPort Electrical Specifications” section. • Updated the “ESD Protection” section.
7 (Aug 2008)	• Changed document type from Advance Information to Technical Data. • Added supported device list in subtitle. • Removed preliminary text from electrical specifications section as device is fully characterized. • Corrected I_{VREFH}, VREFH current unit from “m” to “mA” in ADC specification table. • Changed V_{OFFSET} from TBD to — in ADC specification table.
8 (Jun 2009)	• Updated Orderable Part Number Summary table to include MCF52233CAL60A, MCF52235CAL60A, and MCF52236AF50A parts

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