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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 60MHz |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 73 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LQFP |
| Supplier Device Package | 112-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52235cal60 |

# 1 MCF52235 Family Configurations

**Table 1. MCF52235 Family Configurations**

| Module | 52230 | 52231 | 52232 | 52233 | 52234 | 52235 | 52236 |
|---|---|---|---|---|---|---|---|
| Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit) | • | • | • | • | • | • | • |
| System Clock (MHz) | 60 | 60 | 50 | 60 | 60 | 60 | 50 |
| Performance (Dhrystone 2.1 MIPS) | 56 | 56 | 46 | 56 | 56 | 56 | 46 |
| Flash / Static RAM (SRAM) | 128/32 Kbytes | 128/32 Kbytes | 128/32 Kbytes | 256/32 Kbytes | 256/32 Kbytes | 256/32 Kbytes | 256/32 Kbytes |
| Interrupt Controllers (INTC0/INTC1) | • | • | • | • | • | • | • |
| Fast Analog-to-Digital Converter (ADC) | • | • | • | • | • | • | • |
| Random Number Generator and Crypto Acceleration Unit (CAU) | — | — | — | — | — | • | — |
| FlexCAN 2.0B Module | — | • | — | — | • | • | — |
| Fast Ethernet Controller (FEC) with on-chip interface (EPHY) | • | • | • | • | • | • | • |
| Four-channel Direct-Memory Access (DMA) | • | • | • | • | • | • | • |
| Software Watchdog Timer (WDT) | • | • | • | • | • | • | • |
| Programmable Interrupt Timer | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Four-Channel General Purpose Timer | • | • | • | • | • | • | • |
| 32-bit DMA Timers | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| QSPI | • | • | • | • | • | • | • |
| UART(s) | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| $I^2C$ | • | • | • | • | • | • | • |
| Eight/Four-channel 8/16-bit PWM Timer | • | • | • | • | • | • | • |
| General Purpose I/O Module (GPIO) | • | • | • | • | • | • | • |
| Chip Configuration and Reset Controller Module | • | • | • | • | • | • | • |
| Background Debug Mode (BDM) | • | • | • | • | • | • | • |
| JTAG - IEEE 1149.1 Test Access Port[1] | • | • | • | • | • | • | • |
| Package | 80 LQFP 112 LQFP | 80 LQFP 112 LQFP | 80 LQFP | 80 LQFP 112 LQFP | 112 LQFP 121 MAPBGA | 112 LQFP 121 MAPBGA | 80 LQFP |

[1] The full debug/trace interface is available only on the 112- and 121-pin packages. A reduced debug interface is bonded on the 80-pin package.

  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)
  - System configuration during reset
  - Selects one of three clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

### 1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic

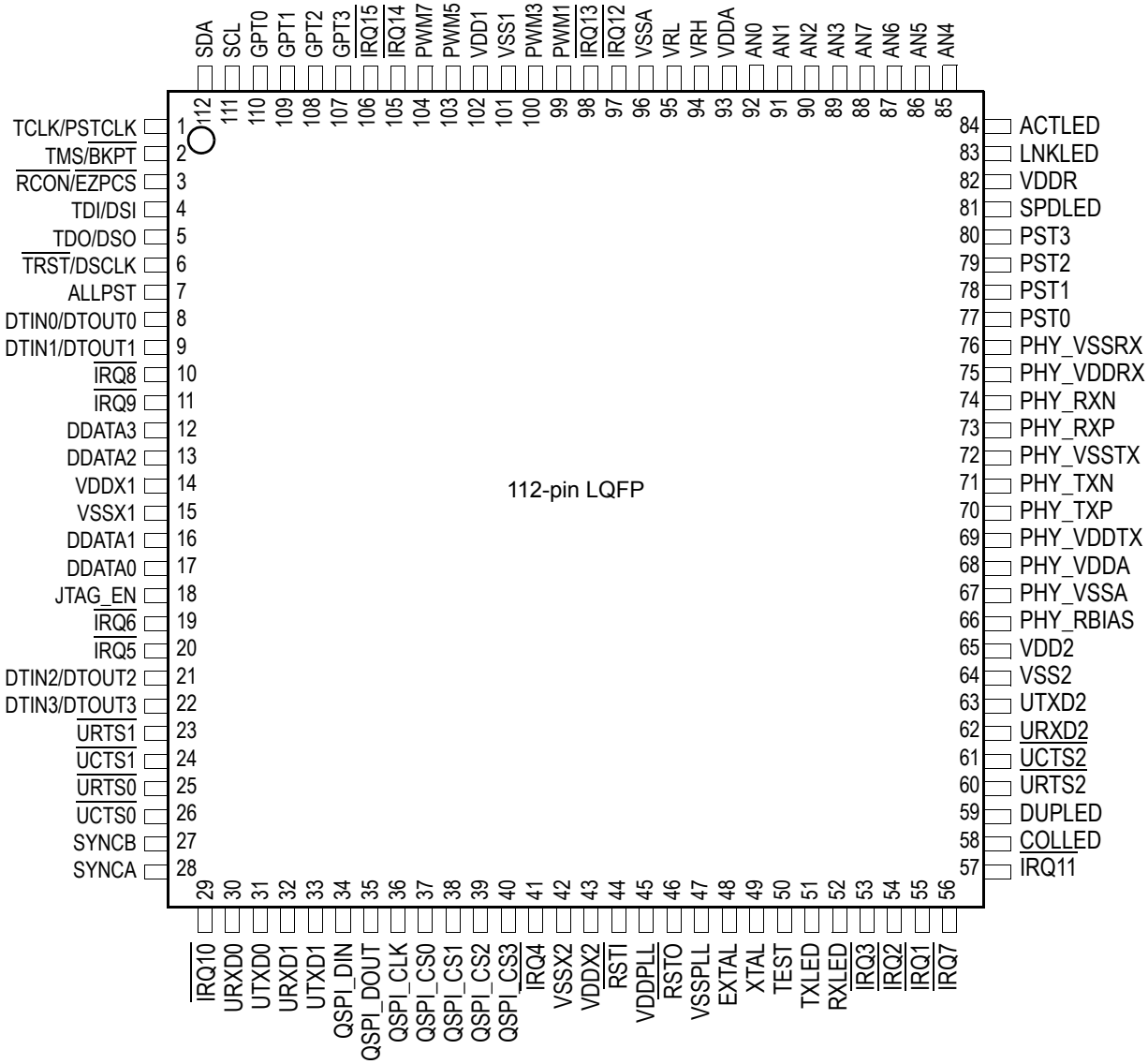



**Figure 3. 112-pin LQFP Pin Assignments**

Figure 4 shows the pinout configuration for the 121 MAPBGA.

**Table 3. Pin Functions by Primary and Alternate Purpose**

| Pin Group | Primary Function | SecondaryFunction | Tertiary Function | Quaternary Function | Drive Strength/ Control[1] | Wired OR Control | Pull-up/ Pull-down[2] | Pin on 121 MAPBGA | Pin on 112 LQFP | Pin on 80 LQFP |
|---|---|---|---|---|---|---|---|---|---|---|
| ADC[3] | AN7 | — | — | PAN[7] | Low | — | — | A10 | 88 | 64 |
| | AN6 | — | — | PAN[6] | Low | — | — | B10 | 87 | 63 |
| | AN5 | — | — | PAN[5] | Low | — | — | A11 | 86 | 62 |
| | AN4 | — | — | PAN[4] | Low | — | — | B11 | 85 | 61 |
| | AN3 | — | — | PAN[3] | Low | — | — | C9 | 89 | 65 |
| | AN2 | — | — | PAN[2] | Low | — | — | B9 | 90 | 66 |
| | AN1 | — | — | PAN[1] | Low | — | — | A9 | 91 | 67 |
| | AN0 | — | — | PAN[0] | Low | — | — | C8 | 92 | 68 |
| | SYNCA | CANTX[4] | FEC_MDIO | PAS[3] | PDSR[39] | — | — | K1 | 28 | 20 |
| | SYNCB | CANRX[4] | FEC_MDC | PAS[2] | PDSR[39] | — | — | J1 | 27 | 19 |
| | VDDA | — | — | — | N/A | N/A | — | A8 | 93 | 69 |
| | VSSA | — | — | — | N/A | N/A | — | A7 | 96 | 72 |
| | VRH | — | — | — | N/A | N/A | — | B8 | 94 | 70 |
| | VRL | — | — | — | N/A | N/A | — | B7 | 95 | 71 |
| Clock Generation | EXTAL | — | — | — | N/A | N/A | — | L7 | 48 | 36 |
| | XTAL | — | — | — | N/A | N/A | — | J7 | 49 | 37 |
| | VDDPLL[5] | — | — | — | N/A | N/A | — | K6 | 45 | 33 |
| | VSSPLL | — | — | — | N/A | N/A | — | K7 | 47 | 35 |
| Debug Data | ALLPST | — | — | — | High | — | — | D3 | 7 | 7 |
| | DDATA[3:0] | — | — | PDD[7:4] | High | — | — | E1, F3,F2, F1 | 12,13,16,17 | — |
| | PST[3:0] | — | — | PDD[3:0] | High | — | — | D10, D9, E10, E9 | 80,79,78,77 | — |

**Table 3. Pin Functions by Primary and Alternate Purpose (continued)**

| Pin Group | Primary Function | SecondaryFunction | Tertiary Function | Quaternary Function | Drive Strength/ Control[1] | Wired OR Control | Pull-up/ Pull-down[2] | Pin on 121 MAPBGA | Pin on 112 LQFP | Pin on 80 LQFP |
|---|---|---|---|---|---|---|---|---|---|---|
| Ethernet LEDs | ACTLED | — | — | PLD[0] | PDSR[32] | PWOR[8] | — | C11 | 84 | 60 |
| | COLLED | — | — | PLD[4] | PDSR[36] | PWOR[12] | — | J9 | 58 | 42 |
| | DUPLED | — | — | PLD[3] | PDSR[35] | PWOR[11] | — | J10 | 59 | 43 |
| | LNKLED | — | — | PLD[1] | PDSR[33] | PWOR[9] | — | C10 | 83 | 59 |
| | SPDLED | — | — | PLD[2] | PDSR[34] | PWOR[10] | — | D11 | 81 | 57 |
| | RXLED | — | — | PLD[5] | PDSR[37] | PWOR[13] | — | H9 | 52 | — |
| | TXLED | — | — | PLD[6] | PDSR[38] | PWOR[14] | — | H8 | 51 | — |
| | VDDR | — | — | — | — | — | — | D8 | 82 | 58 |
| Ethernet PHY | PHY_RBIAS | — | — | — | — | — | | J11 | 66 | 46 |
| | PHY_RXN | — | — | — | — | — | | E11 | 74 | 54 |
| | PHY_RXP | — | — | — | — | — | | F11 | 73 | 53 |
| | PHY_TXN | — | — | — | — | — | | H11 | 71 | 51 |
| | PHY_TXP | — | — | — | — | — | | G11 | 70 | 50 |
| | PHY_VDDA[5] | — | — | — | | N/A | | H10 | 68 | 48 |
| | PHY_VDDRX[5] | — | — | — | | N/A | | F10 | 75 | 55 |
| | PHY_VDDTX[5] | — | — | — | | N/A | | G10 | 69 | 49 |
| | PHY_VSSA | — | — | — | | N/A | | G8 | 67 | 47 |
| | PHY_VSSRX | — | — | — | | N/A | | F9 | 76 | 56 |
| | PHY_VSSTX | — | — | — | | N/A | | G9 | 72 | 52 |
| $I^2C$ | SCL | CANTX[4] | UTXD2 | PAS[0] | PDSR[0] | — | Pull-Up[6] | A3 | 111 | 79 |
| | SDA | CANRX[4] | URXD2 | PAS[1] | PDSR[0] | — | Pull-Up[6] | A2 | 112 | 80 |
| Interrupts[3] | IRQ15 | — | — | PGP[7] | PSDR[47] | — | Pull-Up[6] | A4 | 106 | — |
| | IRQ14 | — | — | PGP[6] | PSDR[46] | — | Pull-Up[6] | A5 | 105 | — |
| | IRQ13 | — | — | PGP[5] | PSDR[45] | — | Pull-Up[6] | A6 | 98 | — |
| | IRQ12 | — | — | PGP[4] | PSDR[44] | — | Pull-Up[6] | C7 | 97 | — |

**Table 3. Pin Functions by Primary and Alternate Purpose (continued)**

| Pin Group | Primary Function | SecondaryFunction | Tertiary Function | Quaternary Function | Drive Strength/ Control[1] | Wired OR Control | Pull-up/ Pull-down[2] | Pin on 121 MAPBGA | Pin on 112 LQFP | Pin on 80 LQFP |
|---|---|---|---|---|---|---|---|---|---|---|
| Continued Interrupts[3] | IRQ11 | — | — | PGP[3] | PSDR[43] | — | Pull-Up[6] | K9 | 57 | 41 |
| | IRQ10 | — | — | PGP[2] | PSDR[42] | — | Pull-Up[6] | L1 | 29 | — |
| | IRQ9 | — | — | PGP[1] | PSDR[41] | — | Pull-Up[6] | E2 | 11 | — |
| | IRQ8 | — | — | PGP[0] | PSDR[40] | — | Pull-Up | E3 | 10 | — |
| | IRQ7 | — | — | PNQ[7] | Low | — | Pull-Up[6] | L9 | 56 | 40 |
| | IRQ6 | — | FEC_RXER | PNQ[6] | Low | — | Pull-Up[6] | G3 | 19 | — |
| | IRQ5 | — | FEC_RXD[1] | PNQ[5] | Low | — | Pull-Up[6] | G2 | 20 | — |
| | IRQ4 | — | — | PNQ[4] | Low | — | Pull-Up[6] | L5 | 41 | 29 |
| | IRQ3 | — | FEC_RXD[2] | PNQ[3] | Low | — | Pull-Up[6] | L8 | 53 | — |
| | IRQ2 | — | FEC_RXD[3] | PNQ[2] | Low | — | Pull-Up[6] | K8 | 54 | — |
| | IRQ1 | SYNCA | PWM1 | PNQ[1] | High | — | Pull-Up[6] | J8 | 55 | 39 |
| JTAG/BDM | JTAG_EN | — | — | — | N/A | N/A | Pull-Down | G4 | 18 | 12 |
| | TCLK/ PSTCLK | CLKOUT | — | — | High | — | Pull-Up[7] | A1 | 1 | 1 |
| | TDI/DSI | — | — | — | N/A | N/A | Pull-Up[7] | C3 | 4 | 4 |
| | TDO/DSO | — | — | — | High | N/A | — | C2 | 5 | 5 |
| | TMS/$\overline{\text{BKPT}}$ | — | — | — | N/A | N/A | Pull-Up[7] | B1 | 2 | 2 |
| | TRST/DSCLK | — | — | — | N/A | N/A | Pull-Up | C1 | 6 | 6 |
| Mode Selection | $\overline{\text{RCON}}$/EZPCS | — | — | — | N/A | N/A | Pull-Up | B2 | 3 | 3 |
| PWM | PWM7 | — | — | PTD[3] | PDSR[31] | — | — | C5 | 104 | — |
| | PWM5 | — | — | PTD[2] | PDSR[30] | — | — | B5 | 103 | — |
| | PWM3 | — | — | PTD[1] | PDSR[29] | — | — | C6 | 100 | — |
| | PWM1 | — | — | PTD[0] | PDSR[28] | — | — | B6 | 99 | — |

**Table 3. Pin Functions by Primary and Alternate Purpose (continued)**

| Pin Group | Primary Function | SecondaryFunction | Tertiary Function | Quaternary Function | Drive Strength/ Control[1] | Wired OR Control | Pull-up/ Pull-down[2] | Pin on 121 MAPBGA | Pin on 112 LQFP | Pin on 80 LQFP |
|---|---|---|---|---|---|---|---|---|---|---|
| UART 1[3] | $\overline{\text{UCTS1}}$ | SYNCA | URXD2 | PUB[3] | PDSR[15] | — | — | J3 | 24 | 16 |
| | $\overline{\text{URTS1}}$ | SYNCB | UTXD2 | PUB[2] | PDSR[14] | — | — | H3 | 23 | 15 |
| | URXD1 | — | FEC_TXD[0] | PUB[1] | PDSR[13] | PWOR[2] | — | K3 | 32 | 23 |
| | UTXD1 | — | FEC_COL | PUB[0] | PDSR[12] | PWOR[3] | — | L3 | 33 | 24 |
| UART 2 | $\overline{\text{UCTS2}}$ | — | — | PUC[3] | PDSR[27] | — | — | L10 | 61 | — |
| | $\overline{\text{URTS2}}$ | — | — | PUC[2] | PDSR[26] | — | — | K10 | 60 | — |
| | URXD2 | — | — | PUC[1] | PDSR[25] | — | — | K11 | 62 | — |
| | UTXD2 | — | — | PUC[0] | PDSR[24] | — | — | L11 | 63 | — |
| FlexCAN | SYNCA | CANTX[4] | FEC_MDIO | PAS[3] | PDSR[39] | — | — | — | 28 | 20 |
| | SYNCB | CANRX[4] | FEC_MDC | PAS[2] | PDSR[39] | — | — | — | 27 | 19 |
| VDD[5,11] | VDD | — | — | — | N/A | N/A | — | D7, E8 | 65,102 | 45,74 |
| VDDX | VDDX | — | — | — | N/A | N/A | — | D5, D6, E6, G5, G6, G7, H6 | 14, 43 | 10, 31 |
| VSS | VSS | — | — | — | N/A | N/A | — | E4, E5, E7,F4, F5, F6, F7, F8 | 64,101 | 44,73 |
| VSSX | VSSX | — | — | — | N/A | N/A | — | — | 15, 42 | 11, 30 |

1 The PDSR and PSSR registers are described in Chapter 14, "General Purpose I/O Module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The use of an external PHY limits ADC, interrupt, and QSPI functionality. It also disables the UART0/1 and timer pins.
4 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
5 The VDD1, VDD2, VDDPLL, and PHY_VDD pins are for decoupling only and should not have power directly applied to them.
6 For primary and GPIO functions only.
7 Only when JTAG mode is enabled.
8 For secondary and GPIO functions only.
9 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the Ethernet PHY.

## 1.3 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

**Table 4. Reset Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Reset In | $\overline{\text{RSTI}}$ | Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals. | I |
| Reset Out | $\overline{\text{RSTO}}$ | Driven low for 512 CPU clocks after the reset source has deasserted. | O |

## 1.4 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

**Table 5. PLL and Clock Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| External Clock In | EXTAL | Crystal oscillator or external clock input. | I |
| Crystal | XTAL | Crystal oscillator output. | O |
| Clock Out | CLKOUT | This output signal reflects the internal system clock. | O |

## 1.5 Mode Selection

Table 6 describes signals used in mode selection, Table 6 describes particular clocking modes.

**Table 6. Mode Selection Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Reset Configuration | RCON | The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device. | — |
| Test | TEST | Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions. | I |

## 1.6 External Interrupt Signals

Table 7 describes the external interrupt signals.

**Table 7. External Interrupt Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| External Interrupts | $\overline{\text{IRQ}}$[15:1] | External interrupt sources. | I |

## 1.9 I²C I/O Signals

Table 10 describes the I²C serial interface module signals.

**Table 10. I²C I/O Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Serial Clock | SCL | Open-drain clock signal for the for the I²C interface. Either it is driven by the I²C module when the bus is in master mode or it becomes the clock input when the I²C is in slave mode. | I/O |
| Serial Data | SDA | Open-drain signal that serves as the data input/output for the I²C interface. | I/O |

## 1.10 UART Module Signals

Table 11 describes the UART module signals.

**Table 11. UART Module Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Transmit Serial Data Output | UTXD*n* | Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source. | O |
| Receive Serial Data Input | URXD*n* | Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it. | I |
| Clear-to-Send | $\overline{\text{UCTS}n}$ | Indicate to the UART modules that they can begin data transmission. | I |
| Request-to-Send | $\overline{\text{URTS}n}$ | Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level. | O |

## 1.11 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

**Table 12. DMA Timer Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| DMA Timer Input | DTIN*n* | Event input to the DMA timer modules. | I |
| DMA Timer Output | DTOUT*n* | Programmable output from the DMA timer modules. | O |

## 1.16 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals

**Table 17. EzPort Signal Descriptions**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| EzPort Clock | EZPCK | Shift clock for EzPort transfers | I |
| EzPort Chip Select | EZPCS | Chip select for signalling the start and end of serial transfers | I |
| EzPort Serial Data In | EZPD | EZPD is sampled on the rising edge of EZPCK | I |
| EzPort Serial Data Out | EZPQ | EZPQ transitions on the falling edge of EZPCK | O |

## 1.17 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

**Table 18. Power and Ground Pins**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| PLL Analog Supply | VDDPLL, VSSPLL | Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply. | I |
| Positive Supply | VDD | These pins supply positive power to the core logic. | I |
| Ground | VSS | This pin is the negative supply (ground) to the chip. | — |

Some of the $V_{DD}$ and $V_{SS}$ pins on the device are only to be used for noise bypass. Figure 5 shows a typical connection diagram. Pay particular attention to those pins which show only capacitor connections. Do not connect power supply voltage directly to these pins.

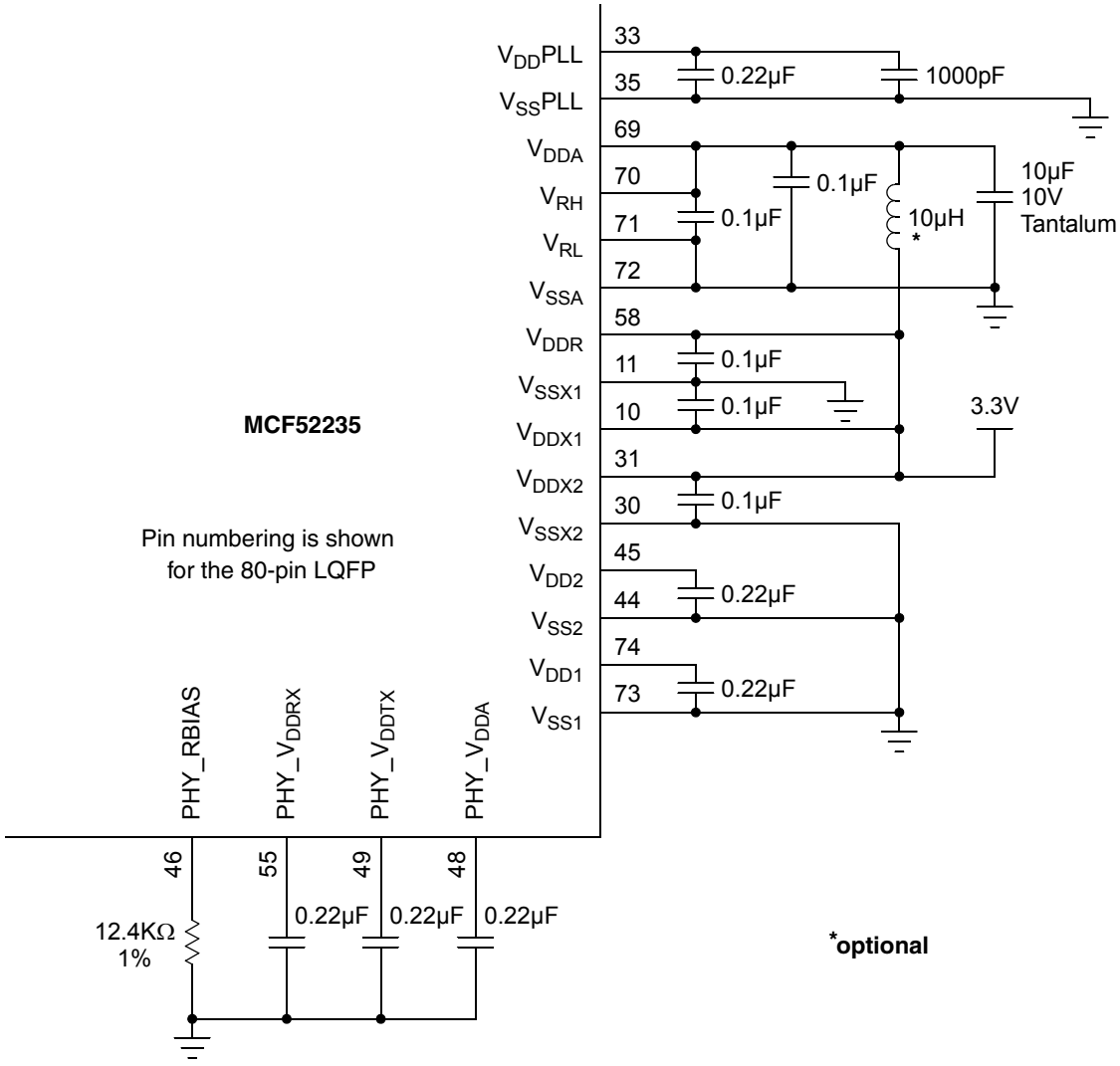



**Figure 5. Suggested Connection Scheme for Power and Ground**

# 2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF52235, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

**NOTE**

The parameters specified in this appendix supersede any values found in the module specifications.

**Table 20. Thermal Characteristics**

| Characteristic | Symbol | Package[1] | Value | Unit |
|---|---|---|---|---|
| Junction to ambient, natural convection | $\theta_{JA}$ | 80-pin LQFP, four-layer board | 36.0[2,3] | °C/W |
| | | 112-pin LQFP, four-layer board | 35.0 | |
| | | 121 MAPBGA, four-layer board | 32 | |
| | | 80-pin LQFP, one-layer board[1] | 49.0[1] | |
| | | 121 MAPBGA, one-layer board[1] | 56[1] | |
| | | 112-pin LQFP, one-layer board[1] | 44.0[1] | |
| Junction to ambient (@200 ft/min) | $\theta_{JMA}$ | 80-pin LQFP, four-layer board | 30.0 | °C/W |
| | | 112-pin LQFP, four-layer board | 29.0 | |
| | | 121 MAPBGA, four-layer board | 28 | |
| | | 80-pin LQFP, one-layer board[1] | 39.0[1] | |
| | | 112-pin LQFP, one-layer board[1] | 35.0[1] | |
| | | 121 MAPBGA, one-layer board[1] | 46[1] | |
| Junction to board | $\theta_{JB}$ | 80-pin LQFP | 22.0[4] | °C/W |
| | | 112-pin LQFP | 23.0 | |
| | | 121 MAPBGA, four-layer board | 18 | |
| Junction to case | $\theta_{JC}$ | 80-pin LQFP | 6.0[5] | °C/W |
| | | 112-pin LQFP | 6.0 | |
| | | 121 MAPBGA | 10 | |
| Junction to top of package, natural convection | $\Psi_{jt}$ | 80-pin LQFP | 2.0[6] | °C/W |
| | | 112-pin LQFP | 2.0[6] | |
| | | 121 MAPBGA | 2.0[6] | |
| Maximum operating junction temperature | $T_j$ | All | 130 | °C |

1 The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

2 $\theta_{JMA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JMA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

## 2.3 DC Electrical Specifications

**Table 22. DC Electrical Specifications [1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.6 | V |
| Input high voltage | $V_{IH}$ | $0.7 \times V_{DD}$ | 4.0 | V |
| Input low voltage | $V_{IL}$ | $V_{SS} - 0.3$ | $0.35 \times V_{DD}$ | V |
| Input hysteresis | $V_{HYS}$ | $0.06 \times V_{DD}$ | — | mV |
| Low-voltage detect trip voltage ($V_{DD}$ falling) | $V_{LVD}$ | 2.15 | 2.3 | V |
| Low-voltage detect hysteresis ($V_{DD}$ rising) | $V_{LVDHYS}$ | 60 | 120 | mV |
| Input leakage current<br>$V_{in} = V_{DD}$ or $V_{SS}$, input-only pins | $I_{in}$ | –1.0 | 1.0 | µA |
| High impedance (off-state) leakage current<br>$V_{in} = V_{DD}$ or $V_{SS}$, all input/output and output pins | $I_{OZ}$ | –1.0 | 1.0 | µA |
| Output high voltage (all input/output and all output pins)<br>$I_{OH}$ = –2.0 mA | $V_{OH}$ | $V_{DD}$ - 0.5 | — | V |
| Output low voltage (all input/output and all output pins)<br>$I_{OL}$ = 2.0 mA | $V_{OL}$ | — | 0.5 | V |
| Weak internal pull-up device current, tested at $V_{IL}$ max.[2] | $I_{APU}$ | –10 | –130 | µA |
| Input capacitance [3]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |
| Load capacitance[4]<br>Low drive strength<br>High drive strength | $C_L$ | | <br>25<br>50 | pF |
| DC injection current [3, 5, 6, 7]<br>$V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$<br>Single pin limit<br>Total MCU limit, Includes sum of all stressed pins | $I_{IC}$ | <br><br>–1.0<br>–10 | <br><br>1.0<br>10 | mA |

1 Refer to Table 25 for additional PLL specifications.

2 Refer to Table 3 for pins with internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

5 All functional non-supply pins are internally clamped to $V_{SS}$ and their respective $V_{DD}$.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that the external $V_{DD}$ load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, the system clock is not present during the power-up sequence until the PLL has attained lock.

**Table 23. Active Current Consumption Specifications**

| Characteristic | Symbol | Typical | | | | Peak | Unit |
|---|---|---|---|---|---|---|---|
| | | Running from SRAM, EPHY Off | Running from Flash, EPHY Off | Running from Flash, EPHY 10BaseT | Running from Flash, EPHY 100BaseT | | |
| Active current, core and I/O<br>PLL @25 MHz<br>PLL @60 MHz | $I_{DDR}+I_{DDX}+I_{DDA}$ | <br>75<br>130 | <br>82<br>138 | <br>150<br>220 | <br>260<br>310 | <br>290<br>340 | <br>mA |
| Analog supply current<br>Normal operation<br>Low-power STOP | $I_{DDA}$ | <br>20<br>15 | <br>20<br>15 | <br>20<br>15 | <br>20<br>15 | <br>30<br>50 | <br>mA<br>μA |

**Table 24. Current Consumption Specifications in Low-Power Modes[1]**

| Mode[2] | PLL @25 MHz (typical)[3] | PLL @60 MHz (typical)[3] | PLL @60 MHz (peak)[4] | Unit |
|---|---|---|---|---|
| STOP mode 3 (STPMD[1:0]=11) | 0.2 | | 1.0 | mA |
| STOP mode 2 (STPMD[1:0]=10) | 7 | | — | |
| STOP mode 1 (STPMD[1:0]=01) | 10 | 12 | — | |
| STOP mode 0 (STPMD[1:0]=00) | 10 | 12 | — | |
| WAIT | 16 | 27 | — | |
| DOZE | 16 | 27 | — | |
| RUN | 25 | 45 | — | |

1 All values are measured with a 3.30 V power supply.

2 Refer to the “Power Management” chapter in the *MCF52235 ColdFire® Integrated Microcontroller Reference Manual* for more information on low-power modes.

3 These values were obtained with CLKOUT and all peripheral clocks except for the CFM clock disabled prior to entering low-power mode. The tests were performed at room temperature. All code was executed from flash memory; running code from SRAM further reduces power consumption.

4 These values were obtained with CLKOUT and all peripheral clocks enabled. All code was executed from flash memory.

## 2.6 Reset Timing

**Table 27. Reset and Configuration Override Timing**

**($V_{DD}$ = 2.7 to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = $T_L$ to $T_H$)[1]**

| Num | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| R1 | $\overline{\text{RSTI}}$ input valid to CLKOUT high | $t_{RVCH}$ | 9 | — | ns |
| R2 | CLKOUT high to $\overline{\text{RSTI}}$ input invalid | $t_{CHRI}$ | 1.5 | — | ns |
| R3 | $\overline{\text{RSTI}}$ input valid time [2] | $t_{RIVT}$ | 5 | — | $t_{CYC}$ |
| R4 | CLKOUT high to $\overline{\text{RSTO}}$ valid | $t_{CHROV}$ | — | 10 | ns |

1 All AC timing is shown with respect to 50% $V_{DD}$ levels unless otherwise noted.

2 During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Therefore, $\overline{\text{RSTI}}$ must be held a minimum of 100ns.

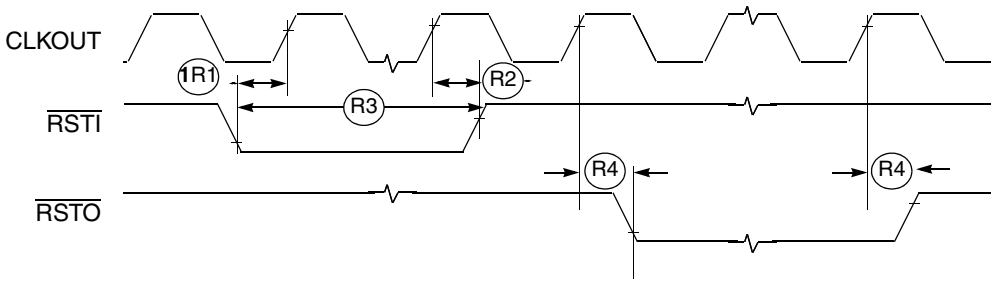



**Figure 7. $\overline{\text{RSTI}}$ and Configuration Override Timing**

## 2.7 I²C Input/Output Timing Specifications

Table 28 lists specifications for the I²C input timing parameters shown in Figure 8.

**Table 28. I²C Input Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1 | Start condition hold time | 2 × $t_{CYC}$ | — | ns |
| I2 | Clock low period | 8 × $t_{CYC}$ | — | ns |
| I3 | SCL/SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | SCL/SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | 4 × $t_{CYC}$ | — | ns |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | 2 × $t_{CYC}$ | — | ns |
| I9 | Stop condition setup time | 2 × $t_{CYC}$ | — | ns |

Table 29 lists specifications for the I²C output timing parameters shown in Figure 8.

**Table 29. I²C Output Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1 [1] | Start condition hold time | 6 × $t_{CYC}$ | — | ns |
| I2 [1] | Clock low period | 10 × $t_{CYC}$ | — | ns |
| I3 [2] | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | — | µs |
| I4 [1] | Data hold time | 7 × $t_{CYC}$ | — | ns |
| I5 [3] | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 3 | ns |
| I6 [1] | Clock high time | 10 × $t_{CYC}$ | — | ns |
| I7 [1] | Data setup time | 2 × $t_{CYC}$ | — | ns |
| I8 [1] | Start condition setup time (for repeated start condition only) | 20 x $t_{CYC}$ | — | ns |
| I9 [1] | Stop condition setup time | 10 x $t_{CYC}$ | — | ns |

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 29. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 29 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 8 shows timing for the values in Table 28 and Table 29.

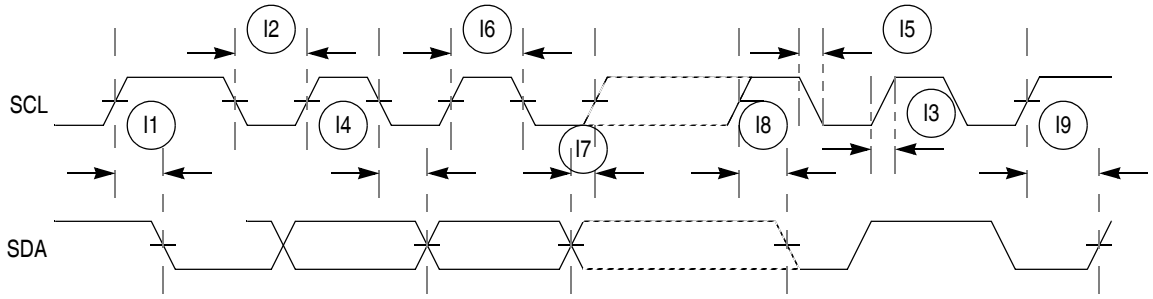



**Figure 8. I²C Input/Output Timings**

# 2.8 EPHY Parameters

## 2.8.1 EPHY Timing

Table 30 and Figure 9 show the relevant EPHY timing parameters.

**Table 30. EPHY Timing Parameters**

| Num | Characteristic | Symbol | Value | Unit |
|---|---|---|---|---|
| E1 | EPHY startup time | $t_{Start-Up}$ | 360 | µs |

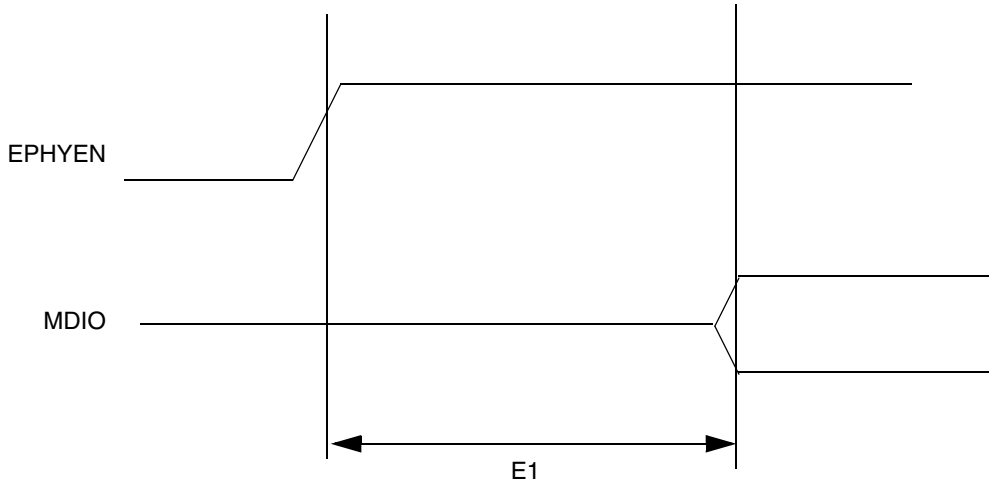



**Figure 9. EPHY Timing**

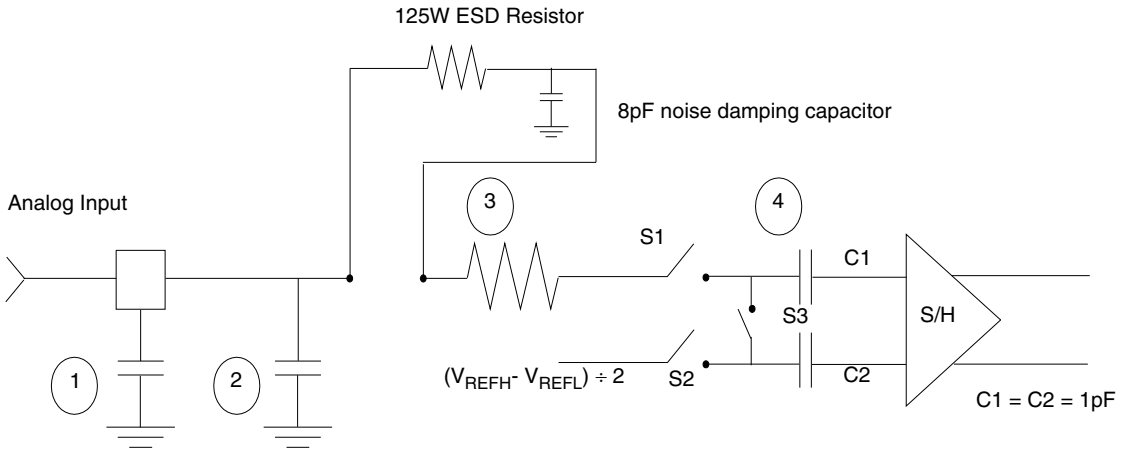
## 2.8.2 10BASE-T SQE (Heartbeat) Timing

Table 31 and Figure 10 show the relevant 10BASE-T SQE (heartbeat) timing parameters.

**Table 31. 10BASE-T SQE (Heartbeat) Timing Parameters**

| Characteristic | Symbol | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| COL (SQE) delay after TXEN off | t1 | — | 1.0 | — | µs |
| COL (SQE) pulse duration | t2 | — | 1.0 | — | µs |

[1] Typical values are at 25°C.




1 Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF

2 Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF

3 Equivalent resistance for the channel select mux; 100 ohms

4 Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF

5 Equivalent input impedance, when the input is selected = $\frac{1}{\text{ADC CLOCK RATE} \times (1.4 \times 10^{-12})}$

**Figure 12. Equivalent Circuit for A/D Loading**

## 2.10 DMA Timers Timing Specifications

Table 36 lists timer module AC timings.

**Table 36. Timer Module AC Timing Specifications**

| Name | Characteristic[1] | Min | Max | Unit |
|---|---|---|---|---|
| T1 | DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time | $3 \times t_{CYC}$ | — | ns |
| T2 | DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width | $1 \times t_{CYC}$ | — | ns |

1 All timing references to CLKOUT are given to its rising edge.

## 2.11 EzPort Electrical Specifications

**Table 37. EzPort Electrical Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| EP1 | EPCK frequency of operation (all commands except READ) | — | $f_{sys}$ / 2 | MHz |
| EP1a | EPCK frequency of operation (READ command) | — | $f_{sys}$ / 8 | MHz |
| EP2 | EPCS_b negation to next EPCS_b assertion | $2 \times T_{cyc}$ | — | ns |
| EP3 | EPCS_B input valid to EPCK high (setup) | 5 | — | ns |
| EP4 | EPCK high to EPCS_B input invalid (hold) | 5 | — | ns |
| EP5 | EPD input valid to EPCK high (setup) | 2 | — | ns |
| EP6 | EPCK high to EPD input invalid (hold) | 5 | — | ns |

## 2.14 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 19.

**Table 40. Debug AC Timing Specification**

| Num | Characteristic | 60 MHz | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| D1 | PST, DDATA to CLKOUT setup | 4 | — | ns |
| D2 | CLKOUT to PST, DDATA hold | 1.5 | — | ns |
| D3 | DSI-to-DSCLK setup | $1 \times t_{CYC}$ | — | ns |
| D4 [1] | DSCLK-to-DSO hold | $4 \times t_{CYC}$ | — | ns |
| D5 | DSCLK cycle time | $5 \times t_{CYC}$ | — | ns |
| D6 | $\overline{BKPT}$ input data setup time to CLKOUT Rise | 4 | — | ns |
| D7 | $\overline{BKPT}$ input data hold time to CLKOUT Rise | 1.5 | — | ns |
| D8 | CLKOUT high to $\overline{BKPT}$ high Z | 0.0 | 10.0 | ns |

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 18 shows real-time trace timing for the values in Table 40.

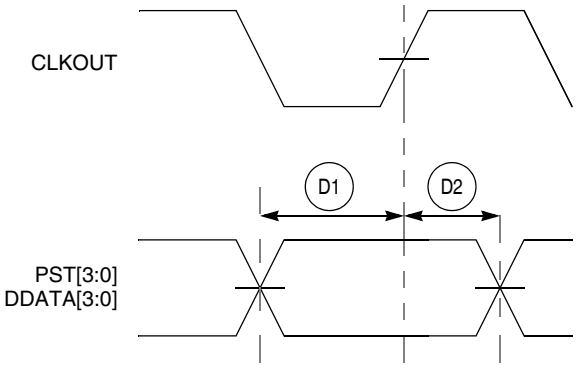



**Figure 18. Real-Time Trace AC Timing**

Figure 19 shows BDM serial port AC timing for the values in Table 40.

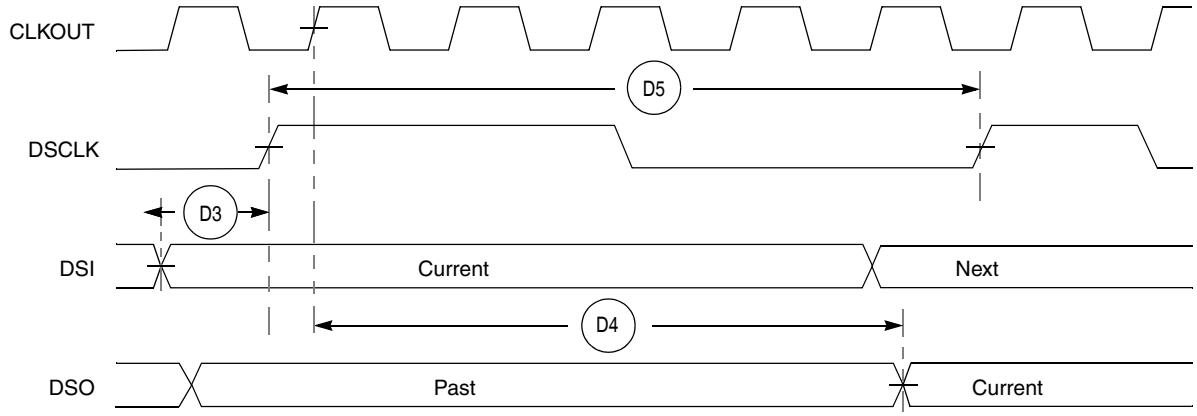
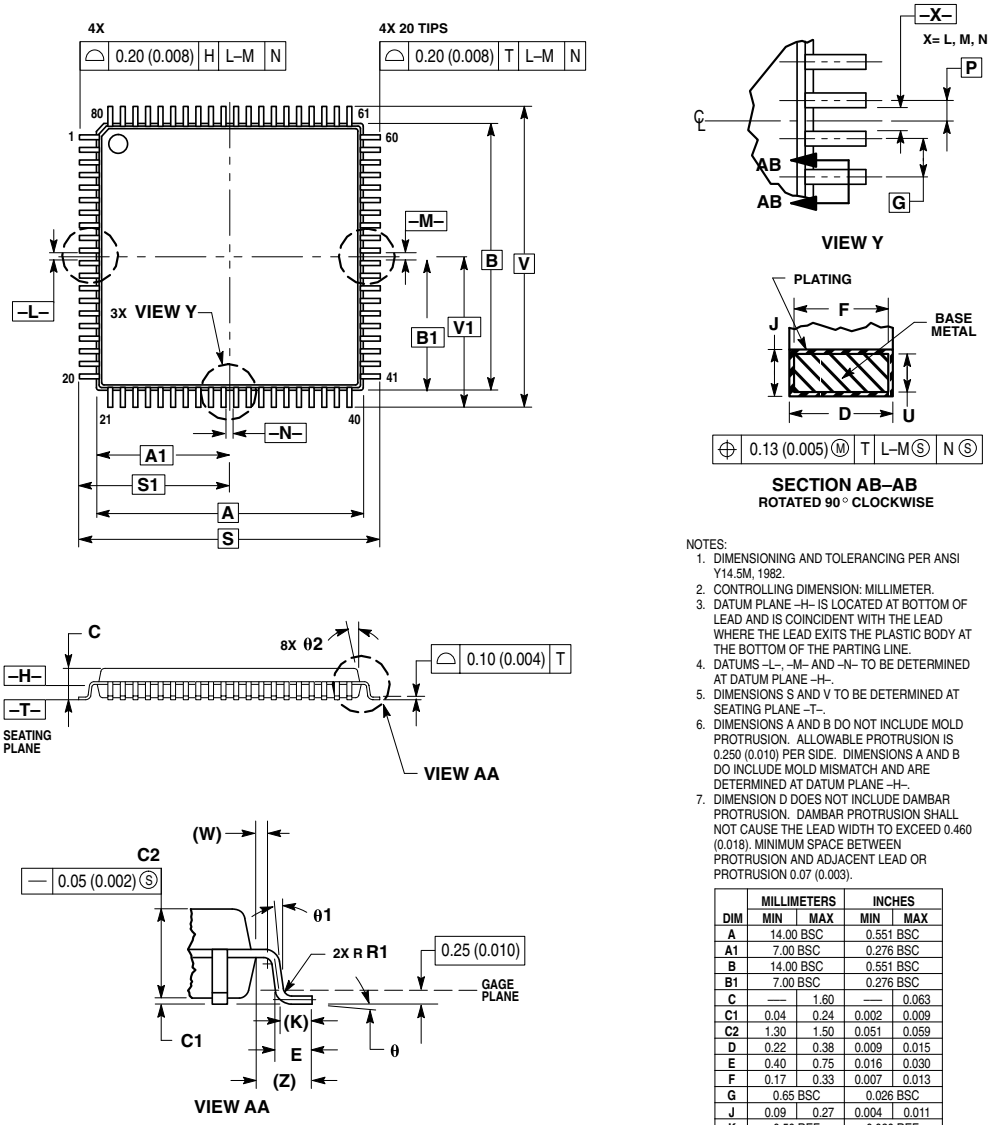



**Figure 19. BDM Serial Port AC Timing**

# 3 Mechanical Outline Drawings

This section describes the physical properties of the MCF52235 and its derivatives.

## 3.1 80-pin LQFP Package




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 14.00 BSC | | 0.551 BSC | |
| A1 | 7.00 BSC | | 0.276 BSC | |
| B | 14.00 BSC | | 0.551 BSC | |
| B1 | 7.00 BSC | | 0.276 BSC | |
| C | — | 1.60 | — | 0.063 |
| C1 | 0.04 | 0.24 | 0.002 | 0.009 |
| C2 | 1.30 | 1.50 | 0.051 | 0.059 |
| D | 0.22 | 0.38 | 0.009 | 0.015 |
| E | 0.40 | 0.75 | 0.016 | 0.030 |
| F | 0.17 | 0.33 | 0.007 | 0.013 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.27 | 0.004 | 0.011 |
| K | 0.50 REF | | 0.020 REF | |
| P | 0.325 BSC | | 0.013 REF | |
| R1 | 0.10 | 0.20 | 0.004 | 0.008 |
| S | 16.00 BSC | | 0.630 BSC | |
| S1 | 8.00 BSC | | 0.315 BSC | |
| U | 0.09 | 0.16 | 0.004 | 0.006 |
| V | 16.00 BSC | | 0.630 BSC | |
| V1 | 8.00 BSC | | 0.315 BSC | |
| W | 0.20 REF | | 0.008 REF | |
| Z | 1.00 REF | | 0.039 REF | |
| θ | 0° | 10° | 0° | 10° |
| θ1 | 0° | — | 0° | — |
| θ2 | 9° | 14° | 9° | 14° |

**CASE 917A–02**
**ISSUE C**

**DATE 09/21/95**