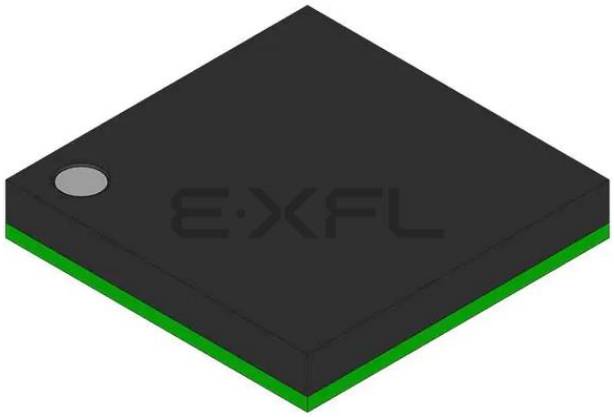

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	73
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LBGA
Supplier Device Package	121-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52235cvm60

1 MCF52235 Family Configurations

Table 1. MCF52235 Family Configurations

Module	52230	52231	52232	52233	52234	52235	52236
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•	•
System Clock (MHz)	60	60	50	60	60	60	50
Performance (Dhrystone 2.1 MIPS)	56	56	46	56	56	56	46
Flash / Static RAM (SRAM)	128/32 Kbytes	128/32 Kbytes	128/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes	256/32 Kbytes
Interrupt Controllers (INTC0/INTC1)	•	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•	•
Random Number Generator and Crypto Acceleration Unit (CAU)	—	—	—	—	—	•	—
FlexCAN 2.0B Module	—	•	—	—	•	•	—
Fast Ethernet Controller (FEC) with on-chip interface (EPHY)	•	•	•	•	•	•	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•	•
Programmable Interrupt Timer	2	2	2	2	2	2	2
Four-Channel General Purpose Timer	•	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4	4
QSPI	•	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port[1]	•	•	•	•	•	•	•
Package	80 LQFP 112 LQFP	80 LQFP 112 LQFP	80 LQFP	80 LQFP 112 LQFP	112 LQFP 121 MAPBGA	112 LQFP 121 MAPBGA	80 LQFP

[1] The full debug/trace interface is available only on the 112- and 121-pin packages. A reduced debug interface is bonded on the 80-pin package.

- Four 32-bit DMA timers
  - 17-ns resolution at 60 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timers
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low power mode support
- Clock Generation Features
  - Crystal input
  - On-chip PLL
  - Provides clock for integrated EPHY
- Dual Interrupt Controllers (INTC0/INTC1)
  - Support for multiple interrupt sources organized as follows:
    - Fully-programmable interrupt sources for each peripheral
    - 7 fixed-level interrupt sources
    - Seven external interrupt signals

1.2.15 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or can be a free-running down-counter.

1.2.16 Pulse Width Modulation (PWM) Timers

The MCF52235 has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0 to 100%. The PWM outputs have programmable polarity and can be programmed as left-aligned outputs or center-aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.17 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.18 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.19 Interrupt Controller (INTC0/INTC1)

There are two interrupt controllers on the MCF52235. These interrupt controllers are organized as seven levels with up to nine interrupt sources per level. Each interrupt source has a unique interrupt vector, and provide each peripheral with all necessary interrupts. Each internal interrupt has a programmable level [1-7] and priority within the level. The seven external interrupts have fixed levels/priorities.

1.2.20 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.21 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
ADC[3]	AN7	—	—	PAN[7]	Low	—	—	A10	88	64
	AN6	—	—	PAN[6]	Low	—	—	B10	87	63
	AN5	—	—	PAN[5]	Low	—	—	A11	86	62
	AN4	—	—	PAN[4]	Low	—	—	B11	85	61
	AN3	—	—	PAN[3]	Low	—	—	C9	89	65
	AN2	—	—	PAN[2]	Low	—	—	B9	90	66
	AN1	—	—	PAN[1]	Low	—	—	A9	91	67
	AN0	—	—	PAN[0]	Low	—	—	C8	92	68
	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	K1	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	J1	27	19
	VDDA	—	—	—	N/A	N/A	—	A8	93	69
	VSSA	—	—	—	N/A	N/A	—	A7	96	72
	VRH	—	—	—	N/A	N/A	—	B8	94	70
	VRL	—	—	—	N/A	N/A	—	B7	95	71
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	L7	48	36
	XTAL	—	—	—	N/A	N/A	—	J7	49	37
	VDDPLL[5]	—	—	—	N/A	N/A	—	K6	45	33
	VSSPLL	—	—	—	N/A	N/A	—	K7	47	35
Debug Data	ALLPST	—	—	—	High	—	—	D3	7	7
	DDATA[3:0]	—	—	PDD[7:4]	High	—	—	E1, F3,F2, F1	12,13,16,17	—
	PST[3:0]	—	—	PDD[3:0]	High	—	—	D10, D9, E10, E9	80,79,78,77	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	SecondaryFunction	Tertiary Function	Quaternary Function	Drive Strength/ Control[1]	Wired OR Control	Pull-up/ Pull-down[2]	Pin on 121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP
UART 1[3]	$\overline{\text{UCTS1}}$	SYNCA	URXD2	PUB[3]	PDSR[15]	—	—	J3	24	16
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	PUB[2]	PDSR[14]	—	—	H3	23	15
	URXD1	—	FEC_TXD[0]	PUB[1]	PDSR[13]	PWOR[2]	—	K3	32	23
	UTXD1	—	FEC_COL	PUB[0]	PDSR[12]	PWOR[3]	—	L3	33	24
UART 2	$\overline{\text{UCTS2}}$	—	—	PUC[3]	PDSR[27]	—	—	L10	61	—
	$\overline{\text{URTS2}}$	—	—	PUC[2]	PDSR[26]	—	—	K10	60	—
	URXD2	—	—	PUC[1]	PDSR[25]	—	—	K11	62	—
	UTXD2	—	—	PUC[0]	PDSR[24]	—	—	L11	63	—
FlexCAN	SYNCA	CANTX[4]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	28	20
	SYNCB	CANRX[4]	FEC_MDC	PAS[2]	PDSR[39]	—	—	—	27	19
VDD[5,11]	VDD	—	—	—	N/A	N/A	—	D7, E8	65,102	45,74
VDDX	VDDX	—	—	—	N/A	N/A	—	D5, D6, E6, G5, G6, G7, H6	14, 43	10, 31
VSS	VSS	—	—	—	N/A	N/A	—	E4, E5, E7,F4, F5, F6, F7, F8	64,101	44,73
VSSX	VSSX	—	—	—	N/A	N/A	—	—	15, 42	11, 30

1 The PDSR and PSSR registers are described in Chapter 14, "General Purpose I/O Module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The use of an external PHY limits ADC, interrupt, and QSPI functionality. It also disables the UART0/1 and timer pins.
4 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
5 The VDD1, VDD2, VDDPLL, and PHY_VDD pins are for decoupling only and should not have power directly applied to them.
6 For primary and GPIO functions only.
7 Only when JTAG mode is enabled.
8 For secondary and GPIO functions only.
9 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the Ethernet PHY.

1.3 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 512 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input.	I
Crystal	XTAL	Crystal oscillator output.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 6 describes signals used in mode selection, Table 6 describes particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device.	—
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

1.6 External Interrupt Signals

Table 7 describes the external interrupt signals.

Table 7. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[15:1]	External interrupt sources.	I

1.7 Queued Serial Peripheral Interface (QSPI)

Table 8 describes QSPI signals.

Table 8. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip selects that can be programmed to be active high or low.	O

1.8 Fast Ethernet Controller EPHY Signals

Table 9 describes the Fast Ethernet Controller (FEC) signals.

Table 9. Fast Ethernet Controller (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Twisted Pair Input +	RXP	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Input -	RXN	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Output +	TXN	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Twisted Pair Output -	TXP	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Bias Control Resistor	RBIAS	Connect a 12.4 kΩ (1.0%) external resistor, RBIAS, between the PHY_RBIAS pin and analog ground. Place this resistor as near to the chip pin as possible. Stray capacitance must be kept to less than 10 pF (>50 pF causes instability). No high-speed signals can be permitted in the region of RBIAS.	I
Activity LED	ACT_LED	Indicates when the EPHY is transmitting or receiving	O
Link LED	LINK_LED	Indicates when the EPHY has a valid link	O
Speed LED	SPD_LED	Indicates the speed of the EPHY connection	O
Duplex LED	DUPLED	Indicates the duplex (full or half) of the EPHY connection	O
Collision LED	COLLED	Indicates if the EPHY detects a collision	O
Transmit LED	TXLED	Indicates if the EPHY is transmitting	O
Receive LED	RXLED	Indicates if the EPHY is receiving	O

Table 20. Thermal Characteristics

Characteristic	Symbol	Package[1]	Value	Unit
Junction to ambient, natural convection	θ_{JA}	80-pin LQFP, four-layer board	36.0[2,3]	°C/W
		112-pin LQFP, four-layer board	35.0	
		121 MAPBGA, four-layer board	32	
		80-pin LQFP, one-layer board[1]	49.0[1]	
		121 MAPBGA, one-layer board[1]	56[1]	
		112-pin LQFP, one-layer board[1]	44.0[1]	
Junction to ambient (@200 ft/min)	θ_{JMA}	80-pin LQFP, four-layer board	30.0	°C/W
		112-pin LQFP, four-layer board	29.0	
		121 MAPBGA, four-layer board	28	
		80-pin LQFP, one-layer board[1]	39.0[1]	
		112-pin LQFP, one-layer board[1]	35.0[1]	
		121 MAPBGA, one-layer board[1]	46[1]	
Junction to board	θ_{JB}	80-pin LQFP	22.0[4]	°C/W
		112-pin LQFP	23.0	
		121 MAPBGA, four-layer board	18	
Junction to case	θ_{JC}	80-pin LQFP	6.0[5]	°C/W
		112-pin LQFP	6.0	
		121 MAPBGA	10	
Junction to top of package, natural convection	Ψ_{jt}	80-pin LQFP	2.0[6]	°C/W
		112-pin LQFP	2.0[6]	
		121 MAPBGA	2.0[6]	
Maximum operating junction temperature	T_j	All	130	°C

1 The use of this device in one- or two-layer board designs is not recommended due to the limited thermal conductance provided by those boards.

2 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JMA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

2.3 DC Electrical Specifications

Table 22. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, input-only pins	I_{in}	–1.0	1.0	µA
High impedance (off-state) leakage current $V_{in} = V_{DD}$ or V_{SS}, all input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Weak internal pull-up device current, tested at V_{IL} max.[2]	I_{APU}	–10	–130	µA
Input capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load capacitance[4] Low drive strength High drive strength	C_L		 25 50	pF
DC injection current [3, 5, 6, 7] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single pin limit Total MCU limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10	 1.0 10	mA

1 Refer to Table 25 for additional PLL specifications.

2 Refer to Table 3 for pins with internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

5 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, the system clock is not present during the power-up sequence until the PLL has attained lock.

Table 23. Active Current Consumption Specifications

Characteristic	Symbol	Typical				Peak	Unit
		Running from SRAM, EPHY Off	Running from Flash, EPHY Off	Running from Flash, EPHY 10BaseT	Running from Flash, EPHY 100BaseT		
Active current, core and I/O PLL @25 MHz PLL @60 MHz	$I_{DDR}+I_{DDX}+I_{DDA}$	 75 130	 82 138	 150 220	 260 310	 290 340	 mA
Analog supply current Normal operation Low-power STOP	I_{DDA}	 20 15	 20 15	 20 15	 20 15	 30 50	 mA μA

Table 24. Current Consumption Specifications in Low-Power Modes[1]

Mode[2]	PLL @25 MHz (typical)[3]	PLL @60 MHz (typical)[3]	PLL @60 MHz (peak)[4]	Unit
STOP mode 3 (STPMD[1:0]=11)	0.2		1.0	mA
STOP mode 2 (STPMD[1:0]=10)	7		—	
STOP mode 1 (STPMD[1:0]=01)	10	12	—	
STOP mode 0 (STPMD[1:0]=00)	10	12	—	
WAIT	16	27	—	
DOZE	16	27	—	
RUN	25	45	—	

1 All values are measured with a 3.30 V power supply.

2 Refer to the “Power Management” chapter in the *MCF52235 ColdFire® Integrated Microcontroller Reference Manual* for more information on low-power modes.

3 These values were obtained with CLKOUT and all peripheral clocks except for the CFM clock disabled prior to entering low-power mode. The tests were performed at room temperature. All code was executed from flash memory; running code from SRAM further reduces power consumption.

4 These values were obtained with CLKOUT and all peripheral clocks enabled. All code was executed from flash memory.

2.8 EPHY Parameters

2.8.1 EPHY Timing

Table 30 and Figure 9 show the relevant EPHY timing parameters.

Table 30. EPHY Timing Parameters

Num	Characteristic	Symbol	Value	Unit
E1	EPHY startup time	$t_{Start-Up}$	360	µs

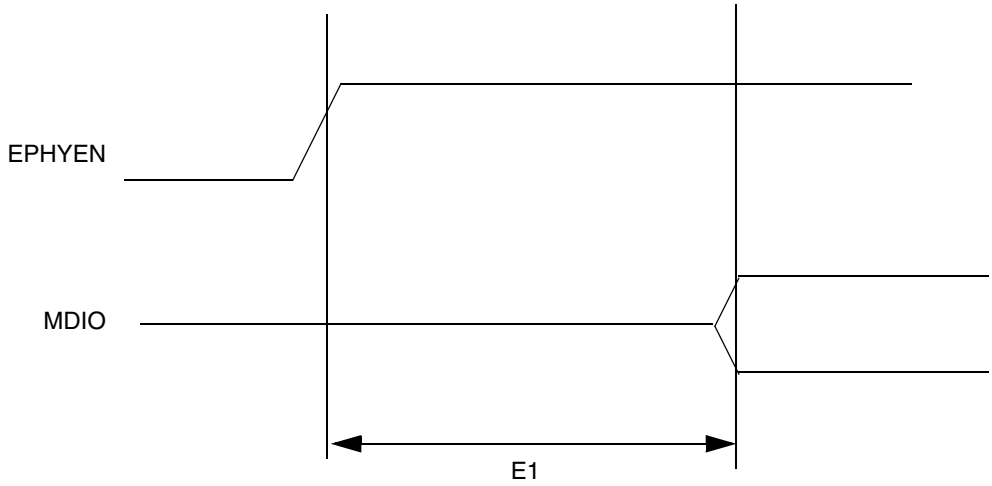


Figure 9. EPHY Timing

2.8.2 10BASE-T SQE (Heartbeat) Timing

Table 31 and Figure 10 show the relevant 10BASE-T SQE (heartbeat) timing parameters.

Table 31. 10BASE-T SQE (Heartbeat) Timing Parameters

Characteristic	Symbol	Min	Typ[1]	Max	Units
COL (SQE) delay after TXEN off	t1	—	1.0	—	µs
COL (SQE) pulse duration	t2	—	1.0	—	µs

[1] Typical values are at 25°C.

Table 35. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 12	—	pF
X_{IN}	Input impedance	—	See Figure 12	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±11	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	—	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	75	—	dB
SINAD	Signal-to-noise plus distortion	—	65	—	dB
ENOB	Effective number OF bits	9.1	10.6	—	Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

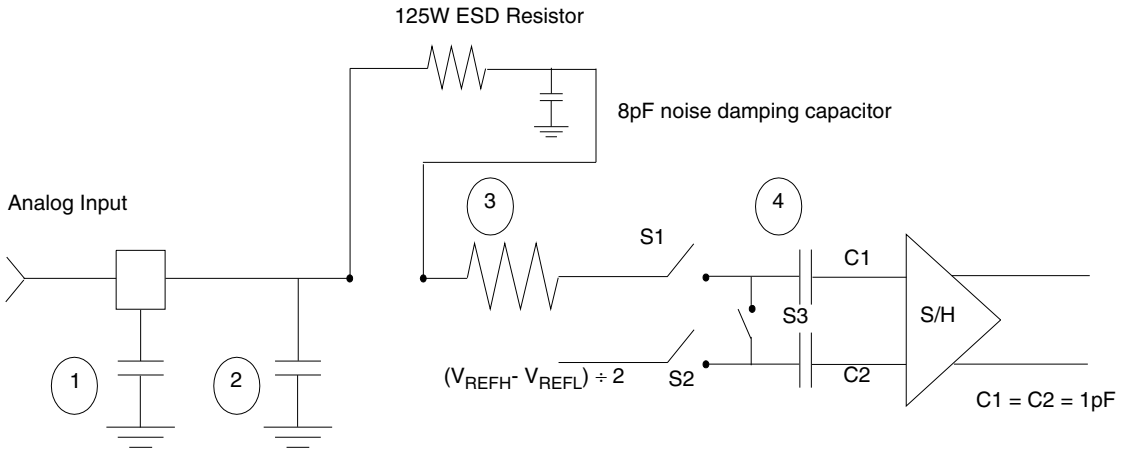
5 Includes power-up of ADC and V_{REF}

6 ADC clock cycles

7 The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.9.1 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an ongoing input current, which is a function of the analog input voltage, V_{REF}, and the ADC clock frequency.



1 Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF

2 Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF

3 Equivalent resistance for the channel select mux; 100 ohms

4 Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF

5 Equivalent input impedance, when the input is selected = $\frac{1}{\text{ADC CLOCK RATE} \times (1.4 \times 10^{-12})}$

Figure 12. Equivalent Circuit for A/D Loading

2.10 DMA Timers Timing Specifications

Table 36 lists timer module AC timings.

Table 36. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

1 All timing references to CLKOUT are given to its rising edge.

2.11 EzPort Electrical Specifications

Table 37. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	f_{sys} / 2	MHz
EP1a	EPCK frequency of operation (READ command)	—	f_{sys} / 8	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{cyc}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns

2.13 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

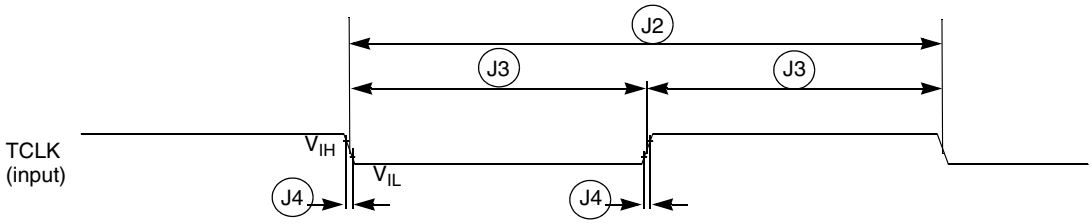
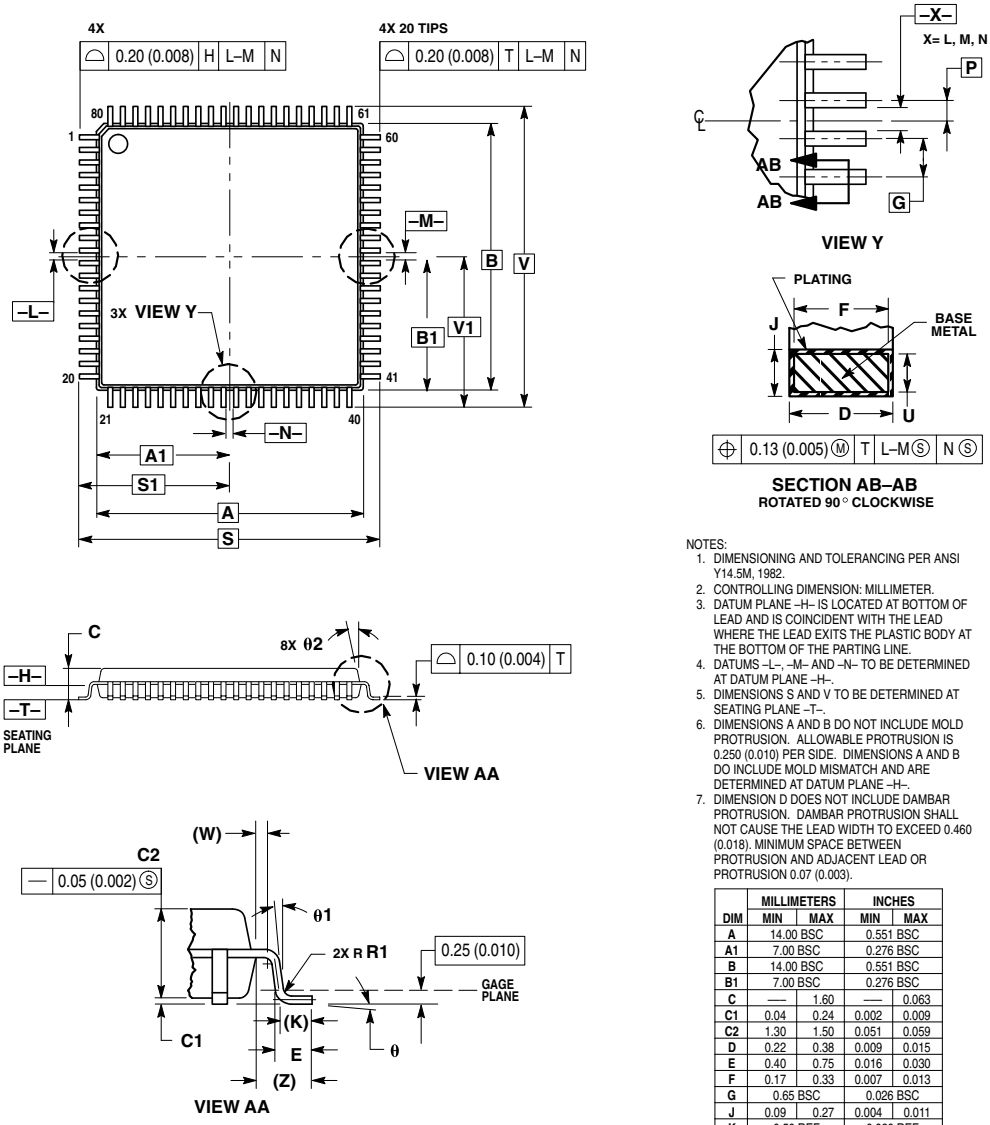


Figure 14. Test Clock Input Timing

3 Mechanical Outline Drawings

This section describes the physical properties of the MCF52235 and its derivatives.

3.1 80-pin LQFP Package



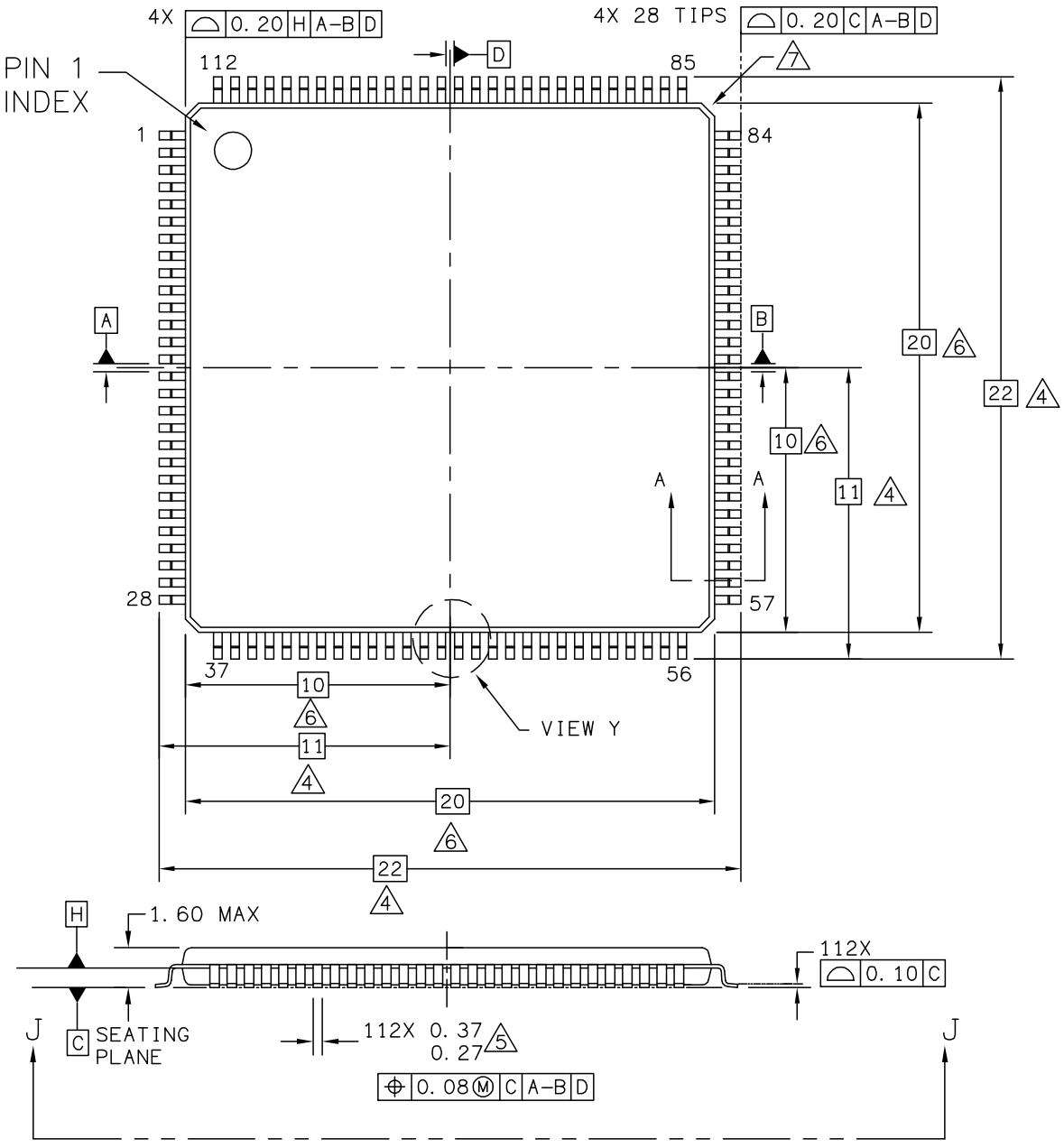
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.60	—	0.063
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.10	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

CASE 917A–02
ISSUE C

DATE 09/21/95

3.2 112-pin LQFP Package



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TITLE: 112LD LQFP 20 X 20 X 1.4 0.65 PITCH	DOCUMENT NO: 98ASS23330W	REV: E
	CASE NUMBER: 987-02	25 MAY 2005
	STANDARD: JEDEC MS-026 BFA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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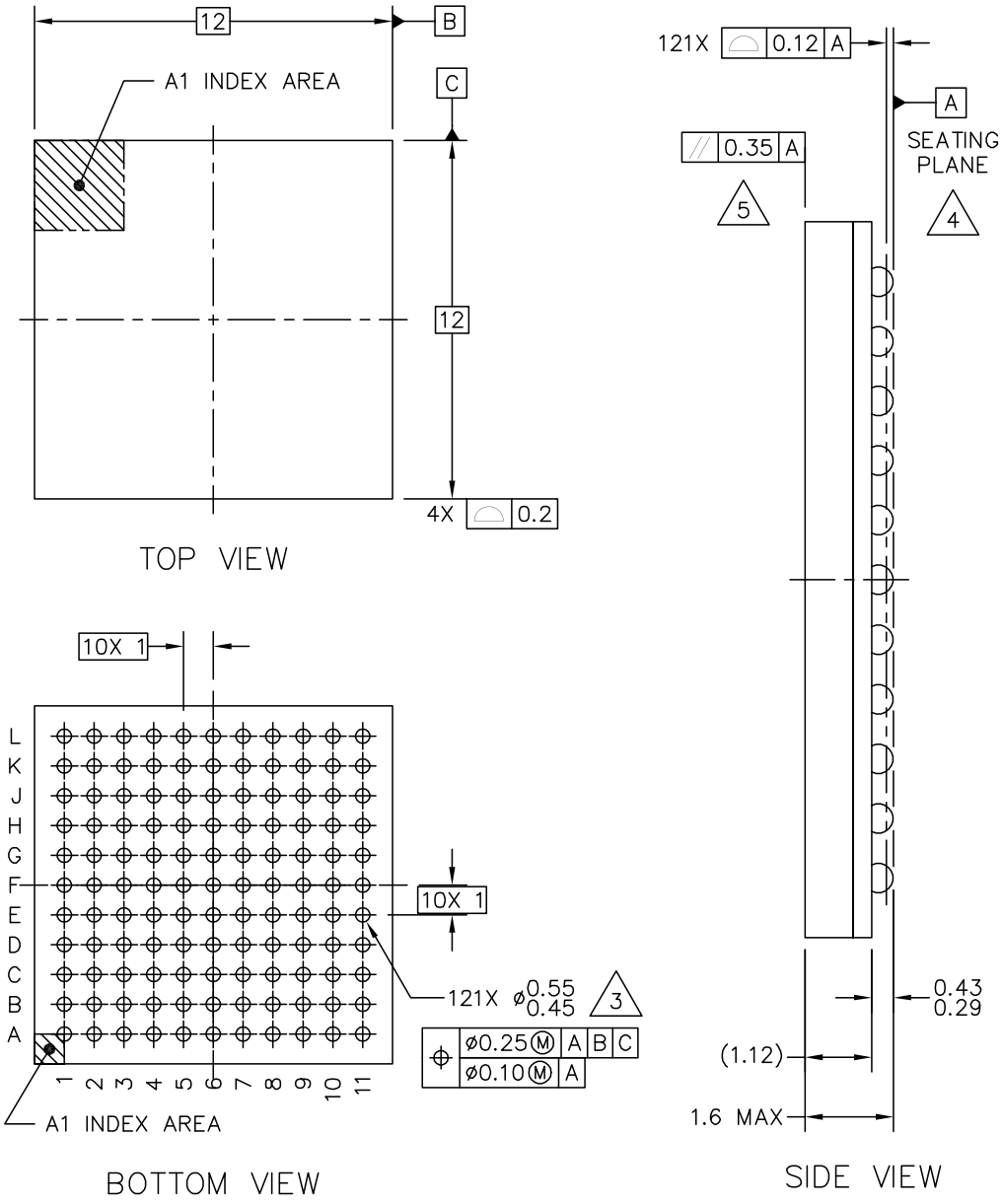
	CASE NUMBER: 987–02	25 MAY 2005
	STANDARD: JEDEC MS–026 BFA	

3.3 121 MAPBGA Package



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	CASE NUMBER: 1817–01	15 NOV 2005
	STANDARD: NON–JEDEC	

Table 41. Revision History (continued)

Revision	Description
8 Sep 2009	• Updated Table 25 — PLL Electrical Specifications.
8 April 2010	• Updated Table 37— EzPort Electrical Specifications
22 Mar 2011	• Updated Table Oscillator and PLL Electrical Specification. In EXTAL input high voltage updated VDD to 3.0
23-Mar-2011	• Changed EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, add a note this value has been updated. • Updated clock generation feature

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