Infineon Technologies - MB90911ASPMC-GT-101E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90911aspmc-gt-101e1

DTP/External interrupt : up to 8 channels, CAN wakeup : up to 1 channel

Module for activation of expanded intelligent I/O service (EI^{2}OS) and generation of external interrupt by external input

Delay interrupt generator module

Generates interrupt request for task switching

8/10-bit A/D converter : 16 channels

- Resolution is selectable between 8-bit and 10-bit
- Activation by external trigger input is allowed
- Conversion time : 3 µs (at 24 MHz machine clock, including sampling time)

Program patch function

Address matching detection for 6 address pointers

Capable of changing input voltage for port

Automotive/CMOS-Schmitt input level (initial level is Automotive in single-chip mode)

ROM security function

The content of ROM can be protected (Only MASK ROM product).

Flash memory security function

Protects the content of Flash memory

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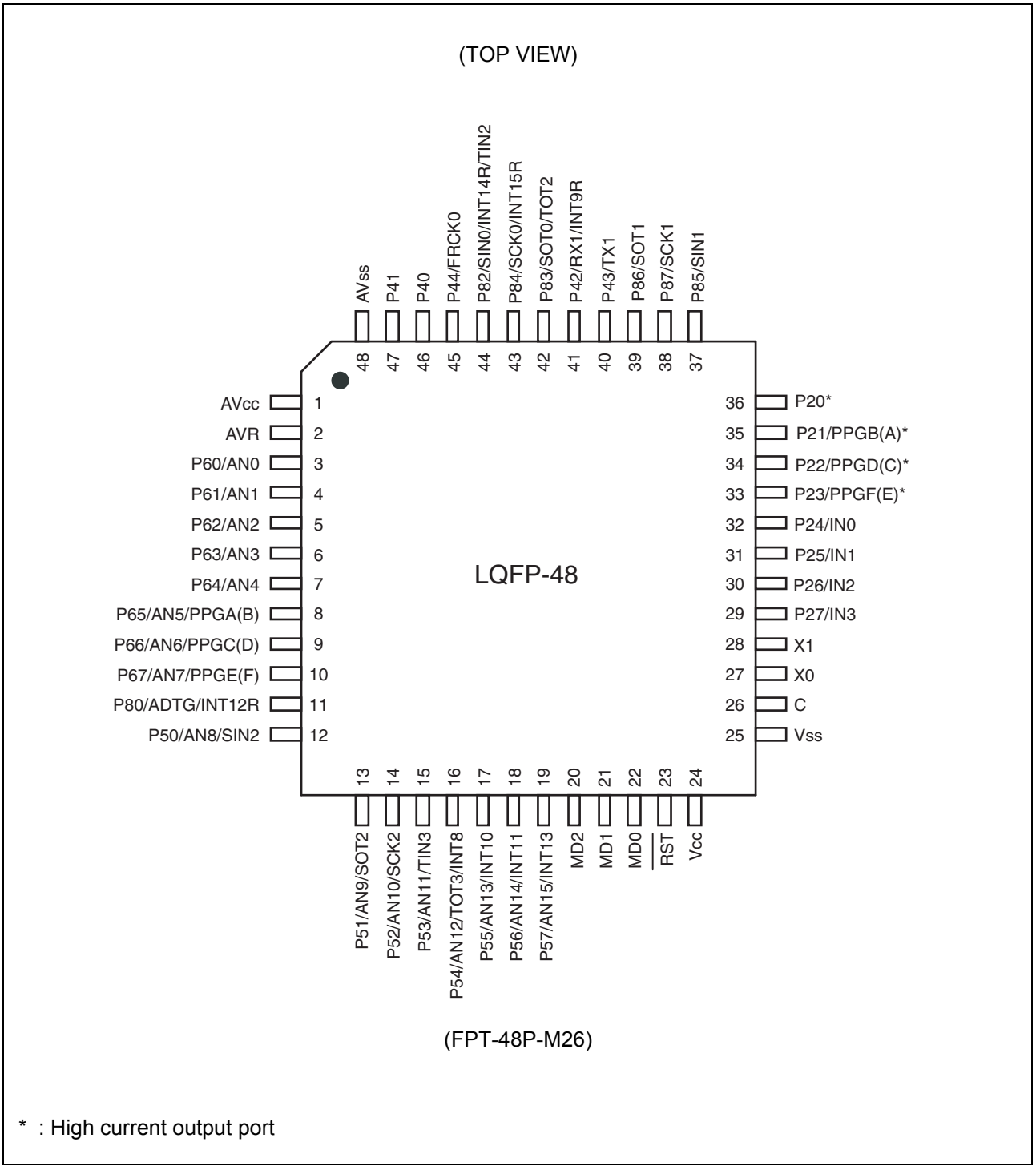
2. Pin Assignment

■ **MB90F912BS, MB90911A**S



* : High current output port

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Pin No.	Pin name	I/O circuit type*	Function
40	P43	F	General-purpose I/O port.
	TX1		TX output pin for CAN1 controller.
41	P42	F	General-purpose I/O port.
	RX1		RX input pin for CAN1 controller.
	INT9R		External interrupt request input pin for INT9R.
42	P83	F	General-purpose I/O port.
	SOT0		Serial data output pin for UART0.
	TOT2		Output pin for reload timer 2.
43	P84	F	General-purpose I/O port.
	SCK0		Clock I/O pin for UART0.
	INT15R		External interrupt request input pin for INT15R.
44	P82	K	General-purpose I/O port.
	SIN0		Serial data input pin for UART0.
	INT14R		External interrupt request input pin for INT14R.
	TIN2		Event input pin for reload timer 2.
45	P44	F	General-purpose I/O port (Different I/O circuit type from MB90V950AMAS).
	FRCK0		Free-run timer 0 clock input pin.
46, 47	P40, P41	F	General-purpose I/O port
48	AV_{SS}	I	V_{SS} power input pin for analog circuit.

* : For the I/O circuit type, refer to “I/O Circuit Type”.

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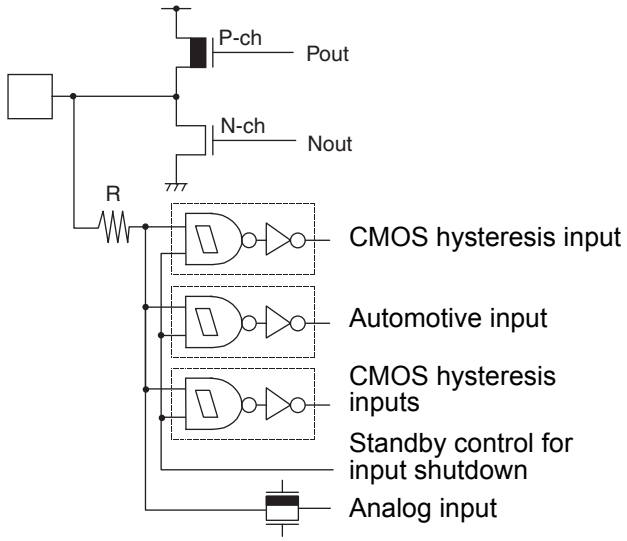
Type	Circuit	Remarks
L		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH}0.8Vcc V_{IL}0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • CMOS hysteresis input (V_{IH}0.7Vcc V_{IL}0.3Vcc) (With the standby-time input shutdown function) • A/D analog input

5. Handling Devices

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

■ A voltage higher than V_{CC} pin or lower than V_{SS} pin is applied to an input or output pin.

■ A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.

■ The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Use meticulous care not to exceed the rating.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVR) exceed the digital power-supply voltage.

2. Treatment of unused pins

Leaving unused input pins open may result in permanent damage of the device due to misbehavior or latch-up. Therefore, they must be pulled up or pulled down through resistors. In this case, those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

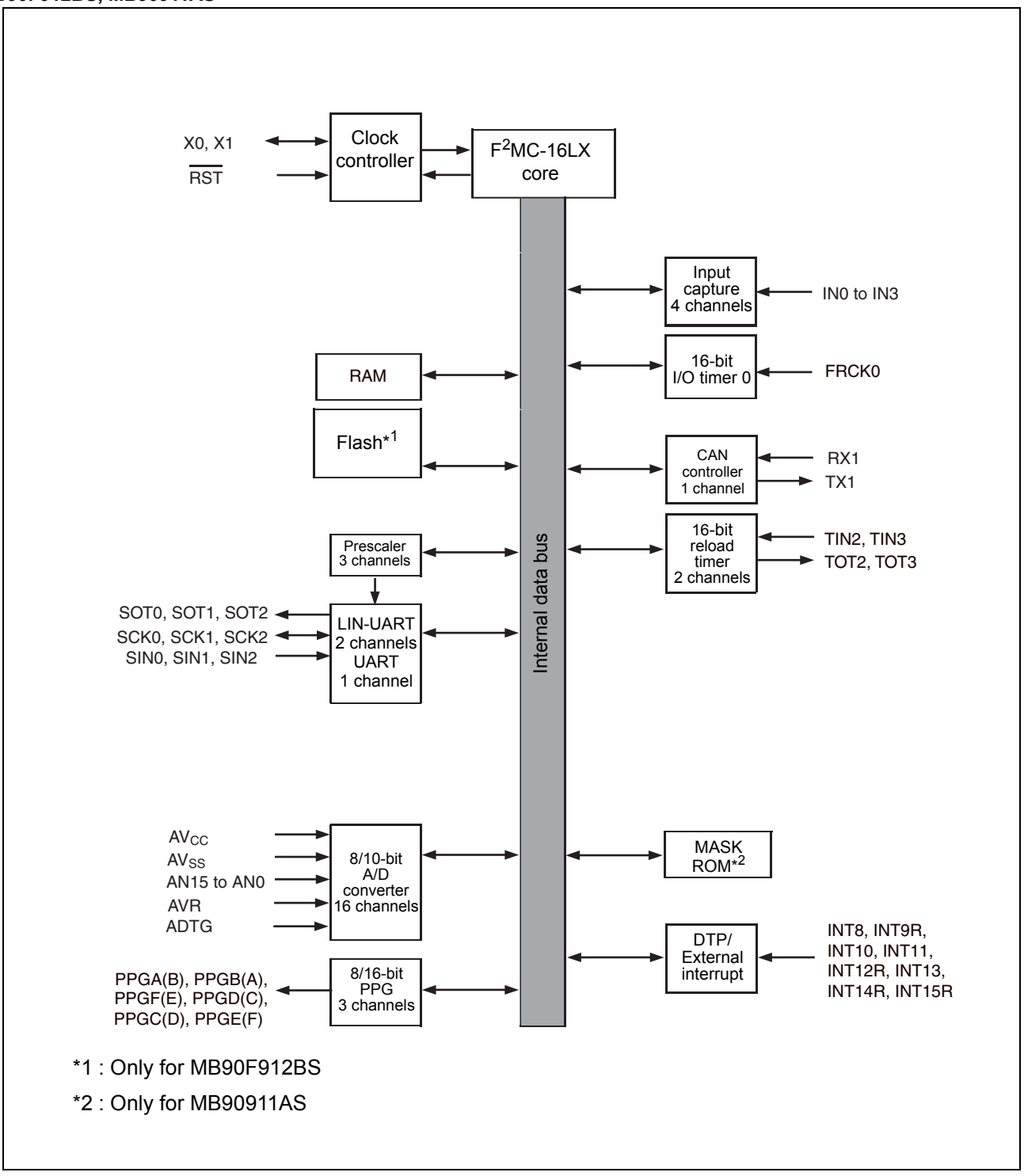
3. Using external clock

The high-speed oscillator pins (X0, X1) can not be used for external clock inputs.

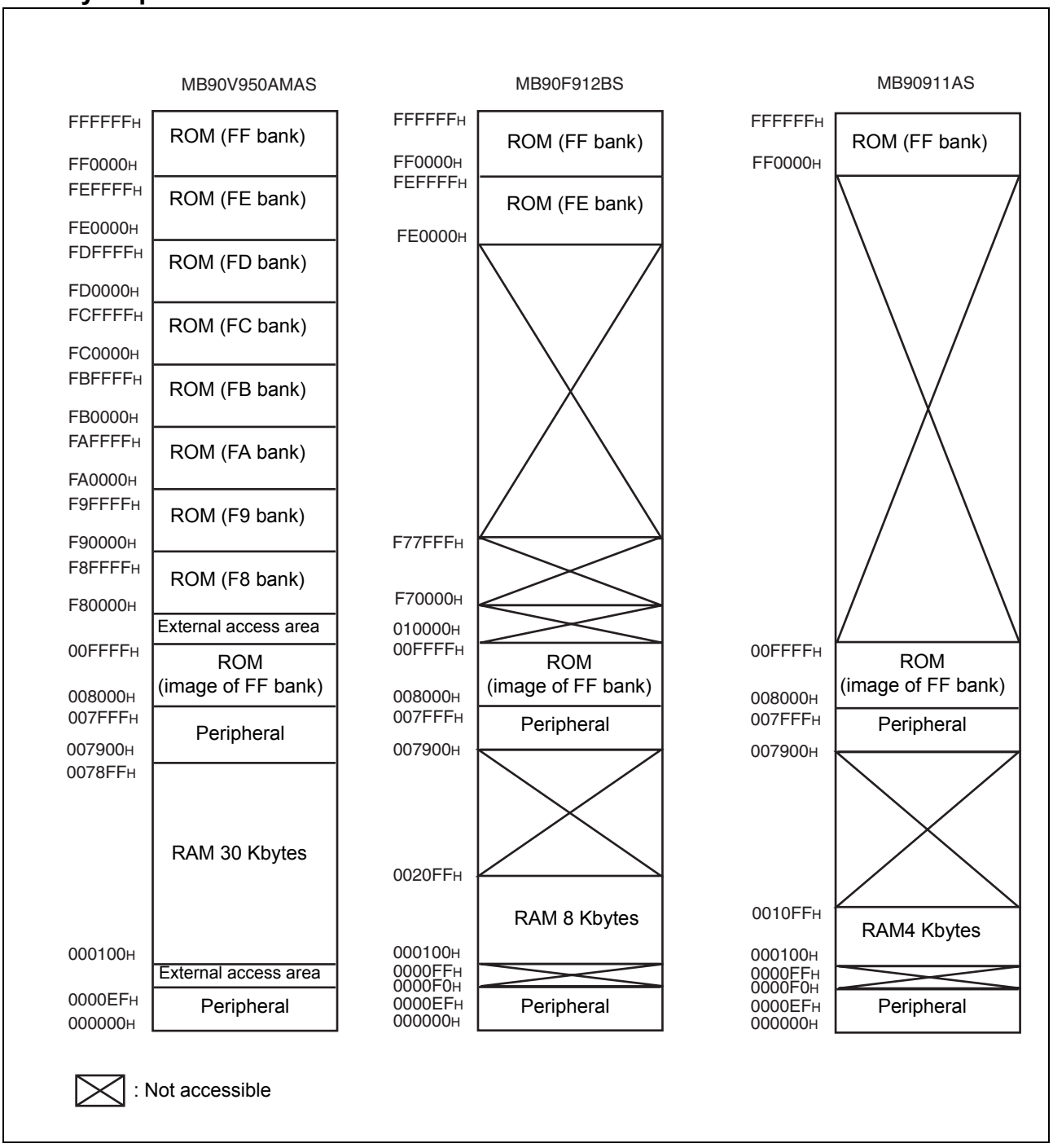
4. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

■ **MB90F912BS, MB90911AS**



7. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referred without using the far specification in the pointer declaration.
For example, an attempt to access $00C000_H$ practically accesses the value at $FFC000_H$ in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
000020_H	Serial Mode Register 0	SMR0	W, R/W	UART0	00000000_B
000021_H	Serial Control Register 0	SCR0	W, R/W		00000000_B
000022_H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000_B/ 11111111_B
000023_H	Serial Status Register 0	SSR0	R, R/W		00001000_B
000024_H	Extended Communication Control Register 0	ECCR0	R, W, R/W		$000000XX_B$
000025_H	Extended Status/Control Register 0	ESCR0	R/W		$00000X00_B$
000026_H	Baud Rate Generator Register 00	BGR00	R/W, R		00000000_B
000027_H	Baud Rate Generator Register 01	BGR01	R/W, R		00000000_B
000028_H	Serial Mode Register 1	SMR1	W, R/W	UART1	00000000_B
000029_H	Serial Control Register 1	SCR1	W, R/W		00000000_B
$00002A_H$	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000_B/ 11111111_B
$00002B_H$	Serial Status Register 1	SSR1	R, R/W		00001000_B
$00002C_H$	Extended Communication Control Register 1	ECCR1	R, W, R/W		$000000XX_B$
$00002D_H$	Extended Status/Control Register 1	ESCR1	R/W		$00000X00_B$
$00002E_H$	Baud Rate Generator Register 10	BGR10	R/W, R		00000000_B
$00002F_H$	Baud Rate Generator Register 11	BGR11	R/W, R		00000000_B
000030_H to $00003A_H$	Reserved				
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	11000000_B
$00003C_H$ to 000043_H	Reserved				
000044_H	PPGA Operation Mode Control Register	PPGCA	W, R/W	16-bit PPG A/B	01000111_B
000045_H	PPGB Operation Mode Control Register	PPGCB	W, R/W		01000001_B
000046_H	PPGA/B Count Clock Select Register	PPGAB	R/W		00000010_B
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W, R/W	16-bit PPG C/D	01000111_B
000049_H	PPG D Operation Mode Control Register	PPGCD	W, R/W		01000001_B
$00004A_H$	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		00000010_B
$00004B_H$	Reserved				

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Address	Register	Abbrevia-tion	Access	Resource name	Initial value
$0079A2_H$	Flash Write Control Register 0	FWR0	R/W	Flash	00000000_B
$0079A3_H$	Flash Write Control Register 1	FWR1	R/W		00000000_B
$0079A4_H$ to $0079B1_H$	Reserved				
$0079B2_H$	Reserved				
$0079B3_H$ to $0079B7_H$	Reserved				
$0079B8_H$	Reserved				
$0079B9_H$	Reserved				
$0079BA_H$	Reserved				
$0079BB_H$	Reserved				
$0079BC_H$	Reserved				
$0079BD_H$	Reserved				
$0079BE_H$	Reserved				
$0079BF_H$	Reserved				
$0079C0_H$ to $0079DF_H$	Reserved				
$0079E0_H$	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E1_H$	Detect Address Setting Register 0	PADR0	R/W		$XXXXXXXX_B$
$0079E2_H$	Detect Address Setting Register 0	PADR0	R/W		$XXXXXXXX_B$
$0079E3_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E4_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E5_H$	Detect Address Setting Register 1	PADR1	R/W		$XXXXXXXX_B$
$0079E6_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E7_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E8_H$	Detect Address Setting Register 2	PADR2	R/W		$XXXXXXXX_B$
$0079E9_H$ to $0079EF_H$	Reserved				

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Address	Register	Abbreviation	Access	Resource name	Initial value
$0079F0_H$	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	$XXXXXXXX_B$
$0079F1_H$	Detect Address Setting Register 3	PADR3	R/W		$XXXXXXXX_B$
$0079F2_H$	Detect Address Setting Register 3	PADR3	R/W		$XXXXXXXX_B$
$0079F3_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F4_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F5_H$	Detect Address Setting Register 4	PADR4	R/W		$XXXXXXXX_B$
$0079F6_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F7_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F8_H$	Detect Address Setting Register 5	PADR5	R/W		$XXXXXXXX_B$
$0079F9_H$ to $007BFF_H$	Reserved				
$007C00_H$ to $007CFF_H$	Reserved for CAN Controller. Refer to “CAN Controllers”				
$007D00_H$ to $007DFF_H$	Reserved for CAN Controller. Refer to “CAN Controllers”				
$007E00_H$ to $007FFF_H$	Reserved				

* : The initial value of MB90V950AMAS is $XXXXXXXX_B$.

Notes :
- Initial value of “X” represents undefined value.
- Do not write to reserved address in I/O map. A read access to reserved addresses results in reading “X”.

9. CAN Controllers

- Conforms to CAN Specification Ver 2.0 Part A and Part B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps/s to 1 Mbps/s (when input clock is at 16 MHz)

List of Control Registers (1)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
000080_H	Message buffer valid register	BVALR	R/W	$00000000\ 00000000_B$
000081_H				
000082_H	Transmit request register	TREQR	R/W	$00000000\ 00000000_B$
000083_H				
000084_H	Transmit cancel register	TCANR	W	$00000000\ 00000000_B$
000085_H				
000086_H	Transmission complete register	TCR	R/W	$00000000\ 00000000_B$
000087_H				
000088_H	Receive complete register	RCR	R/W	$00000000\ 00000000_B$
000089_H				
$00008A_H$	Remote request receiving register	RRTRR	R/W	$00000000\ 00000000_B$
$00008B_H$				
$00008C_H$	Receive overrun register	ROVRR	R/W	$00000000\ 00000000_B$
$00008D_H$				
$00008E_H$	Reception interrupt enable register	RIER	R/W	$00000000\ 00000000_B$
$00008F_H$				

List of Control Registers (2)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1\ 00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000\ XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive and transmit error counter	RTEC	R	$00000000\ 00000000_B$
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	$11111111\ X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	$00000000\ 00000000_B$
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	$00000000\ 00000000_B$
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX\ XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX\ XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX\ XXXXXXXX_B$
$007D1B_H$				

List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C60_H$	DLC register 0	DLCR0	R/W	$XXXXXXXX_B$
$007C61_H$				
$007C62_H$	DLC register 1	DLCR1	R/W	$XXXXXXXX_B$
$007C63_H$				
$007C64_H$	DLC register 2	DLCR2	R/W	$XXXXXXXX_B$
$007C65_H$				
$007C66_H$	DLC register 3	DLCR3	R/W	$XXXXXXXX_B$
$007C67_H$				
$007C68_H$	DLC register 4	DLCR4	R/W	$XXXXXXXX_B$
$007C69_H$				
$007C6A_H$	DLC register 5	DLCR5	R/W	$XXXXXXXX_B$
$007C6B_H$				
$007C6C_H$	DLC register 6	DLCR6	R/W	$XXXXXXXX_B$
$007C6D_H$				
$007C6E_H$	DLC register 7	DLCR7	R/W	$XXXXXXXX_B$
$007C6F_H$				
$007C70_H$	DLC register 8	DLCR8	R/W	$XXXXXXXX_B$
$007C71_H$				
$007C72_H$	DLC register 9	DLCR9	R/W	$XXXXXXXX_B$
$007C73_H$				
$007C74_H$	DLC register 10	DLCR10	R/W	$XXXXXXXX_B$
$007C75_H$				
$007C76_H$	DLC register 11	DLCR11	R/W	$XXXXXXXX_B$
$007C77_H$				
$007C78_H$	DLC register 12	DLCR12	R/W	$XXXXXXXX_B$
$007C79_H$				
$007C7A_H$	DLC register 13	DLCR13	R/W	$XXXXXXXX_B$
$007C7B_H$				
$007C7C_H$	DLC register 14	DLCR14	R/W	$XXXXXXXX_B$
$007C7D_H$				
$007C7E_H$	DLC register 15	DLCR15	R/W	$XXXXXXXX_B$
$007C7F_H$				

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007C80_H$ to $007C87_H$	Data register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C88_H$ to $007C8F_H$	Data register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C90_H$ to $007C97_H$	Data register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C98_H$ to $007C9F_H$	Data register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA0_H$ to $007CA7_H$	Data register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA8_H$ to $007CAF_H$	Data register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB0_H$ to $007CB7_H$	Data register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB8_H$ to $007CBF_H$	Data register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC0_H$ to $007CC7_H$	Data register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC8_H$ to $007CCF_H$	Data register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD0_H$ to $007CD7_H$	Data register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD8_H$ to $007CDF_H$	Data register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE0_H$ to $007CE7_H$	Data register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE8_H$ to $007CEF_H$	Data register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

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10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N	#08	$FFFFDC_H$	—	—
INT9 instruction	N	#09	$FFFFD8_H$	—	—
Exception	N	#10	$FFFFD4_H$	—	—
Reserved	N	#11	$FFFFD0_H$	ICR00	$0000B0_H$
Reserved	N	#12	$FFFFCC_H$		
CAN 1 reception	N	#13	$FFFFC8_H$	ICR01	$0000B1_H$
CAN 1 transmission/node status	N	#14	$FFFFC4_H$		
Reserved	N	#15	$FFFFC0_H$	ICR02	$0000B2_H$
Reserved	N	#16	$FFFFBC_H$		
Reserved	N	#17	$FFFFB8_H$	ICR03	$0000B3_H$
Reserved	N	#18	$FFFFB4_H$		
16-bit reload timer 2	Y1	#19	$FFFFB0_H$	ICR04	$0000B4_H$
16-bit reload timer 3	Y1	#20	$FFFFAC_H$		
Reserved	N	#21	$FFFFA8_H$	ICR05	$0000B5_H$
Reserved	N	#22	$FFFFA4_H$		
PPG C/D	N	#23	$FFFFA0_H$	ICR06	$0000B6_H$
PPG A/B/E/F	N	#24	$FFFF9C_H$		
Timebase timer	N	#25	$FFFF98_H$	ICR07	$0000B7_H$
External interrupt 8 to 11	Y1	#26	$FFFF94_H$		
Reserved	N	#27	$FFFF90_H$	ICR08	$0000B8_H$
External interrupt 12 to 15	Y1	#28	$FFFF8C_H$		
A/D converter	Y1	#29	$FFFF88_H$	ICR09	$0000B9_H$
I/O timer 0	N	#30	$FFFF84_H$		
Reserved	N	#31	$FFFF80_H$	ICR10	$0000BA_H$
Reserved	N	#32	$FFFF7C_H$		
Input capture 0 to 3	Y1	#33	$FFFF78_H$	ICR11	$0000BB_H$
Reserved	N	#34	$FFFF74_H$		
UART 0 reception	Y2	#35	$FFFF70_H$	ICR12	$0000BC_H$
UART 0 transmission	Y1	#36	$FFFF6C_H$		
UART 1 reception	Y2	#37	$FFFF68_H$	ICR13	$0000BD_H$
UART 1 transmission	Y1	#38	$FFFF64_H$		

(Continued)

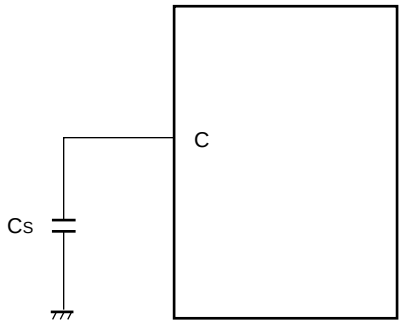
11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	3.0	5.0	5.5	V	Under normal operation
		2.6	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. By-pass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+105	°C	
		−40	—	+125	°C	*

* : For the restricted reliability, contact us if use the devices over Ta=+105 °C.
It is ensured to write/erase data to the Flash memory between T_A = −40 °C and +105 °C.

- **C Pin Connection Diagram**



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

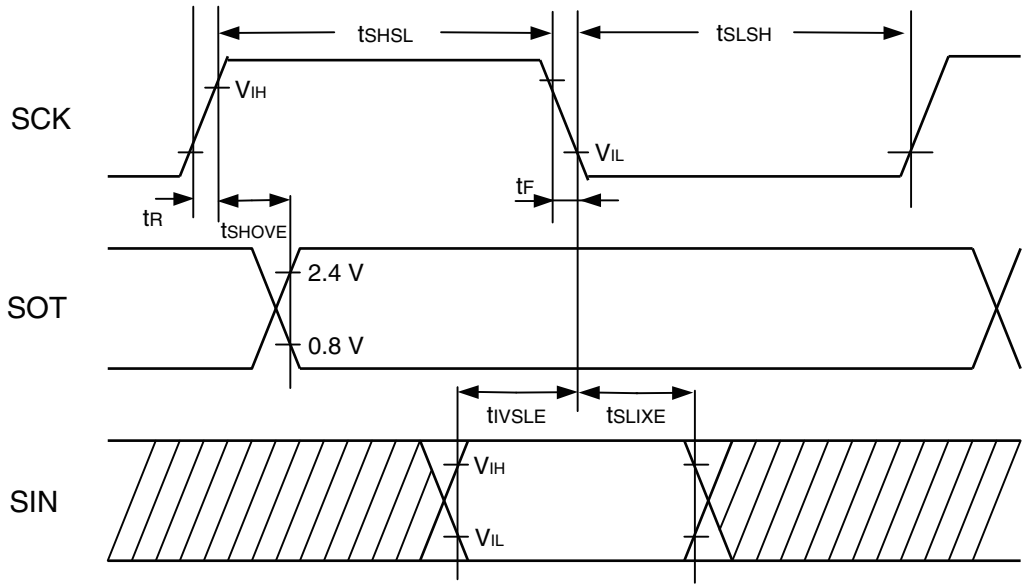
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(Continued)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 32 MHz, At normal operation.	—	30	40	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	22.5	30	mA	
			V_{CC} = 5.0 V, Internal frequency : 2 MHz, At normal operation.	—	3	7	mA	
			V_{CC} = 5.0 V, Internal frequency : 32 MHz, At writing Flash memory.	—	50	65	mA	
			V_{CC} = 5.0 V, Internal frequency : 32 MHz, At erasing Flash memory.	—	50	65	mA	
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 32 MHz, At sleep mode.	—	13	23	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At main timer mode	—	0.3	0.9	mA	
	$I_{CTSPLL8}$		V_{CC} = 5.0 V, Internal frequency : 32 MHz, At PLL timer mode, External frequency = 4 MHz	—	4	7	mA	
	I_{CCH}		V_{CC} = 5.0 V, At stop mode, T_A = +25°C	—	25	100	μA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, V_{CC}, V_{SS}, C	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

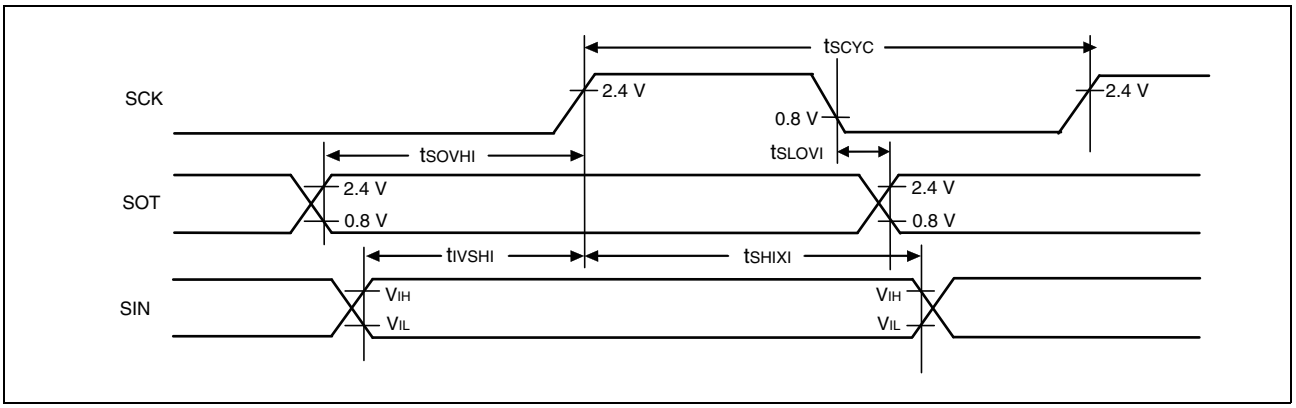


External Clock Shift Operation

ESCR : SCES = 1, ECCR : SCDE = 1

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal clock operation C_L = 80pF + 1TTL.	5 tcp*	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}		– 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp + 80	–	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}		3 tcp – 70	–	ns

*: The tcp indicates machine clock



11.4.5 Trigger Input Timing

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8, INT9R INT10, INT11 INT12R, INT13 INT14R, INT15R ADTG	—	5 t_{CP}	—	ns

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.