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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f912bspmc-ge1

DTP/External interrupt : up to 8 channels, CAN wakeup : up to 1 channel

Module for activation of expanded intelligent I/O service (EI^{2}OS) and generation of external interrupt by external input

Delay interrupt generator module

Generates interrupt request for task switching

8/10-bit A/D converter : 16 channels

- Resolution is selectable between 8-bit and 10-bit
- Activation by external trigger input is allowed
- Conversion time : 3 µs (at 24 MHz machine clock, including sampling time)

Program patch function

Address matching detection for 6 address pointers

Capable of changing input voltage for port

Automotive/CMOS-Schmitt input level (initial level is Automotive in single-chip mode)

ROM security function

The content of ROM can be protected (Only MASK ROM product).

Flash memory security function

Protects the content of Flash memory

Contents

3. Pin Description

Pin No.	Pin name	I/O circuit type*	Function
1	AV_{CC}	I	V_{CC} power input pin for analog circuit.
2	AVR	—	Power (Vref+) input pin for A/D converter. It should be below V_{CC}.
3 to 7	P60 to P64	H	General-purpose I/O port.
	AN0 to AN4		Analog input pins for A/D converter.
8 to 10	P65 to P67	H	General-purpose I/O port.
	AN5 to AN7		Analog input pins for A/D converter.
	PPGA (B) , PPGC (D) , PPGE (F)		Output pins for PPG.
11	P80	F	General-purpose I/O port.
	ADTG		Trigger input pin for A/D converter.
	INT12R		External interrupt request input pin for INT12R.
12	P50	L	General-purpose I/O port.
	AN8		Analog input pin for A/D converter.
	SIN2		Serial data input pin for UART2.
13	P51	H	General-purpose I/O port.
	AN9		Analog input pin for A/D converter.
	SOT2		Serial data output pin for UART2.
14	P52	H	General-purpose I/O port.
	AN10		Analog input pin for A/D converter.
	SCK2		Clock I/O pin for UART2.
15	P53	H	General-purpose I/O port.
	AN11		Analog input pin for A/D converter.
	TIN3		Event input pin for reload timer 3.
16	P54	H	General-purpose I/O port.
	AN12		Analog input pin for A/D converter.
	TOT3		Output pin for reload timer 3
	INT8		External interrupt request input pin for INT8.
17	P55	H	General-purpose I/O port.
	AN13		Analog input pin for A/D converter.
	INT10		External interrupt request input pin for INT10.

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Pin No.	Pin name	I/O circuit type*	Function
18	P56	H	General-purpose I/O port (Different I/O circuit type from MB90V950AMAS).
	AN14		Analog input pin for A/D converter.
	INT11		External interrupt request input pin for INT11.
19	P57	H	General-purpose I/O port (Different I/O circuit type from MB90V950AMAS).
	AN15		Analog input pin for A/D converter.
	INT13		External interrupt request input pin for INT13.
20	MD2	D	Input pin for operation mode specification.
21, 22	MD1, MD0	C	Input pins for operation mode specification.
23	$\overline{RST}$	E	Reset input pin.
24	V_{CC}	—	Power input pin (3.5 V to 5.5 V) .
25	V_{SS}	—	Power input pin (0 V) .
26	C	I	Power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic condenser.
27	X0	A	Oscillation input pin.
28	X1		Oscillation output pin.
29 to 32	P27 to P24	G	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	IN3 to IN0		Event input pins for input capture 0 to 3.
33 to 35	P23 to P21	J	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. High current output port (Different I/O circuit type from MB90V950AMAS).
	PPGF (E) , PPGD (C) , PPGB(A)		Output pins for PPG.
36	P20	J	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. High current output port (Different I/O circuit type from MB90V950AMAS).
37	P85	K	General-purpose I/O port.
	SIN1		Serial data input pin for UART1.
38	P87	F	General-purpose I/O port.
	SCK1		Clock I/O pin for UART1.
39	P86	F	General-purpose I/O port.
	SOT1		Serial data output pin for UART1.

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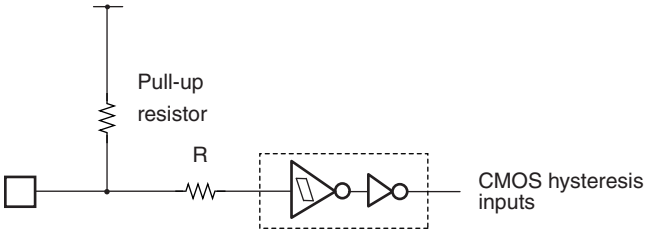
Type	Circuit	Remarks
E		CMOS hysteresis input pin

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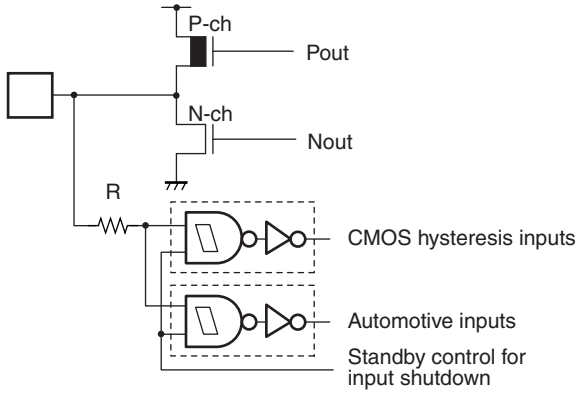
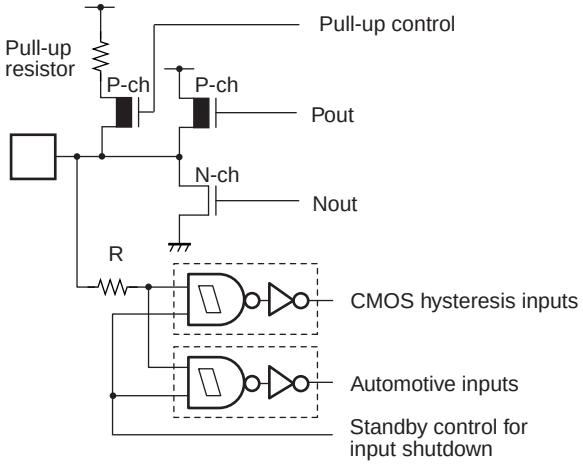
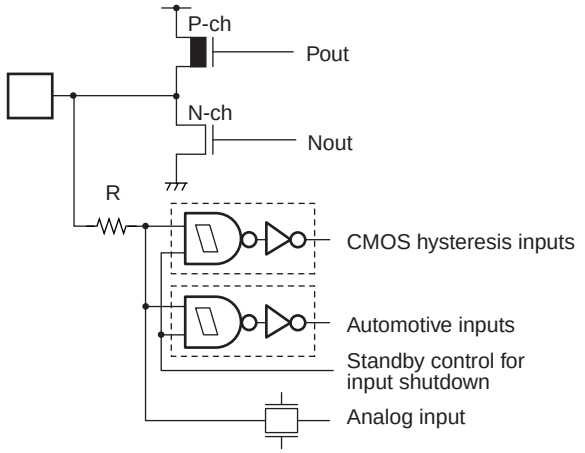
Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS hysteresis inputs (V_{IH}0.8Vcc V_{IL}0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS hysteresis inputs (V_{IH}0.8Vcc V_{IL}0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
H		• CMOS level output (I_{OL} = 4 mA, I_{OH} = − 4 mA) • CMOS hysteresis inputs (V_{IH}0.8Vcc V_{IL}0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input

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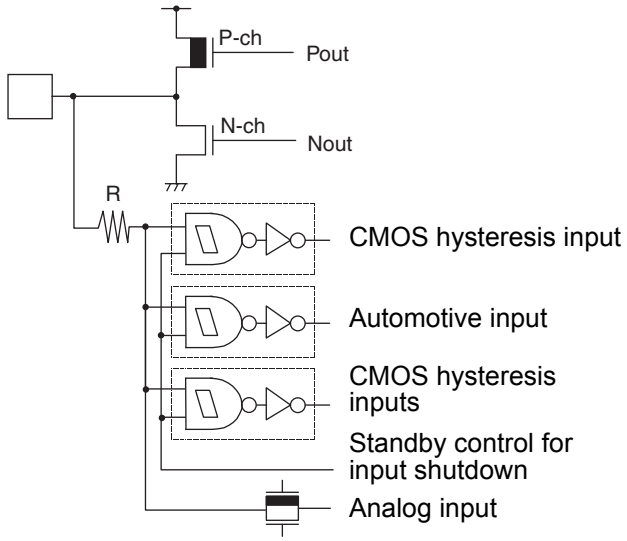
Type	Circuit	Remarks
L		• CMOS level output (I_{OL} = 4 mA, I_{OH} = – 4 mA) • CMOS hysteresis inputs (V_{IH}0.8Vcc V_{IL}0.2Vcc) (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • CMOS hysteresis input (V_{IH}0.7Vcc V_{IL}0.3Vcc) (With the standby-time input shutdown function) • A/D analog input

5. Handling Devices

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

■ A voltage higher than V_{CC} pin or lower than V_{SS} pin is applied to an input or output pin.

■ A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.

■ The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Use meticulous care not to exceed the rating.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVR) exceed the digital power-supply voltage.

2. Treatment of unused pins

Leaving unused input pins open may result in permanent damage of the device due to misbehavior or latch-up. Therefore, they must be pulled up or pulled down through resistors. In this case, those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

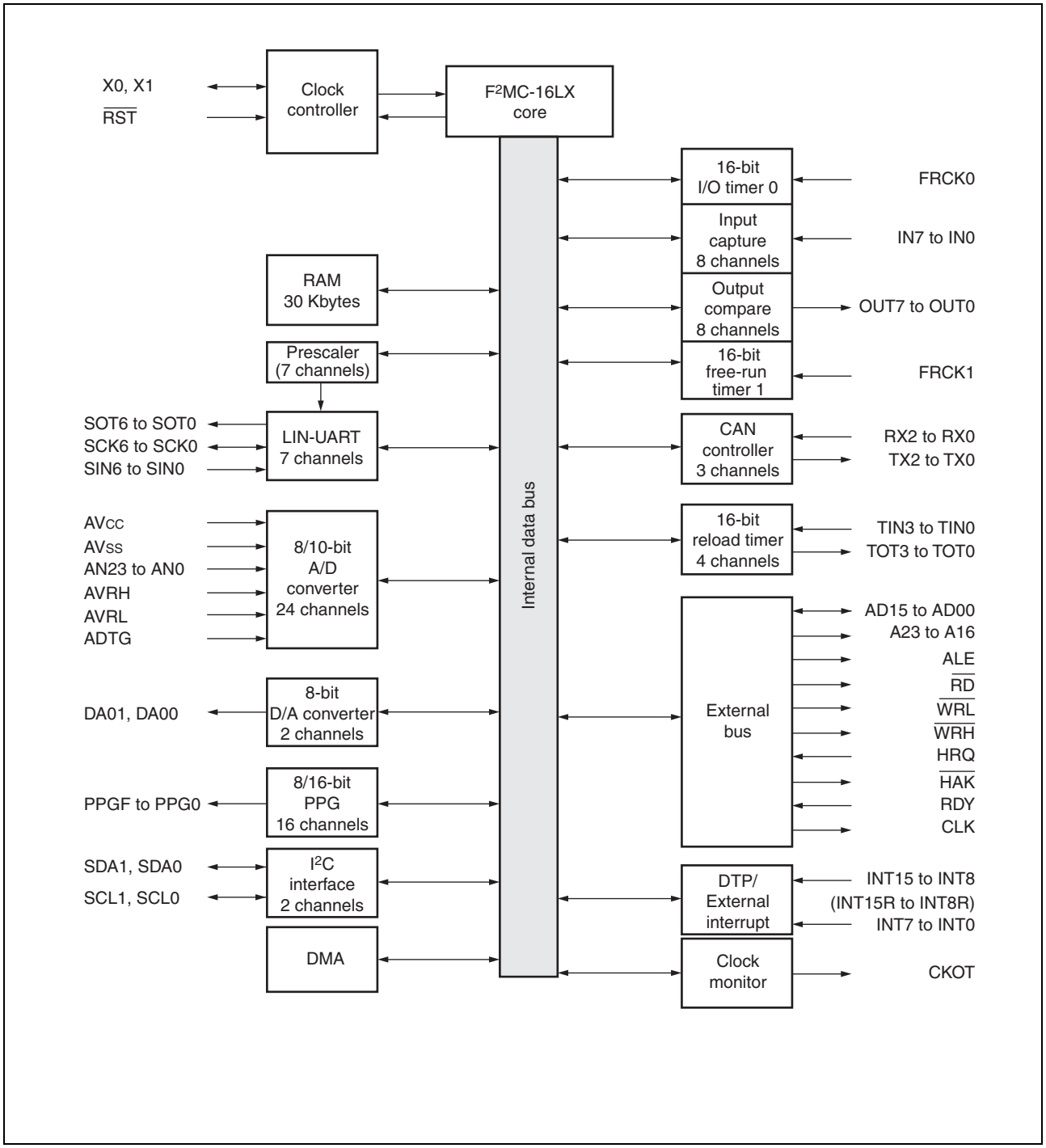
The high-speed oscillator pins (X0, X1) can not be used for external clock inputs.

4. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

6. Block Diagrams

■ **MB90V950AMAS**



Address	Register	Abbreviation	Access	Resource name	Initial value
000020_H	Serial Mode Register 0	SMR0	W, R/W	UART0	00000000_B
000021_H	Serial Control Register 0	SCR0	W, R/W		00000000_B
000022_H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000_B/ 11111111_B
000023_H	Serial Status Register 0	SSR0	R, R/W		00001000_B
000024_H	Extended Communication Control Register 0	ECCR0	R, W, R/W		$000000XX_B$
000025_H	Extended Status/Control Register 0	ESCR0	R/W		$00000X00_B$
000026_H	Baud Rate Generator Register 00	BGR00	R/W, R		00000000_B
000027_H	Baud Rate Generator Register 01	BGR01	R/W, R		00000000_B
000028_H	Serial Mode Register 1	SMR1	W, R/W	UART1	00000000_B
000029_H	Serial Control Register 1	SCR1	W, R/W		00000000_B
$00002A_H$	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000_B/ 11111111_B
$00002B_H$	Serial Status Register 1	SSR1	R, R/W		00001000_B
$00002C_H$	Extended Communication Control Register 1	ECCR1	R, W, R/W		$000000XX_B$
$00002D_H$	Extended Status/Control Register 1	ESCR1	R/W		$00000X00_B$
$00002E_H$	Baud Rate Generator Register 10	BGR10	R/W, R		00000000_B
$00002F_H$	Baud Rate Generator Register 11	BGR11	R/W, R		00000000_B
000030_H to $00003A_H$	Reserved				
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	11000000_B
$00003C_H$ to 000043_H	Reserved				
000044_H	PPGA Operation Mode Control Register	PPGCA	W, R/W	16-bit PPG A/B	01000111_B
000045_H	PPGB Operation Mode Control Register	PPGCB	W, R/W		01000001_B
000046_H	PPGA/B Count Clock Select Register	PPGAB	R/W		00000010_B
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W, R/W	16-bit PPG C/D	01000111_B
000049_H	PPG D Operation Mode Control Register	PPGCD	W, R/W		01000001_B
$00004A_H$	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		00000010_B
$00004B_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$00004C_H$	PPG E Operation Mode Control Register	PPGCE	W, R/W	16-bit PPG E/F	01000111_B
$00004D_H$	PPG F Operation Mode Control Register	PPGCF	W, R/W		01000001_B
$00004E_H$	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		00000010_B
$00004F_H$	Reserved				
000050_H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge 0/1	ICE01	R/W, R		$111010XX_B$
000052_H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000_B
000053_H	Input Capture Edge 2/3	ICE23	R		$111111XX_B$
000054_H to 000063_H	Reserved				
000064_H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status 2	TMCSR2	R/W		11110000_B
000066_H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status 3	TMCSR3	R/W		11110000_B
000068_H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00011110_B
000069_H	A/D Control Status 1	ADCS1	R/W, W		00000001_B
$00006A_H$	A/D Data 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data 1	ADCR1	R		11111100_B
$00006C_H$	A/D Converter Setting 0	ADSR0	R/W		00000000_B
$00006D_H$	A/D Converter Setting 1	ADSR1	R/W		00000000_B
$00006E_H$	Reserved				
$00006F_H$	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	11111101_B
000070_H to $00007F_H$	Reserved				
000080_H to $00008F_H$	Reserved for CAN Controller 1. Refer to "CAN Controllers"				
000090_H to $00009D_H$	Reserved				
$00009E_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	11000000_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000C1_H$	Reserved				
$0000C2_H$	Reserved				
$0000C3_H$ to $0000C9_H$	Reserved				
$0000CA_H$	External Interrupt Enable 1	ENIR1	R/W	DTP/External Interrupt	00000000_B
$0000CB_H$	External Interrupt Source 1	EIRR1	R/W		$XXXXXXXX_B$
$0000CC_H$	Detection Level Setting 1	ELVR1	R/W		00000000_B
$0000CD_H$					00000000_B
$0000CE_H$	External Interrupt Source Select	EISSR	R/W		00000000_B
$0000CF_H$	PLL clock Control Register	PSCCR	W	PLL	11110000_B
$0000D0_H$ to $0000D7_H$	Reserved				
$0000D8_H$	Serial Mode Register 2	SMR2	W, R/W	UART2	00000000_B
$0000D9_H$	Serial Control Register 2	SCR2	W, R/W		00000000_B
$0000DA_H$	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000_B/ 11111111_B
$0000DB_H$	Serial Status Register 2	SSR2	R, R/W		00001000_B
$0000DC_H$	Extended Communication Control Register 2	ECCR2	R, W, R/W		$000000XX_B$
$0000DD_H$	Extended Status/Control Register 2	ESCR2	R/W		$00000X00_B$
$0000DE_H$	Baud Rate Generator Register 20	BGR20	R/W, R		00000000_B
$0000DF_H$	Baud Rate Generator Register 21	BGR21	R/W, R		00000000_B
$0000E0_H$ to $0000FF_H$	Reserved				
007900_H to 007913_H	Reserved				
007914_H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$

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List of Control Registers (2)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1\ 00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000\ XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive and transmit error counter	RTEC	R	$00000000\ 00000000_B$
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	$11111111\ X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	$00000000\ 00000000_B$
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	$00000000\ 00000000_B$
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX\ XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX\ XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX\ XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX\ XXXXXXXX_B$
$007D1B_H$				

List of Message Buffers (DLC Registers and Data Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C60_H$	DLC register 0	DLCR0	R/W	$XXXXXXXX_B$
$007C61_H$				
$007C62_H$	DLC register 1	DLCR1	R/W	$XXXXXXXX_B$
$007C63_H$				
$007C64_H$	DLC register 2	DLCR2	R/W	$XXXXXXXX_B$
$007C65_H$				
$007C66_H$	DLC register 3	DLCR3	R/W	$XXXXXXXX_B$
$007C67_H$				
$007C68_H$	DLC register 4	DLCR4	R/W	$XXXXXXXX_B$
$007C69_H$				
$007C6A_H$	DLC register 5	DLCR5	R/W	$XXXXXXXX_B$
$007C6B_H$				
$007C6C_H$	DLC register 6	DLCR6	R/W	$XXXXXXXX_B$
$007C6D_H$				
$007C6E_H$	DLC register 7	DLCR7	R/W	$XXXXXXXX_B$
$007C6F_H$				
$007C70_H$	DLC register 8	DLCR8	R/W	$XXXXXXXX_B$
$007C71_H$				
$007C72_H$	DLC register 9	DLCR9	R/W	$XXXXXXXX_B$
$007C73_H$				
$007C74_H$	DLC register 10	DLCR10	R/W	$XXXXXXXX_B$
$007C75_H$				
$007C76_H$	DLC register 11	DLCR11	R/W	$XXXXXXXX_B$
$007C77_H$				
$007C78_H$	DLC register 12	DLCR12	R/W	$XXXXXXXX_B$
$007C79_H$				
$007C7A_H$	DLC register 13	DLCR13	R/W	$XXXXXXXX_B$
$007C7B_H$				
$007C7C_H$	DLC register 14	DLCR14	R/W	$XXXXXXXX_B$
$007C7D_H$				
$007C7E_H$	DLC register 15	DLCR15	R/W	$XXXXXXXX_B$
$007C7F_H$				

(Continued)

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N	#08	$FFFFDC_H$	—	—
INT9 instruction	N	#09	$FFFFD8_H$	—	—
Exception	N	#10	$FFFFD4_H$	—	—
Reserved	N	#11	$FFFFD0_H$	ICR00	$0000B0_H$
Reserved	N	#12	$FFFFCC_H$		
CAN 1 reception	N	#13	$FFFFC8_H$	ICR01	$0000B1_H$
CAN 1 transmission/node status	N	#14	$FFFFC4_H$		
Reserved	N	#15	$FFFFC0_H$	ICR02	$0000B2_H$
Reserved	N	#16	$FFFFBC_H$		
Reserved	N	#17	$FFFFB8_H$	ICR03	$0000B3_H$
Reserved	N	#18	$FFFFB4_H$		
16-bit reload timer 2	Y1	#19	$FFFFB0_H$	ICR04	$0000B4_H$
16-bit reload timer 3	Y1	#20	$FFFFAC_H$		
Reserved	N	#21	$FFFFA8_H$	ICR05	$0000B5_H$
Reserved	N	#22	$FFFFA4_H$		
PPG C/D	N	#23	$FFFFA0_H$	ICR06	$0000B6_H$
PPG A/B/E/F	N	#24	$FFFF9C_H$		
Timebase timer	N	#25	$FFFF98_H$	ICR07	$0000B7_H$
External interrupt 8 to 11	Y1	#26	$FFFF94_H$		
Reserved	N	#27	$FFFF90_H$	ICR08	$0000B8_H$
External interrupt 12 to 15	Y1	#28	$FFFF8C_H$		
A/D converter	Y1	#29	$FFFF88_H$	ICR09	$0000B9_H$
I/O timer 0	N	#30	$FFFF84_H$		
Reserved	N	#31	$FFFF80_H$	ICR10	$0000BA_H$
Reserved	N	#32	$FFFF7C_H$		
Input capture 0 to 3	Y1	#33	$FFFF78_H$	ICR11	$0000BB_H$
Reserved	N	#34	$FFFF74_H$		
UART 0 reception	Y2	#35	$FFFF70_H$	ICR12	$0000BC_H$
UART 0 transmission	Y1	#36	$FFFF6C_H$		
UART 1 reception	Y2	#37	$FFFF68_H$	ICR13	$0000BD_H$
UART 1 transmission	Y1	#38	$FFFF64_H$		

(Continued)

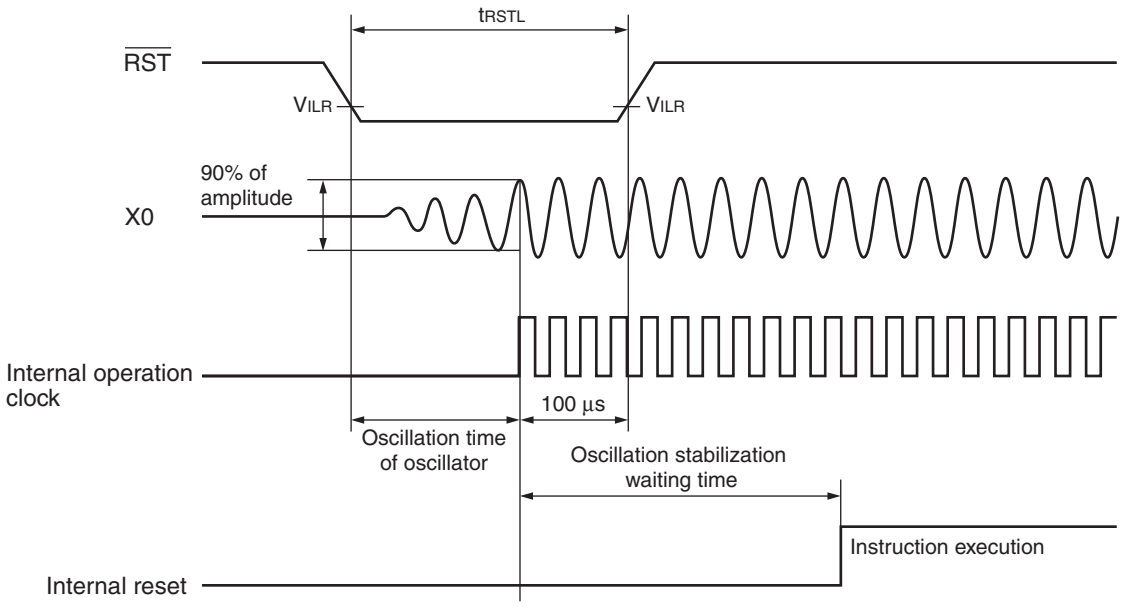
11.4.2 Reset Standby Input

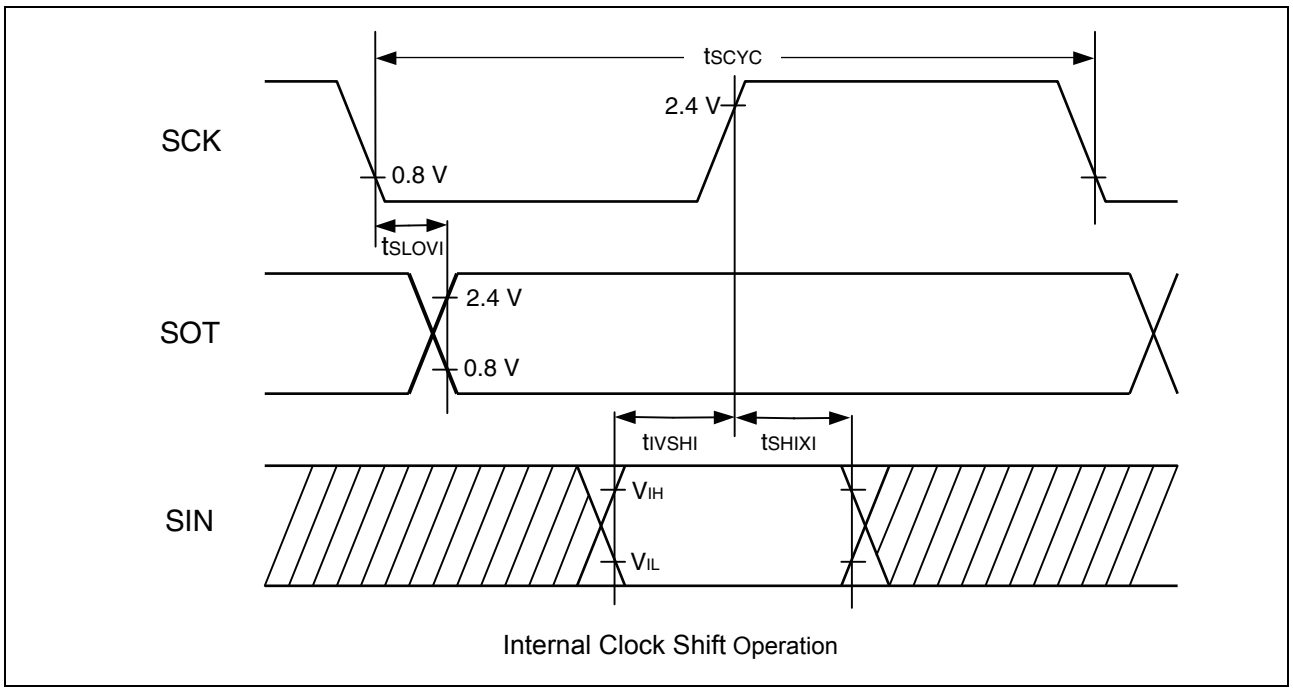
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In stop mode
			100	—	µs	In timebase timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. An External clock of oscillation time is 0 ms.

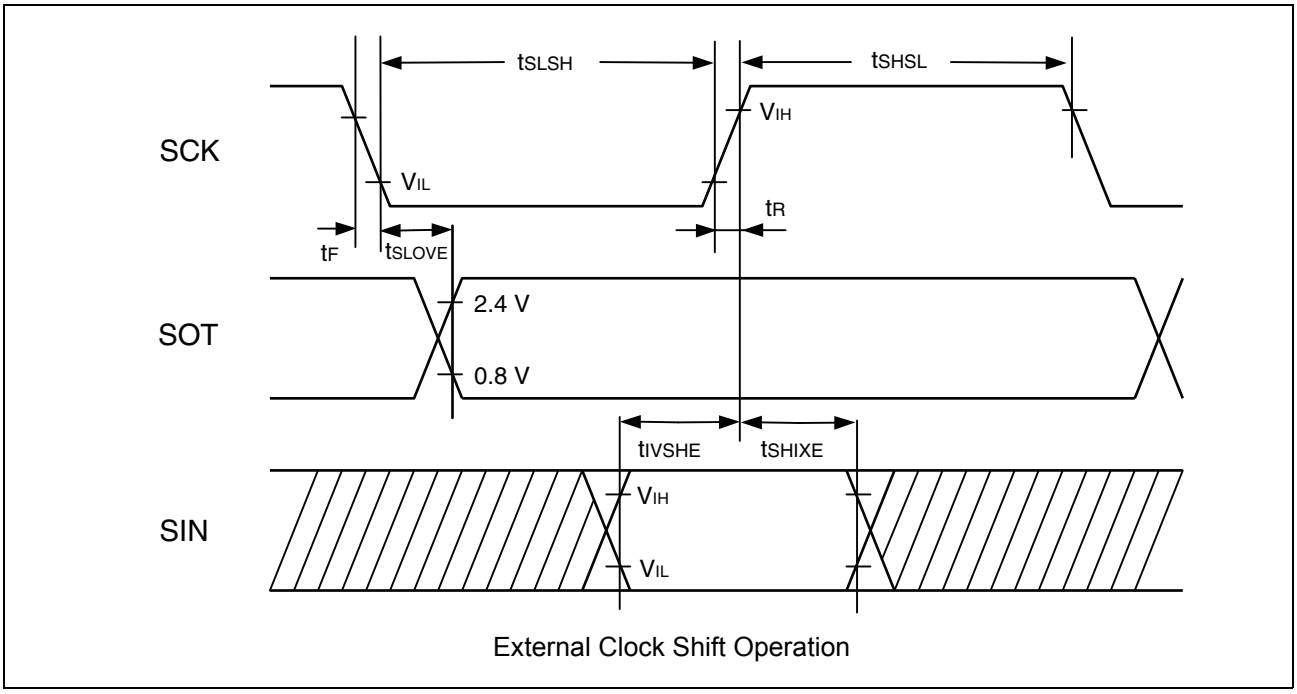
- **Under normal operation :**

- **In stop mode**





Internal Clock Shift Operation

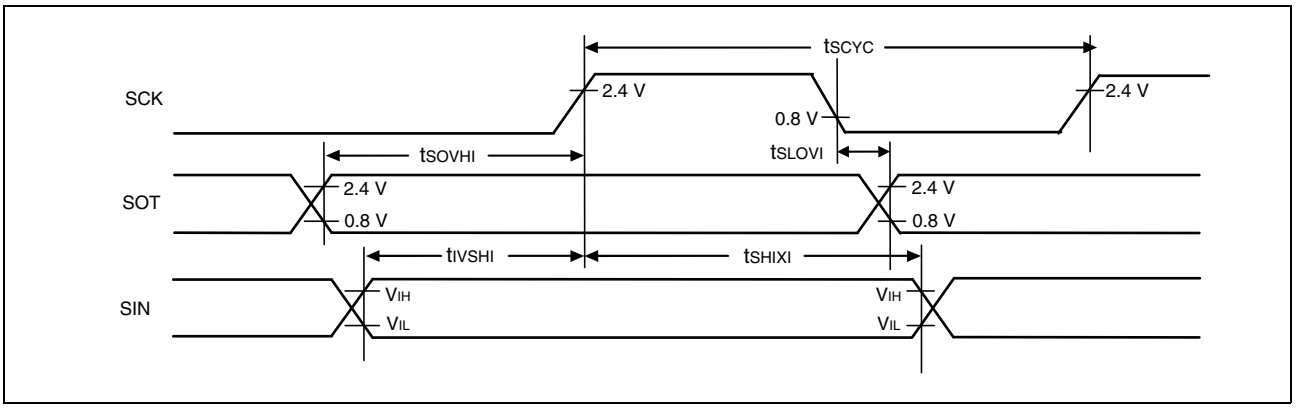


External Clock Shift Operation

ESCR : SCES = 1, ECCR : SCDE = 1

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal clock operation C_L = 80pF + 1TTL.	5 tcp*	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}		– 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp + 80	–	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}		3 tcp – 70	–	ns

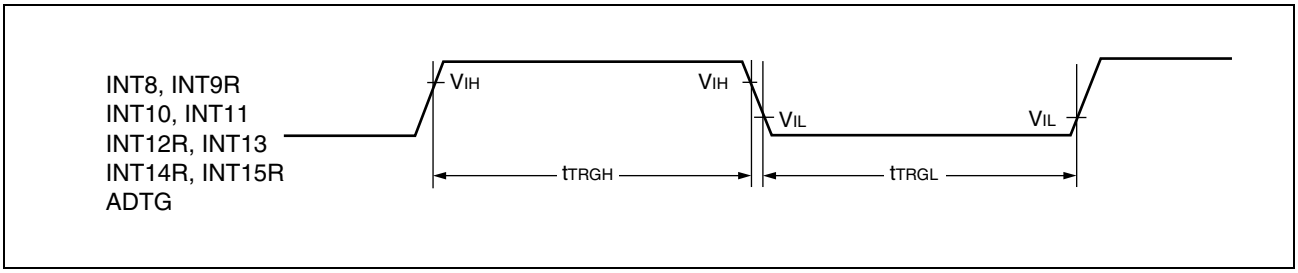
*: The tcp indicates machine clock



11.4.5 Trigger Input Timing

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8, INT9R INT10, INT11 INT12R, INT13 INT14R, INT15R ADTG	—	5 t_{CP}	—	ns

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.



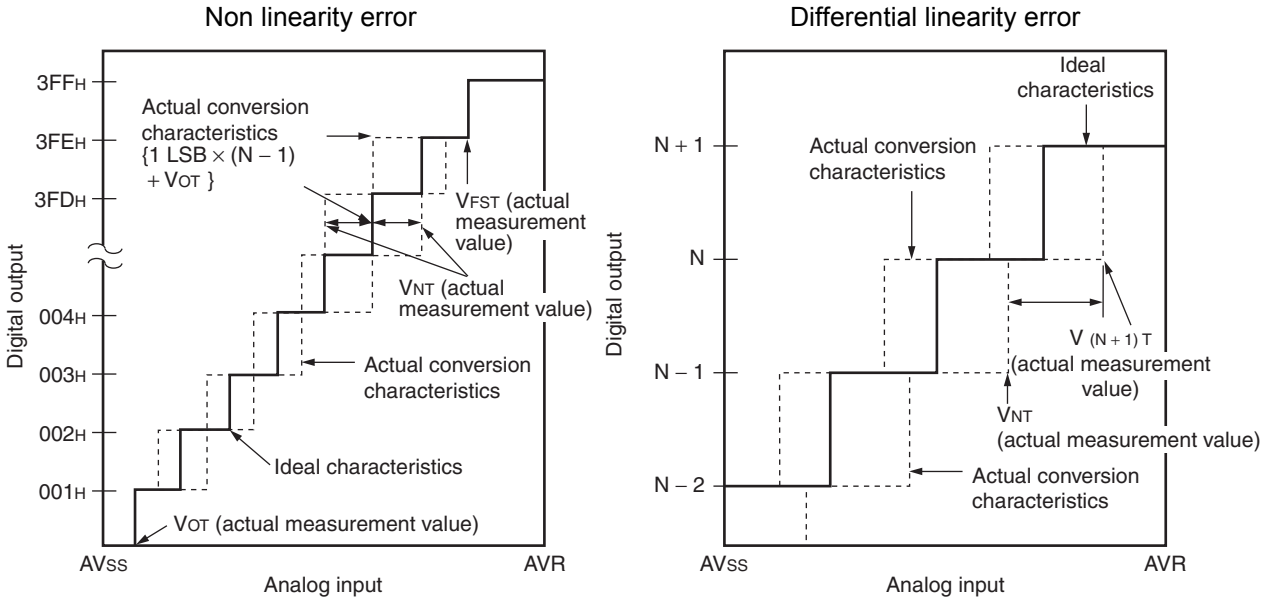
11.5 A/D Converter

($3.0\ V \le AVR = AV_{SS}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5LSB	AV_{SS} + 0.5LSB	AV_{SS} + 2.5LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN15	AVR – 3.5LSB	AVR – 1.5LSB	AVR + 0.5LSB	V	
Compare time	—	—	0.66	—	16500	µs	$4.5\ V \le AV_{CC} \le 5.5\ V$
			2.2				$3.0\ V \le AV_{CC} < 4.5\ V$
Sampling time	—	—	0.4	—	∞	µs	$4.5\ V \le AV_{CC} \le 5.5\ V$
			1.0				$3.0\ V \le AV_{CC} <$ 4.5 V
Analog port input current	I_{AIN}	AN0 to AN15	– 3	—	+ 3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN15	AV_{SS}	—	AVR	V	
Reference voltage range	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVR	—	600	900	µA	
	I_{RH}	AVR	—	—	5	µA	*
Offset between input channels	—	AN0 to AN15	—	—	4	LSB	

* : If A/D converter is not operating, a current when CPU is stopped is applicable ($V_{CC} = AV_{CC} = AVR = 5.0\ V$) .

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."