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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SC3850, Security; SEC 4.4
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=bsc9132nse7knkb

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_CLE/ GPO48	NAND Command Latch Enable/GPCM Write Byte Select1	L25	O	BVDD	18
IFC_OE_B/ GPO49	NOR Output Enable/NAND Read Enable/ GPCM Output Enable/Generic ASIC Interface Read-Write Indicator	K23	O	BVDD	2
IFC_WP_B/ GPO66	IFC Write Protect	K26	O	BVDD	18
IFC_RB_B/ GPO50	IFC Read Busy/GPCM External Transreciver/ Generic ASIC i/f Ready Indicator	K25	I	BVDD	—
IFC_BCTL/ GPO67	Data Buffer Control	K22	O	BVDD	18
IFC_CLK00/ GPO68	IFC Clock	K27	O	BVDD	—
eSDHC					
SDHC_CLK/ SIM_CLK/ GPO52	SDHC Clock	B27	O	BVDD	—
SDHC_CMD/ SIM_RST_B/ GPIO48	SDHC Command	C26	I/O	BVDD	15
SDHC_DATA00/ SIM_TRXD/ GPIO49	SDHC Data2 in all modes	D25	I/O	BVDD	15
SDHC_DATA01/ SIM_SVEN/ GPIO50	SDHC Data1 in 4-bit mode	F23	I/O	BVDD	15
SDHC_DATA02/ SIM_PD/ GPIO51	SDHC Data2 in 4-bit mode	F24	I/O	BVDD	15
SDHC_DATA03/ DMA_DDONE_B00/ CKSTP1_IN_B/ GPIO77	SDHC Data3 in 1-bit mode SDHC Data3 in 4-bit mode	E25	I/O	BVDD	15,16
SDHC_WP/ DMA_DREQ_B00/ CKSTP0_IN_B/ GPIO78	SDHC Write Protect Detect	G23	I	BVDD	—
SDHC_CD/ DMA_DACK_B00/ MCP1_B/ GPIO79/ IRQ10	SDHC Card Detect	C25	I	BVDD	—
USIM					

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SDHC_CLK/ **SIM_CLK**/ GPO52	SIM Clock	B27	O	BVDD	—
SDHC_CMD/ **SIM_RST_B**/ GPIO48	SIM Reset	C26	O	BVDD	17
SDHC_DATA00/ **SIM_TRXD**/ GPIO49	SIM TX RX Data	D25	I/O	BVDD	15
SDHC_DATA01/ **SIM_SVEN**/ GPIO50	SIM Enable	F23	O	BVDD	17
SDHC_DATA02/ **SIM_PD**/ GPIO51	SIM Card Detect	F24	I	BVDD	17
USIM over SPI1					
SPI1_CLK/ **SIM_CLK**	SIM Clock	M27	O	CVDD	—
SPI1_MISO/ UART_CTS_B03/ **SIM_RST_B**/ GPIO55	SIM Reset	M22	O	CVDD	17
SPI1_CS0_B/ UART_RTS_B03/ **SIM_TRXD**	SIM TX RX Data	M28	I/O	CVDD	15
SPI1_MOSI/ UART_SIN03/ **SIM_SVEN**/ GPIO54	SIM Enable	L22	O	CVDD	17
UART_CTS_B00/ **SIM_PD/** TIMER04/ GPIO42/ IRQ04	SIM Card Detect	AB27	I	OVDD	17
USB					
USB_CLK/ UART_SIN02/ GPIO69/ IRQ11/ TIMER03	ULPI Clock	R24	I	CVDD	—
USB_D07/ UART_SOUT02/ GPIO70	ULPI Data	P28	I/O	CVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT3_RX_CLK/ TDM2_TCK/ **GPIO04**	General Purpose I/O	D1	I/O	X2VDD	—
ANT4_RX_FRAME/ **GPIO05**	General Purpose I/O	Y5	I/O	X1VDD	—
ANT1_DIO108/ **GPIO21**/ IRQ08	General Purpose I/O	T7	I/O	X1VDD	—
ANT1_DIO109/ **GPIO22**/ IRQ09	General Purpose I/O	U1	I/O	X1VDD	—
ANT1_DIO110/ TIMER06/ **GPIO23**	General Purpose I/O	U2	I/O	X1VDD	—
ANT1_DIO111/ TIMER07/ **GPIO24**	General Purpose I/O	U3	I/O	X1VDD	—
ANT2_DIO000/ USB_D00/ **GPIO25**	General Purpose I/O	E2	I/O	X2VDD	—
ANT2_DIO001/ USB_D01/ **GPIO26**	General Purpose I/O	E1	I/O	X2VDD	—
ANT2_DIO002/ USB_D02/ **GPIO27**	General Purpose I/O	J6	I/O	X2VDD	—
ANT2_DIO003/ USB_D03/ **GPIO28**	General Purpose I/O	J5	I/O	X2VDD	—
ANT2_DIO004/ USB_D04/ **GPIO29**	General Purpose I/O	E5	I/O	X2VDD	—
ANT2_DIO005/ USB_D05/ **GPIO30**	General Purpose I/O	G5	I/O	X2VDD	—
ANT2_DIO006/ USB_D06/ **GPIO31**	General Purpose I/O	F1	I/O	X2VDD	—
ANT2_DIO007/ USB_D07/ **GPIO32**	General Purpose I/O	G3	I/O	X2VDD	—
ANT2_DIO008/ USB_DIR/ **GPIO33**	General Purpose I/O	F2	I/O	X2VDD	—
IFC_AD08**/ GPIO34**	General Purpose I/O	E28	I/O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_AD09/ **GPIO35**	General Purpose I/O	F27	I/O	BVDD	—
IFC_AD10/ **GPIO36**	General Purpose I/O	F28	I/O	BVDD	—
IFC_AD11/ **GPIO37/** IRQ08	General Purpose I/O	G25	I/O	BVDD	—
IFC_AD12/ **GPIO38/** IRQ09	General Purpose I/O	G26	I/O	BVDD	—
IFC_AD13/ **GPIO39/** IRQ07	General Purpose I/O	G27	I/O	BVDD	—
IFC_AD14/ **GPIO40/** IRQ06	General Purpose I/O	G28	I/O	BVDD	—
IFC_AD15/ **GPIO41/** TIMER02	General Purpose I/O	H28	I/O	BVDD	—
UART_CTS_B00/ SIM_PD/ TIMER04/ **GPIO42**/ IRQ04	General Purpose I/O	AB27	I/O	OVDD	—
UART_CTS_B01/ SYS_DMA_REQ/ SRESET_B/ **GPIO44**/ IRQ05	General Purpose I/O	W22	I/O	OVDD	—
IIC1_SDA/ **GPIO46**	General Purpose I/O	V25	I/O	OVDD	—
IIC1_SCL/ **GPIO47**	General Purpose I/O	V24	I/O	OVDD	—
SDHC_CMD/ SIM_RST_B/ **GPIO48**	General Purpose I/O	C26	I/O	BVDD	—
SDHC_DATA00/ SIM_TRXD/ **GPIO49**	General Purpose I/O	D25	I/O	BVDD	—
SDHC_DATA01/ SIM_SVEN/ **GPIO50**	General Purpose I/O	F23	I/O	BVDD	—
SDHC_DATA02/ SIM_PD/ **GPIO51**	General Purpose I/O	F24	I/O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_ADDR18/ **GPO10**	General Purpose Output	H24	O	BVDD	—
IFC_ADDR19/ **GPO11**	General Purpose Output	H22	O	BVDD	—
IFC_ADDR20/ **GPO12**	General Purpose Output	H21	O	BVDD	—
IFC_ADDR21/ **GPO13**	General Purpose Output	J28	O	BVDD	—
IFC_ADDR22/ **GPO14**	General Purpose Output	J27	O	BVDD	—
IFC_ADDR23/ **GPO15**	General Purpose Output	J25	O	BVDD	—
IFC_ADDR24/ **GPO16**	General Purpose Output	J24	O	BVDD	—
IFC_ADDR25/ **GPO17**	General Purpose Output	J23	O	BVDD	—
IFC_ADDR26/ **GPO18**	General Purpose Output	J22	O	BVDD	—
ANT1_TXNRX/ TSEC_1588_PULSE_OUT2/ **GPO19**	General Purpose Output	P3	O	X1VDD	—
ANT1_TX_FRAME/ **GPO20**	General Purpose Output	R4	O	X1VDD	—
UART_RTS_B00/ PPS_LED/ **GPO43**	General Purpose Output	AB26	O	OVDD	—
UART_RTS_B01/ SYS_DMA_DONE/ **GPO45**/ ANT4_AGC	General Purpose Output	Y27	O	OVDD	—
IFC_CLE/ **GPO48**	General Purpose Output	L25	O	BVDD	—
IFC_OE_B/ **GPO49**	General Purpose Output	K23	O	BVDD	—
IFC_RB_B/ **GPO50**	General Purpose Output	K25	O	BVDD	—
IFC_WE_B/ **GPO52**	General Purpose Output	L26	O	BVDD	—
IFC_AVD/ **GPO54**	General Purpose Output	L28	O	BVDD	—
IFC_CS_B00/ **GPO55**	General Purpose Output	K21	O	BVDD	—
UART_SOUT01/ **GPO56**	General Purpose Output	W23	O	OVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VDDC	Core/Platform Supply	Y10	—	VDDC	—
VDDC	Core/Platform Supply	Y14	—	VDDC	—
VDDC	Core/Platform Supply	J16	—	VDDC	—
VDDC	Core/Platform Supply	J18	—	VDDC	—
VDDC	Core/Platform Supply	K16	—	VDDC	—
VDDC	Core/Platform Supply	K18	—	VDDC	—
VDDC	Core/Platform Supply	L16	—	VDDC	—
VDDC	Core/Platform Supply	L18	—	VDDC	—
VDDC	Core/Platform Supply	M16	—	VDDC	—
VDDC	Core/Platform Supply	M18	—	VDDC	—
VDDC	Core/Platform Supply	N16	—	VDDC	—
VDDC	Core/Platform Supply	N18	—	VDDC	—
VDDC	Core/Platform Supply	P16	—	VDDC	—
VDDC	Core/Platform Supply	P18	—	VDDC	—
VDDC	Core/Platform Supply	R16	—	VDDC	—
VDDC	Core/Platform Supply	R18	—	VDDC	—
VDDC	Core/Platform Supply	T16	—	VDDC	—
VDDC	Core/Platform Supply	T18	—	VDDC	—
VDDC	Core/Platform Supply	U16	—	VDDC	—
VDDC	Core/Platform Supply	U18	—	VDDC	—
VDDC	Core/Platform Supply	V16	—	VDDC	—
VDDC	Core/Platform Supply	V18	—	VDDC	—
VDDC	Core/Platform Supply	W16	—	VDDC	—
VDDC	Core/Platform Supply	W18	—	VDDC	—
VDDC	Core/Platform Supply	Y18	—	VDDC	—
VDD	MAPLE Supply	J10	—	VDD	—
VDD	MAPLE Supply	J12	—	VDD	—
VDD	MAPLE Supply	K10	—	VDD	—
VDD	MAPLE Supply	K12	—	VDD	—
VDD	MAPLE Supply	L10	—	VDD	—
VDD	MAPLE Supply	L12	—	VDD	—
VDD	MAPLE Supply	M10	—	VDD	—
VDD	MAPLE Supply	M12	—	VDD	—
VDD	MAPLE Supply	N10	—	VDD	—
VDD	MAPLE Supply	N12	—	VDD	—
G1VDD	DDR Supply	B13	—	G1VDD	—

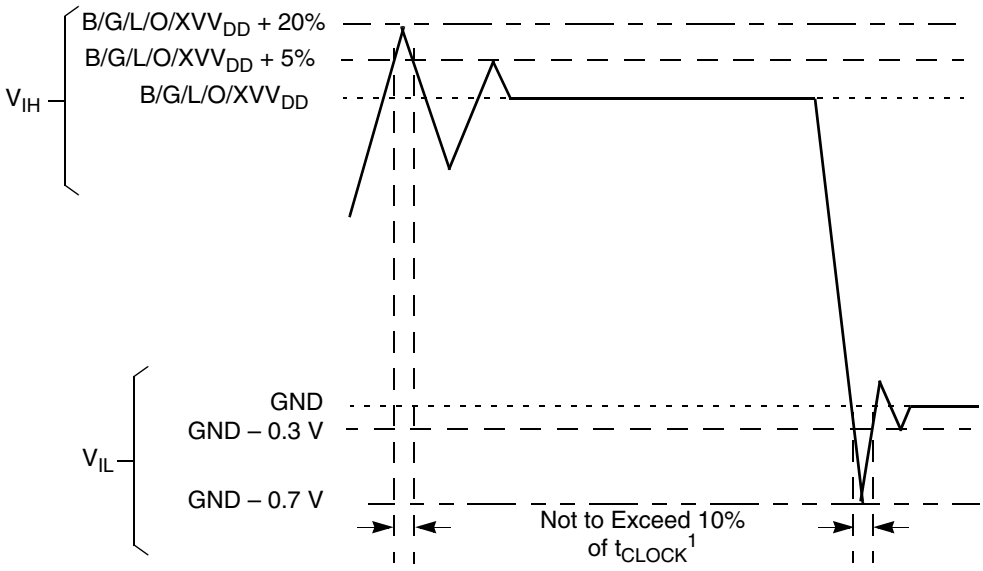
Table 3. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Note

Note:

1. **Caution:** POV_{DD1} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD1} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Sequencing."
2. USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.
3. Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.

This figure shows the undershoot and overshoot voltages at the interfaces.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references TSEC*n*_GTX_CLK125.
   For IFC, t_{CLOCK} references IFC_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/X1V_{DD}/X2V_{DD}$

The core voltage must always be provided at nominal 1 V (see Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR3 SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.7.5 RF Parallel Interface Clock Specifications

The following table lists the RF parallel interface clock DC electrical characteristics.

Table 16. RF Parallel Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	C	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following table lists the RF parallel interface clock AC electrical characteristics.

Table 17. RF Parallel Reference Clock AC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
ANT*n*_REF_CLK frequency	$f_{ANT\_REF\_CLK}$	—	19.2	—	MHz	—
ANT*n*_REF_CLK cycle time	$t_{ANT\_REF\_CLK}$	—	52	—	ns	—
ANT*n*_REF_CLK duty cycle	$t_{KHK}/t_{ANT\_REF\_CLK}$	48	50	52	%	—
ANT*n*_REF_CLK slew rate	—	1	—	4	V/ns	1
ANT*n*_REF_CLK peak period jitter	—	—	—	±100	ps	—
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:
1. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.

2.7.6 Other Input Clocks

A description of the overall clocking of this device is available in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and IFC, see the specific interface section.

2.8 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V and 1.35 V when interfacing to DDR3 or DDR3L SDRAM, respectively.

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCS[n]_B output setup with respect to MCK	t_{DDKHCS}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCS[n]_B output hold with respect to MCK	t_{DDKHCX}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
≥ 1066 MHz data rate		–0.245	0.245		
800 MHz data rate		–0.375	0.375		
667 MHz data rate		–0.6	0.6		

Table 48. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Figure 3.
2. Open drain mode for MMC cards only.

2.14.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 25.

Table 49. eSDHC AC Timing Specifications

At recommended operating conditions with BV_{DD} = 3.3 or 1.8 V

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SFSCK}	 0 0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SFSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SFSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx	$t_{SFSIVKH}$	2.5	—	ns	3, 4
Input hold times: SD_CMD, SD_DATx	$t_{SFSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SFSKHOV}$	—	3	ns	4
Output delay time: SD_CLK to SD_CMD, SD_DATx hold time	$t_{SFSKHOX}$	–3	—	ns	4

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1.5 ns.
4. CCARD ≤10 pF, (1 card), and CL = CBUS + CHOST + CCARD ≤ 40 pF

Table 55. JTAG AC Timing Specifications (continued)

For recommended operating conditions see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

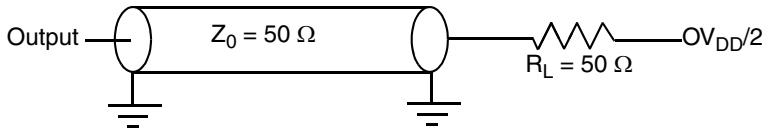


Figure 26. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

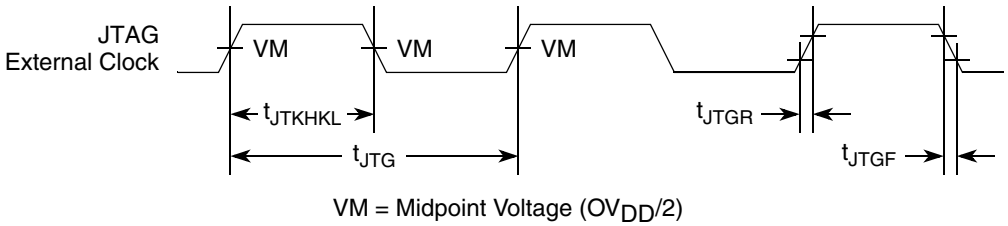


Figure 27. JTAG Clock Input Timing Diagram

This figure provides the TRST_B timing diagram.

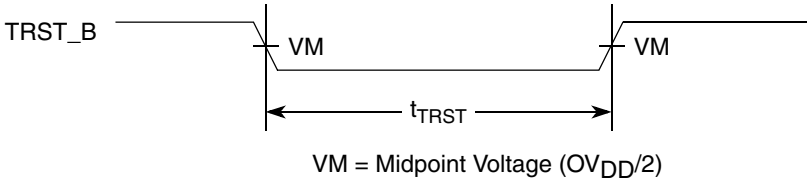


Figure 28. TRST_B Timing Diagram

This figure shows the TDM transmit signal timing.

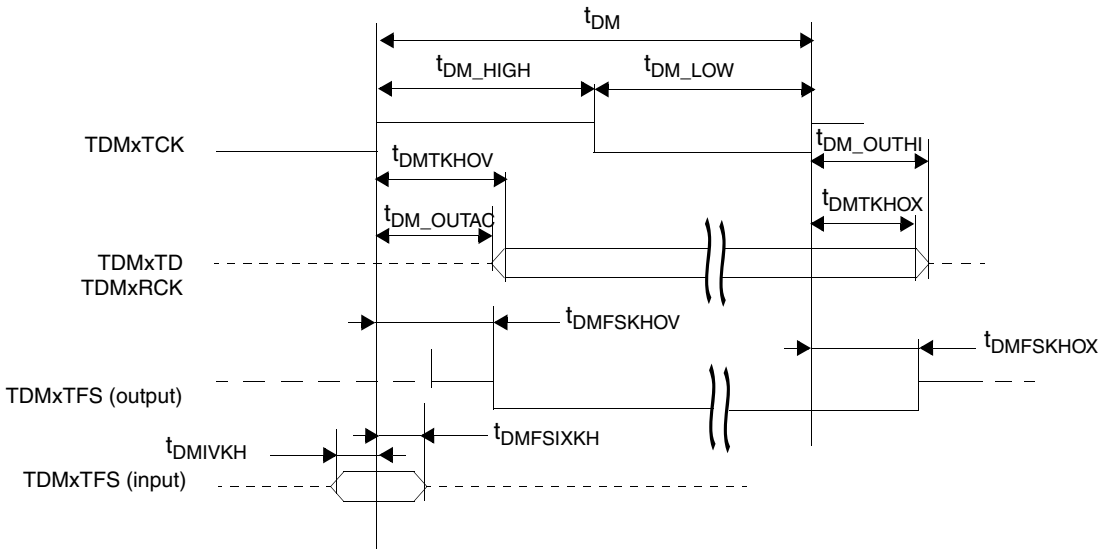


Figure 34. TDM Transmit Signals

This figure provides the AC test load for the TDM.

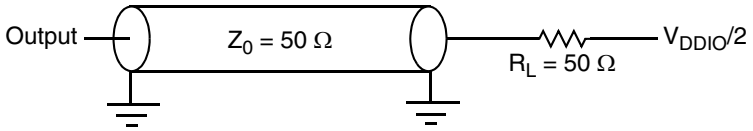


Figure 35. TDM AC Test Load

2.20 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The device features an HSSI that includes one 4-channel SerDes port (lanes 0 through 3) used for high-speed serial interface applications (PCI Express, CPRI, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the reset configuration word. Specific AC electrical characteristics are defined in Section 2.20.3, “HSSI AC Timing Specifications.”

Table 1. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Note

Note:

1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D-}|$. Measured at the package pins of the receiver.

2.20.2.3 DC-Level Requirements for CPRI Configurations

This section provide various DC-level requirements for CPRI Configurations. Specifications are valid at the recommended operating conditions listed in Table 3.

Table 70. CPRI Transmitter DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Output voltage	V_O	–0.40	—	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair.
Differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	L[0:3]TECR0[AMP_RED] = 0b000000.
Differential resistance	T_Rd	80	100	120	Ω	—

Note: LV is XAUI-based.

Table 71. CPRI Transmitter DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	L[0:3]TECR0[AMP_RED] = 0x000000
Differential resistance	T_Rd	80	100	120	Ω	—

Note: LV-II is CEI-6G-LR-based.

Table 72. CPRI Receiver DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Differential input voltage	V_{IN}	200	—	1600	mVp-p	Measured at receiver.
Difference resistance	R_Rdin	80	—	120	Ω	—

Note: LV is XAUI-based.

NOTE

The intended application is a point-to-point interface up to two connectors. The maximum allowed total loss (channel + interconnects + other loss) is 20.4 dB @ 6.144 Gbps.

2.20.3.5 SGMII AC Timing Specifications

Table 85 provides the SGMII transmit AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 85. SGMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Unit interval	UI	800 – 100ppm	800	800 + 100ppm	pS	± 100ppm
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	—
AC coupling capacitor	CTX	75	—	200	nF	All transmitters must be AC-coupled
Note: The AC specifications do not include REF_CLK jitter.						

Table 86 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 86. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Unit interval	UI	800 – 100ppm	800	800 + 100ppm	pS	± 100ppm
Deterministic jitter tolerance	JD	—	—	0.37	UI p-p	Measured at receiver.
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p-p	Measured at receiver
Total jitter tolerance	JT	—	—	0.65	UI p-p	Measured at receiver
Bit error ratio	BER	—	—	10^{-12}	—	—

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region shown in Figure 44 or Figure 45.

2.21.1.2 RF Parallel Interface AC Electrical Characteristics (eSPI2)

2.21.1.2.1 RF Parallel AC Data Interface

Table 89 provides the timing specifications for the RF parallel interface.

Table 89. RF Parallel Interface Timing Specification (3.3 V, 1.8 V)[1,2]

Parameter	Symbol	Min	Max	Unit	Note
Data_clk (MCLK) clock period	t_{PDCP}	16.276 (61.44)	—	ns (MHz)	—
Data_clk (MCLK) and fb_clk (FCLK) pulse width	t_{PDMP}	45% of t_{PDCP}	—	—	—
Delay between MCLK and FCLK at the external RFIC including trace delay	t_{PDCD}	—	7.32	ns	—
MCLK input to FCLK output delay at the BSC9132 BBIC	t_{PDMFD}	—	6.32	ns	—
Control/Data output valid time wrt FCLK during Tx from the BSC9132 BBIC	t_{PDOV}	—	6.0	ns	—
Control/Data hold from FCLK during Tx from the BSC9132 BBIC	t_{PDOX}	1.37	—	ns	3
Control/Data setup wrt MCLK	t_{PDIV}	2.5	—	ns	—
Control/Data hold wrt MCLK	t_{PDIX}	0.4	—	ns	—

Note:

1 The max trace delay of MCLK from the external RFIC to the BSC9132 BBIC and FCK/TXNRX/ENABLE from BBIC to RFIC = 1 ns each.

2 The max allowable trace skew between MCLK/FCLK and the respective data/control is 70 ps.

3 1.37 ns includes 70 ps trace skew.

This figure shows the AC test load for the timers.

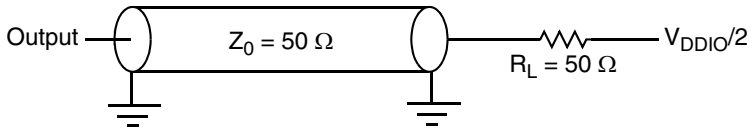


Figure 54. Timer AC Test Load

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 Power Architecture System Clocking

This section describes the PLL configuration for the Power Architecture side of the device. Note that the platform clock is identical to the internal core complex bus (CCB) clock.

This device includes 6 PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock from the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 3.1.3, "e500 Core to Platform Clock PLL Ratios." This device has two e500 core PLLs.
- The DDR PLL generates the clocking for the DDR SDRAM controller. The frequency ratio between DDR clock and platform clock is selected using the DDR PLL ratio configuration bits as described in section Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio."
- The SerDes block has two PLLs.

3.1.1 Power Architecture Clock Ranges

Table 97 provides the clocking specifications for the processor core and platform.

Table 97. Power Architecture Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Note
	Min	Max		
e500 core processor frequency	400	1200	MHz	1, 2, 3
Platform CCB bus clock frequency	267	600	MHz	1, 4, 5

- Binary value on IFC_AD[0:2] at power up

These signals must be pulled to the desired values.

In asynchronous mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 99. Power Architecture Platform/SYSCLK Clock Ratios

Binary Value of IFC_AD[0:2] Signals	Platform: SYSCLK Ratio
000	4:1
001	5:1
010	6:1
All Others	Reserved

3.1.3 e500 Core to Platform Clock PLL Ratios

The clock ratio between the e500 core0 and the platform clock is determined by the binary value of IFC_AD[3:5] signals at power up. Table 100 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[6] must be pulled low if the core frequency is 1001 MHz or below.

Table 100. e500 Core0 to Platform Clock Ratios

Binary Value of IFC_AD[3:5]Signals	e500 Core0: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

The clock ratio between the e500 core1 and the platform clock is determined by the binary value of the IFC_CLE, IFC_OE_B, IFC_WP_B signals at power up. Table 101 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[12] must be pulled low if the core frequency is 1001 MHz or below.

Table 101. e500 Core1 to Platform Clock Ratios

Binary Value of IFC_CLE, IFC_OE_B, IFC_WP_B Signals	e500 Core1: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

3.2.1 DSP Clock Ranges

Table 104 provides the clocking specifications for the SC3850 processor core, MAPLE, and DSP memory.

Table 104. DSP Processor Clocking Specifications

DSP Core	Minimum Frequency	Maximum Frequency	Unit
SC3850 cores	800	1200	MHz
MAPLE eVTPE	800	800	MHz
DSP DDR Controller	800	1333	MHz

3.2.2 DSPCLKIN and SC3850 Core Frequency Options

Table 105 shows the expected frequency options for DSPCLKIN and SC3850 core frequencies.

Table 105. Options for SC3850 Core0 and Core1 Clocking

PLL_T2 MF	DSPCLKIN Frequency (MHz)			
	66.66	80	100	133
	SC3850 Core Frequency (MHz)			
1	66.66	80	100	133
6	400	480	600	800
7.5	500	600	750	1000
8	533	640	800	1066
9	600	720	900	1200
10	667	800	1000	—
12	800	960	1200	—
15	1000	1200	—	—

3.3 Supply Power Default Setting

This device is capable of supporting multiple power supply levels on its I/O supply. Table 106 through Table 110 shows the encoding used to select the voltage level for each I/O supply. When setting the VSEL signals, "1" is selected through a pull-up resistor to OVDD (as seen in Table 1).

Table 106. Default Voltage Level for BV_{DD}

BVDD_VSEL[0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 V
11	Reserved

Table 107. Default Voltage Level for CV_{DD}

CVDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 108. Default Voltage Level for $X1V_{DD}$

X1VDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 109. Default Voltage Level for $X2V_{DD}$

XVDD2_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 110. Default Voltage Level for LV_{DD}

LVDD_VSEL	I/O Voltage Level
0	3.3 V
1	2.5 V

3.4 PLL Power Supply Design

Each of the PLLs listed above is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE0, AVDD_CORE1, AVDD_D1_DDR, AVDD_D2_DDR, AVDD_DSP, and AVDD_MAPLE respectively). The AV_{DD} level should always be equivalent to V_{DDC}, and these voltages must be derived directly from V_{DDC} through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 55, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 780 ball FCPBGA the footprint, without the inductance of vias.

- *e500 PowerPC Core Reference Manual* (E500CORERM)

7 Revision History

Table 115. Document Revision History

Rev	Date	Substantive Change(s)
1	08/2014	Updated Table 1, “BSC9132 Pinout Listing.”
0	03/2014	Initial public release.