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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SC3850, Security; SEC 4.4
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=bsc9132nse7mnmb

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1.1 Ball Layout Diagrams

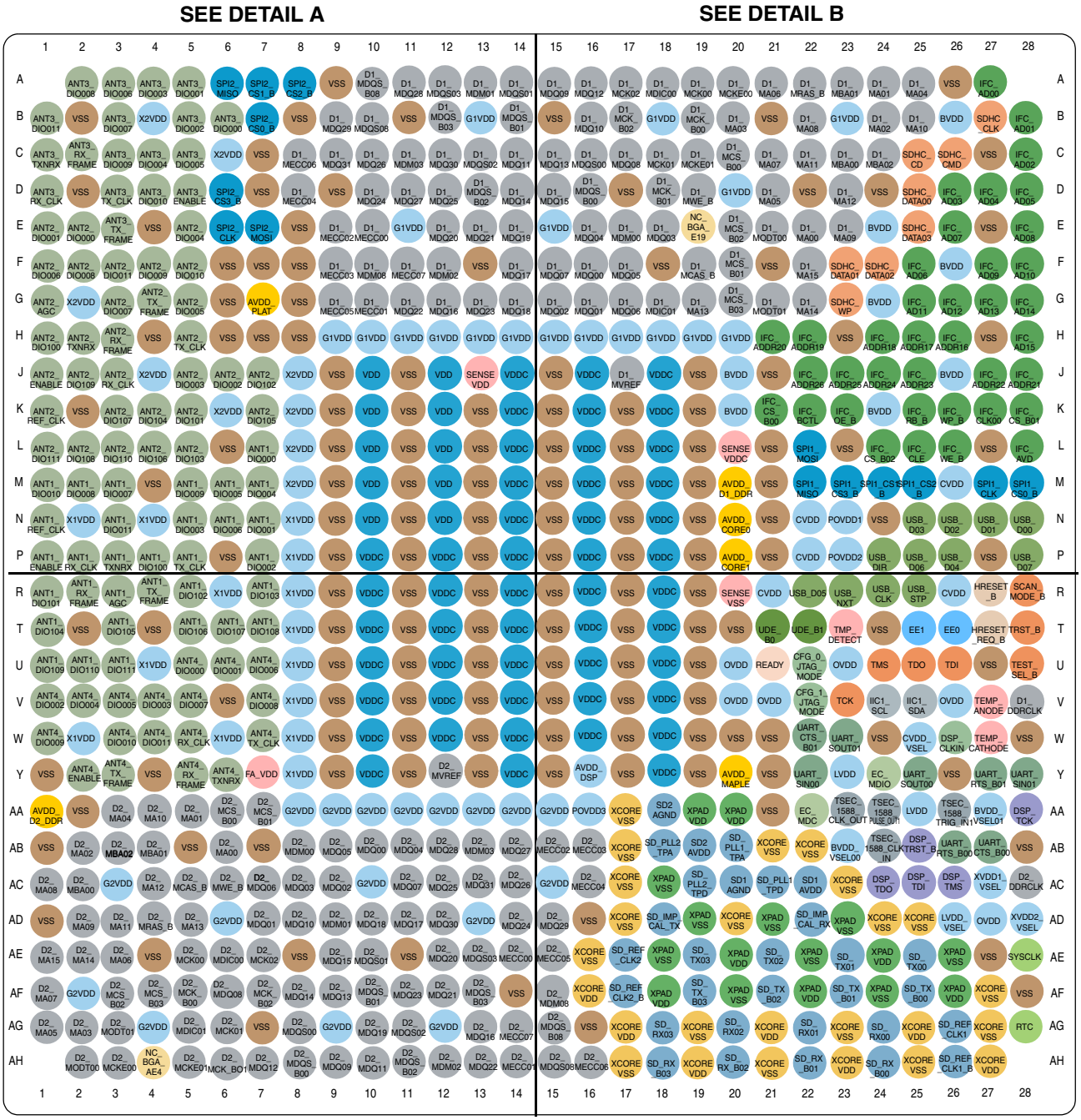

Figure 2. Ball Layout Diagram—Top-Level View

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO104/ **TDM1_RCK**/ GPIO92	TDM1 Receive Clock	K4	I/O	X2VDD	—
ANT2_DIO105/ **TDM1_RFS**/ TIMER08	TDM1 Receive Frame Sync	K7	I/O	X2VDD	—
ANT2_DIO102/ **TDM1_RXD**	TDM1 Receive Data	J7	I/O	X2VDD	—
TDM2 over RF3					
ANT3_RX_CLK/ **TDM2_TCK**/ GPIO04	TDM2 Clock	D1	I/O	X2VDD	—
ANT3_DIO007/ **TDM2_TFS**	TDM2 Transmit Frame Sync	B3	I/O	X2VDD	—
ANT3_DIO011/ **TDM2_TXD**	TDM2 Transmit Data	B1	I/O	X2VDD	—
ANT3_DIO008/ **TDM2_RCK**/ CKSTP0_OUT_B	TDM2 Receive Clock	A2	I/O	X2VDD	—
ANT3_DIO009/ **TDM2_RFS**/ CKSTP1_OUT_B	TDM2 Receive Frame Sync	C3	I/O	X2VDD	—
ANT3_DIO010/ **TDM2_RXD**	TDM2 Receive Data	D4	I/O	X2VDD	—
SerDes					
SD_TX03	Tx Data out	AE19	O	XPADVDD	—
SD_TX02	Tx Data out	AE21	O	XPADVDD	—
SD_TX01	Tx Data out	AE23	O	XPADVDD	—
SD_TX00	Tx Data out	AE25	O	XPADVDD	—
SD_TX_B03	Tx Data out, inverted	AF19	O	XPADVDD	—
SD_TX_B02	Tx Data out, inverted	AF21	O	XPADVDD	—
SD_TX_B01	Tx Data out, inverted	AF23	O	XPADVDD	—
SD_TX_B00	Tx Data out, inverted	AF25	O	XPADVDD	—
SD_RX03	Rx Data in	AG18	I	XCOREVDD	—
SD_RX02	Rx Data in	AG20	I	XCOREVDD	—
SD_RX01	Rx Data in	AG22	I	XCOREVDD	—
SD_RX00	Rx Data in	AG24	I	XCOREVDD	—
SD_RX_B03	Rx Data in, Inverted	AH18	I	XCOREVDD	—
SD_RX_B02	Rx Data in, Inverted	AH20	I	XCOREVDD	—
SD_RX_B01	Rx Data in, Inverted	AH22	I	XCOREVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_ADDR18/ **GPO10**	General Purpose Output	H24	O	BVDD	—
IFC_ADDR19/ **GPO11**	General Purpose Output	H22	O	BVDD	—
IFC_ADDR20/ **GPO12**	General Purpose Output	H21	O	BVDD	—
IFC_ADDR21/ **GPO13**	General Purpose Output	J28	O	BVDD	—
IFC_ADDR22/ **GPO14**	General Purpose Output	J27	O	BVDD	—
IFC_ADDR23/ **GPO15**	General Purpose Output	J25	O	BVDD	—
IFC_ADDR24/ **GPO16**	General Purpose Output	J24	O	BVDD	—
IFC_ADDR25/ **GPO17**	General Purpose Output	J23	O	BVDD	—
IFC_ADDR26/ **GPO18**	General Purpose Output	J22	O	BVDD	—
ANT1_TXNRX/ TSEC_1588_PULSE_OUT2/ **GPO19**	General Purpose Output	P3	O	X1VDD	—
ANT1_TX_FRAME/ **GPO20**	General Purpose Output	R4	O	X1VDD	—
UART_RTS_B00/ PPS_LED/ **GPO43**	General Purpose Output	AB26	O	OVDD	—
UART_RTS_B01/ SYS_DMA_DONE/ **GPO45**/ ANT4_AGC	General Purpose Output	Y27	O	OVDD	—
IFC_CLE/ **GPO48**	General Purpose Output	L25	O	BVDD	—
IFC_OE_B/ **GPO49**	General Purpose Output	K23	O	BVDD	—
IFC_RB_B/ **GPO50**	General Purpose Output	K25	O	BVDD	—
IFC_WE_B/ **GPO52**	General Purpose Output	L26	O	BVDD	—
IFC_AVD/ **GPO54**	General Purpose Output	L28	O	BVDD	—
IFC_CS_B00/ **GPO55**	General Purpose Output	K21	O	BVDD	—
UART_SOUT01/ **GPO56**	General Purpose Output	W23	O	OVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
BVDD	IFC, eSDHC, USIM Supply	B26	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	E24	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	F26	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	G24	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	J20	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	J26	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	K20	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	K24	—	BVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	N22	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	P22	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	M26	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	R21	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	R26	—	CVDD	—
OVDD	DUART, System, I2C, JTAG Supply	U20	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	V20	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	V21	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	V26	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	U23	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	AD27	—	OVDD	—
X1VDD	RF Supply	N2	—	X1VDD	—
X1VDD	RF Supply	N4	—	X1VDD	—
X1VDD	RF Supply	N8	—	X1VDD	—
X1VDD	RF Supply	U4	—	X1VDD	—
X1VDD	RF Supply	W2	—	X1VDD	—
X1VDD	RF Supply	W6	—	X1VDD	—
X1VDD	RF Supply	P8	—	X1VDD	—
X1VDD	RF Supply	R6	—	X1VDD	—
X1VDD	RF Supply	R8	—	X1VDD	—
X1VDD	RF Supply	T8	—	X1VDD	—
X1VDD	RF Supply	U8	—	X1VDD	—
X1VDD	RF Supply	V8	—	X1VDD	—
X1VDD	RF Supply	W8	—	X1VDD	—
X1VDD	RF Supply	Y8	—	X1VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	B4	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	C6	—	X2VDD	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR3/DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	5, 10
	DDR3/DDR3L DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	10
	Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	6, 10
	IFC, eSDHC, USIM signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	7, 10
	DUART1, SYSCLK, system control and power management, I^2C1, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	8, 10
	USB, eSPI1, DUART2, I^2C2, USIM	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 10
	RF parallel interface	$X1V_{IN}$	–0.3 to ($X1V_{DD}$ + 0.3)	V	9, 10
	eSPI2, USB, TDM1, TDM2, RF parallel interface	$X2V_{IN}$	–0.3 to ($X2V_{DD}$ + 0.3)	V	9, 10
Storage temperature range		T_{STG}	–55 to 150	°C	—

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. AV_{DD} is measured at the input to the filter and not at the pin of the device.
3. USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.
4. Caution: CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Caution: LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. Caution: $X[1\text{-}2]V_{IN}$ must not exceed $X[1\text{-}2]V_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. $(C,X,B,G,L,O,R)V_{DD}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Platform supply voltage	V_{DDC}	1 + 50 mV / – 30mV	V	1
MAPLE-B2P supply voltage	V_{DD}	1 + 50 mV / – 30mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
PLL supply voltage		$AV_{DD\_CORE[0–1]}$ $AV_{DD\_D[1–2]\_DDR}$ AV_{DD_PLAT} AV_{DD_DSP} AV_{DD_MAPLE} $SD[1–2]AV_{DD}$	1 + 50 mV / – 30mV	V	1
Fuse supply voltage		POV_{DD1}	1.5 V ± 75 mV	V	1
DDR3 DRAM I/O voltage		$G[1–2]V_{DD}$	1.5 V ± 75 mV	—	—
DDR3L DRAM I/O voltage		$G[1–2]V_{DD}$	1.35 V +100mV/ –67mV	—	—
Three-speed Ethernet, Ethernet management (eTSEC) and 1588		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
DUART1, SYSCLK, system control and power management, I^2C1, clocking, I/O voltage select, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
IFC, eSDHC, USIM		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	2
USB, eSPI1, DUART2, I^2C2, USIM		CV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	2
RF parallel interface		$X1V_{DD}$	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
eSPI2, USB, TDM1, TDM2, RF parallel interface		$X2V_{DD}$	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
SerDes pad voltage		$XPADV_{DD}$	1.5 V ± 75 mV	V	—
SerDes core voltage		$XCOREV_{DD}$	1.0 V ± 50 mV	V	—
Input voltage	DDR3/DDR3L DRAM	MV_{IN}	GND to GV_{DD}	V	—
	DDR3/DDR3L DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Ethernet, USB	LV_{IN}	GND to LV_{DD}	V	—
	IFC, eSDHC signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART1, SYSCLK, system control and power management, eSPI, I^2C1, USIM, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	—
	USB, eSPI, eSDHC, DUART2, I^2C2, USIM	CV_{IN}	GND to CV_{DD}	V	—
	RF parallel interface	$X1V_{IN}$	GND to $X1V_{DD}$	V	—
	eSPI2, USB, TDM1, TDM2, RF parallel interface	$X2V_{IN}$	GND to $X2V_{DD}$	V	—
Maximum input capacitance		C_{INMAX}	10	pF	3
Operating Temperature range	Standard	T_A/T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended	T_A/T_J	T_A = –40 (min) to T_J = 105 (max)	°C	—
	Secure boot fuse programming	T_A/T_J	T_A = 0 (min) to T_J = 70 (max)	°C	1

Table 24. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	2
1333 MHz data rate		–250	250		
1200 MHz data rate		–275	275		
1066 MHz data rate		–300	300		
800 MHz data rate		–425	425		
667 MHz data rate		–510	510		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

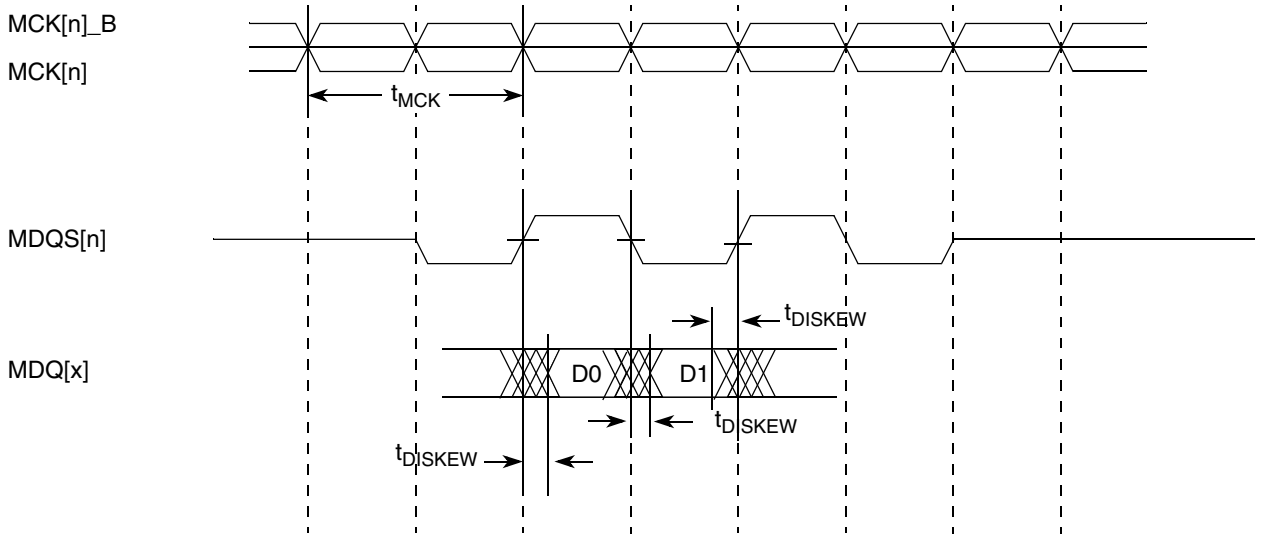

Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

2.8.2.2 DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR3 and DDR3L SDRAM interface.

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	1.5	3	ns	2

Table 35. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	10	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.11.2.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

This figure shows the MII management interface timing diagram.

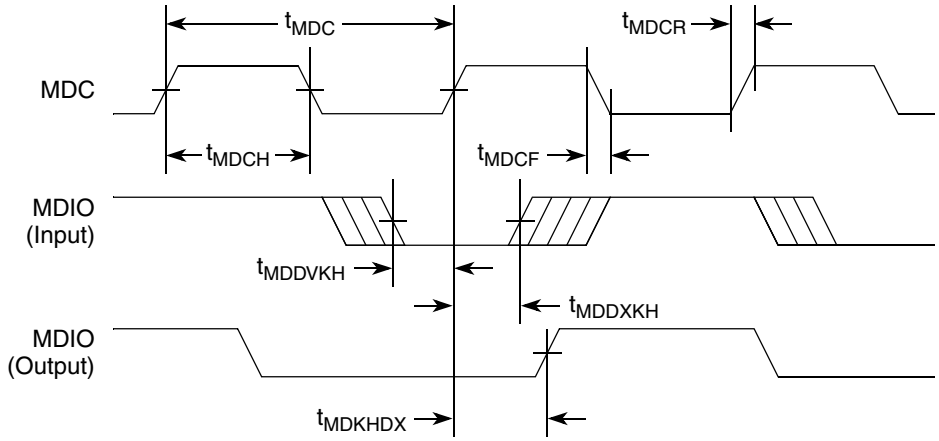

Figure 16. MII Management Interface Timing Diagram

2.11.3 eTSEC IEEE Std 1588 Electrical Specifications

2.11.3.1 eTSEC IEEE Std 1588 DC Specifications

This table shows IEEE Std 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 37. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

This table shows the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 38. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.13 Integrated Flash Controller (IFC)

This section describes the DC and AC electrical specifications for the integrated flash controller.

2.13.1 IFC DC Electrical Characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 3.3 V.

Table 44. Integrated Flash Controller DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 2.5 V.

Table 45. Integrated Flash Controller DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—

This figure shows the AC timing diagram.

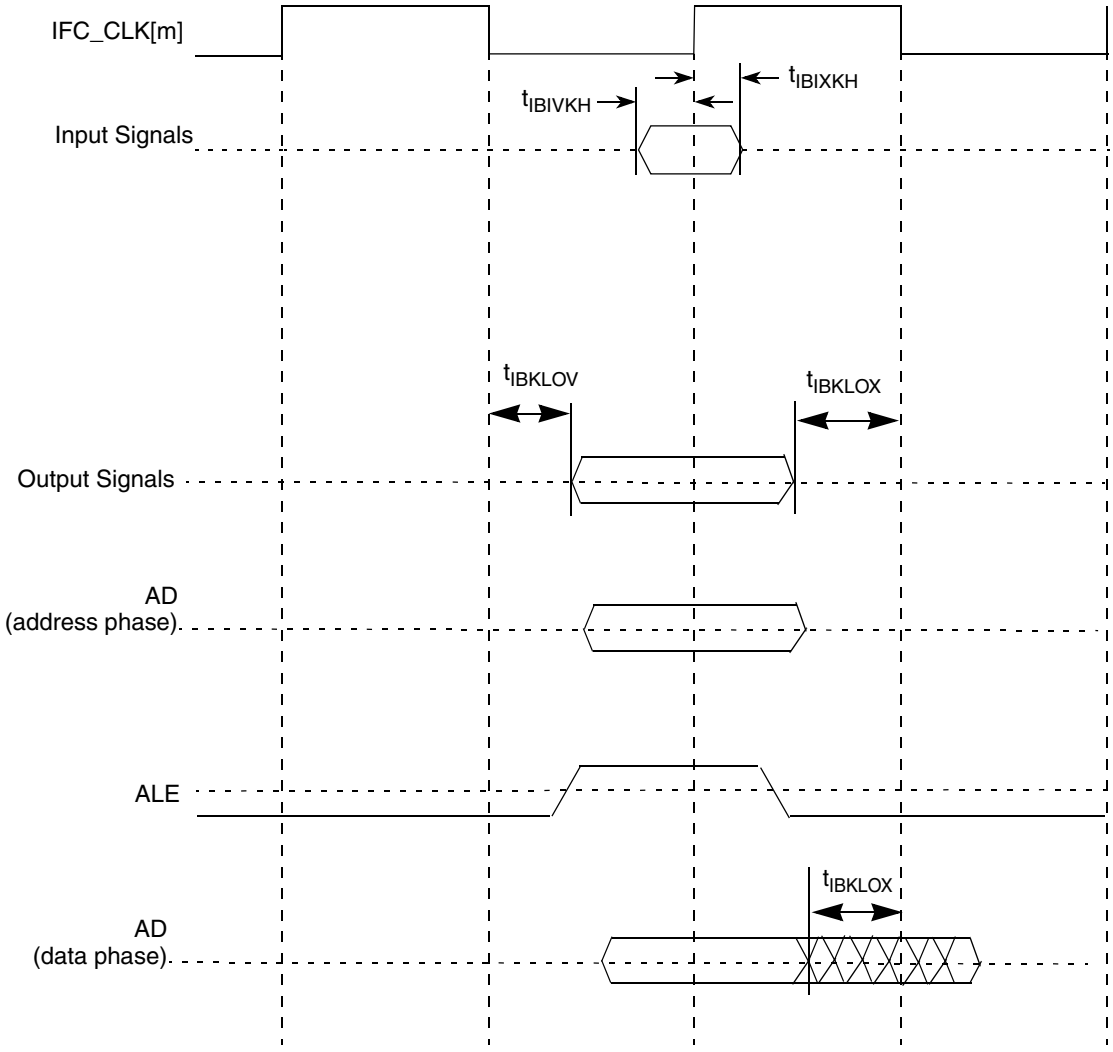

Figure 22. Integrated Flash Controller Signals

Figure 22 applies to all the controllers that IFC supports.

For input signals, the AC timing data is used directly for all controllers. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows the TDM transmit signal timing.

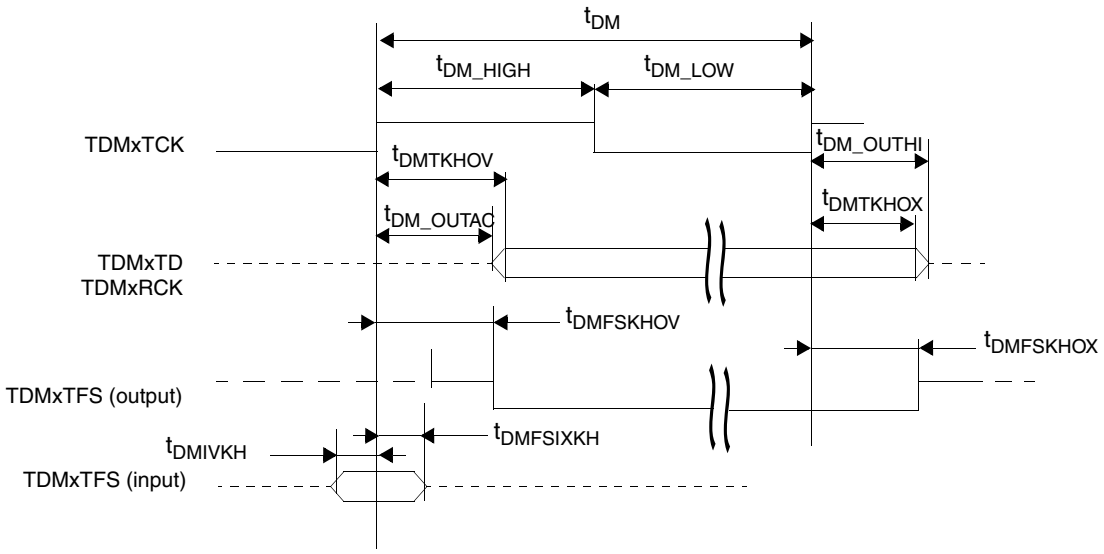

Figure 34. TDM Transmit Signals

This figure provides the AC test load for the TDM.

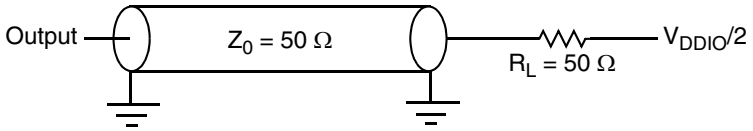

Figure 35. TDM AC Test Load

2.20 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The device features an HSSI that includes one 4-channel SerDes port (lanes 0 through 3) used for high-speed serial interface applications (PCI Express, CPRI, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the reset configuration word. Specific AC electrical characteristics are defined in Section 2.20.3, “HSSI AC Timing Specifications.”

Table 68. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Note

Note:

1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$. Measured at the package pins of the receiver.

Table 69. PCI Express (5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Differential peak-to-peak output voltage swing	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \|V_{TX\text{-}D+} - V_{TX\text{-}D\text{-}}\|$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
Low power differential peak-to-peak output voltage swing	$V_{TX\text{-}DIFFp\text{-}p\_low}$	400	500	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \|V_{TX\text{-}D+} - V_{TX\text{-}D\text{-}}\|$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Table 1. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	5

Table 82. CPRI Transmitter AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Unit Interval: 4.9152 GBaud	UI	1/4915.2 – 100ppm	1/4915.2.8	1/4915.2 + 100ppm	µs
Unit Interval: 6.144 GBaud	UI	1/6144.0 – 100ppm	1/6144.0	1/6144.0 + 100ppm	µs

Table 83 defines the Receiver AC specifications for CPRI LV. The AC timing specifications do not include REF_CLK jitter.

Table 83. CPRI Receiver AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic jitter tolerance	JD	—	—	0.37	UI p-p
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p-p
Total Jitter tolerance	JT	—	—	0.65	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	ps
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	ps
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	ps
Bit error ratio	BER	—	—	10^{-12}	—

Table 84 defines the Receiver AC specifications for CPRI LV-II. The AC timing specifications do not include REF_CLK jitter.

Table 84. CPRI Receiver AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Gaussian	R_GJ	—	—	0.275	UI p-p
Uncorrelated bounded high probability jitter	R_UBHPJ	—	—	0.150	UI p-p
Correlated bounded high probability jitter	R_CBHPJ	—	—	0.525	UI p-p
Bounded high probability jitter	R_BHPJ	—	—	0.675	UI p-p
Sinusoidal jitter, maximum	R_SJ-max	—	—	5.000	UI p-p
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.050	UI p-p
Total Jitter (does not include sinusoidal jitter).	R_TJ	—	—	0.950	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	µs
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	µs
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	µs
Unit Interval: 4.9152 GBaud	UI	1/4915.2 – 100ppm	1/4915.2.8	1/4915.2 + 100ppm	µs
Unit Interval: 6.144 GBaud	UI	1/6144.0 – 100ppm	1/6144.0	1/6144.0 + 100ppm	µs

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 46. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace.

2.22.3 USIM External Pull Up/Pull Down Resistor Requirements

External off-chip pull up resistor of 20 KΩ is required on the SIM_TRXD pin.

External off-chip pull down resistors are required on the SIM_PD, SIM_SVEN, SIM_RST pins.

2.22.4 USIM Reset Sequence

2.22.4.1 SIM Cards With Internal Reset

The sequence of reset for this kind of SIM cards is as follows (see Figure 51):

- After power up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, Rx must be high.
- The card must send a response on Rx acknowledging the reset between 400 and 40000 clock cycles after T0.

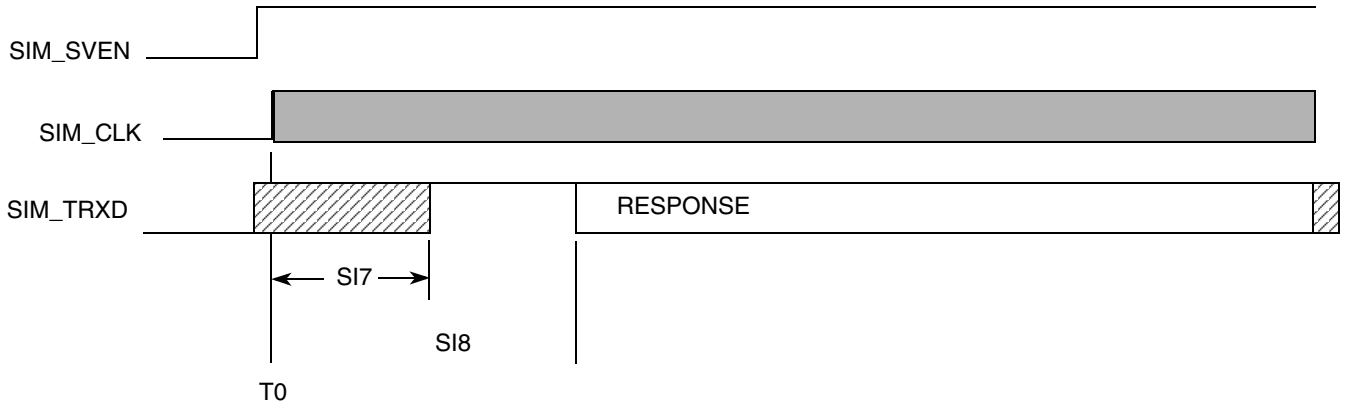

Figure 51. Internal-Reset Card Reset Sequence

Table 93. Parameters of Reset Sequence For Card With Internal Reset

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM clock to SIM TX data H	$S_{clk2dat}$	—	200	SIM_CLK clock cycle
SI8	SIM clock to SIM get ATR data	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle

2.22.4.2 SIM Cards With Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 52):

- After powering up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, SIM_TRXD must be high.
- SIM_RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on Rx during those 40000 clock cycles).
- SIM_RST is set High (time T1).
- SIM_RST must remain High for at least 40000 clock cycles after T1 and a response must be received on SIM_TRXD between 400 and 40000 clock cycles after T1.

Each of these steps is done in one CKIL period (typically 32 KHz). Power down is initiated by detection of a SIM card removal or is launched by the processor. See Figure 53 and Table 95 for the timing requirements for this sequence, with F_{CKIL} = CKIL frequency value.

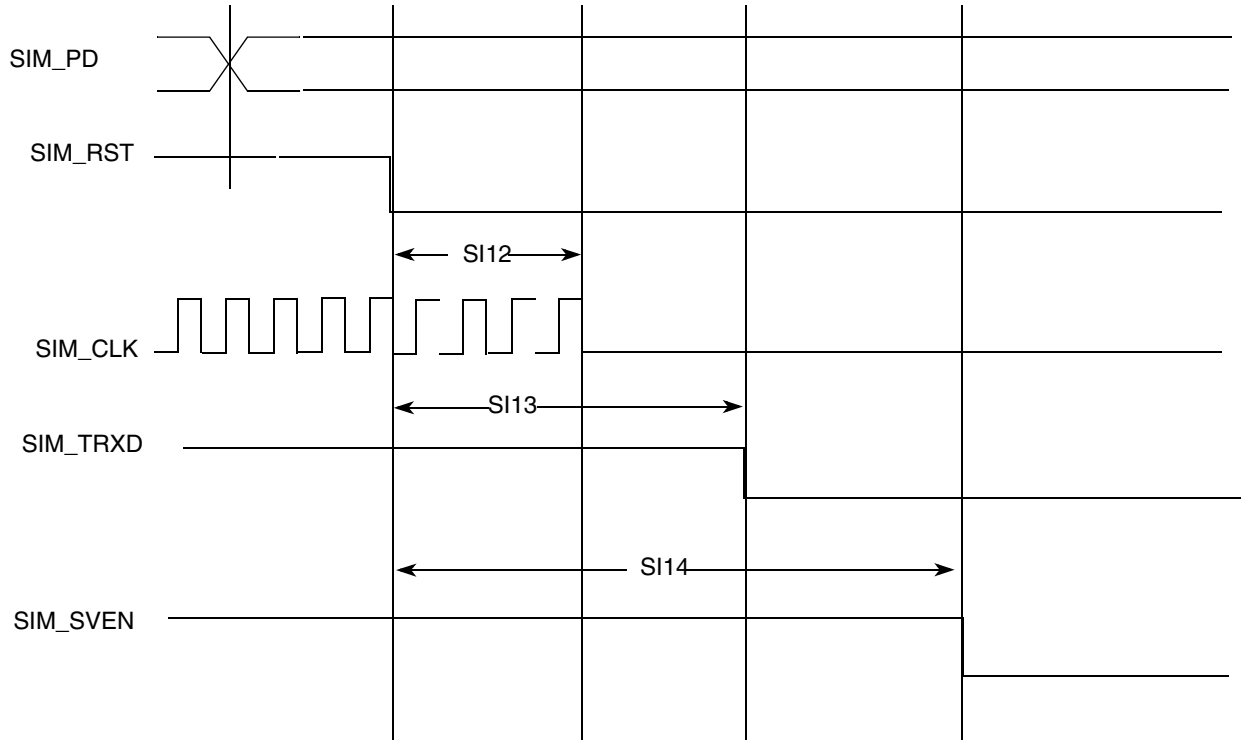

Figure 53. SmartCard Interface Power Down AC Timing

Table 95. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI12	USIM reset to USIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × $1/F_{CKIL}$	ns
SI13	USIM reset to USIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × $1/F_{CKIL}$	ns
SI14	USIM reset to USIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × $1/F_{CKIL}$	ns
SI15	USIM presence detect to USIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × $1/F_{CKIL}$	ns

2.23 Timers and Timers_32b AC Timing Specifications

This table lists the timer input AC timing specifications.

Table 96. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Minimum	Unit	Note
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Note:

1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure shows the AC test load for the timers.

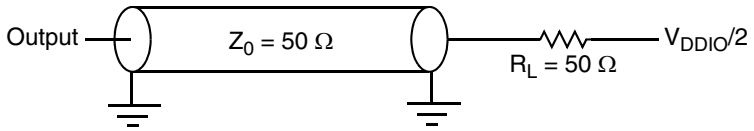

Figure 54. Timer AC Test Load

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 Power Architecture System Clocking

This section describes the PLL configuration for the Power Architecture side of the device. Note that the platform clock is identical to the internal core complex bus (CCB) clock.

This device includes 6 PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock from the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 3.1.3, "e500 Core to Platform Clock PLL Ratios." This device has two e500 core PLLs.
- The DDR PLL generates the clocking for the DDR SDRAM controller. The frequency ratio between DDR clock and platform clock is selected using the DDR PLL ratio configuration bits as described in section Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio."
- The SerDes block has two PLLs.

3.1.1 Power Architecture Clock Ranges

Table 97 provides the clocking specifications for the processor core and platform.

Table 97. Power Architecture Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Note
	Min	Max		
e500 core processor frequency	400	1200	MHz	1, 2, 3
Platform CCB bus clock frequency	267	600	MHz	1, 4, 5

- Binary value on IFC_AD[0:2] at power up

These signals must be pulled to the desired values.

In asynchronous mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 99. Power Architecture Platform/SYSCLK Clock Ratios

Binary Value of IFC_AD[0:2] Signals	Platform: SYSCLK Ratio
000	4:1
001	5:1
010	6:1
All Others	Reserved

3.1.3 e500 Core to Platform Clock PLL Ratios

The clock ratio between the e500 core0 and the platform clock is determined by the binary value of IFC_AD[3:5] signals at power up. Table 100 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[6] must be pulled low if the core frequency is 1001 MHz or below.

Table 100. e500 Core0 to Platform Clock Ratios

Binary Value of IFC_AD[3:5]Signals	e500 Core0: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

The clock ratio between the e500 core1 and the platform clock is determined by the binary value of the IFC_CLE, IFC_OE_B, IFC_WP_B signals at power up. Table 101 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[12] must be pulled low if the core frequency is 1001 MHz or below.

Table 101. e500 Core1 to Platform Clock Ratios

Binary Value of IFC_CLE, IFC_OE_B, IFC_WP_B Signals	e500 Core1: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

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