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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=bsc9132nsn7knkb

1.1 Ball Layout Diagrams

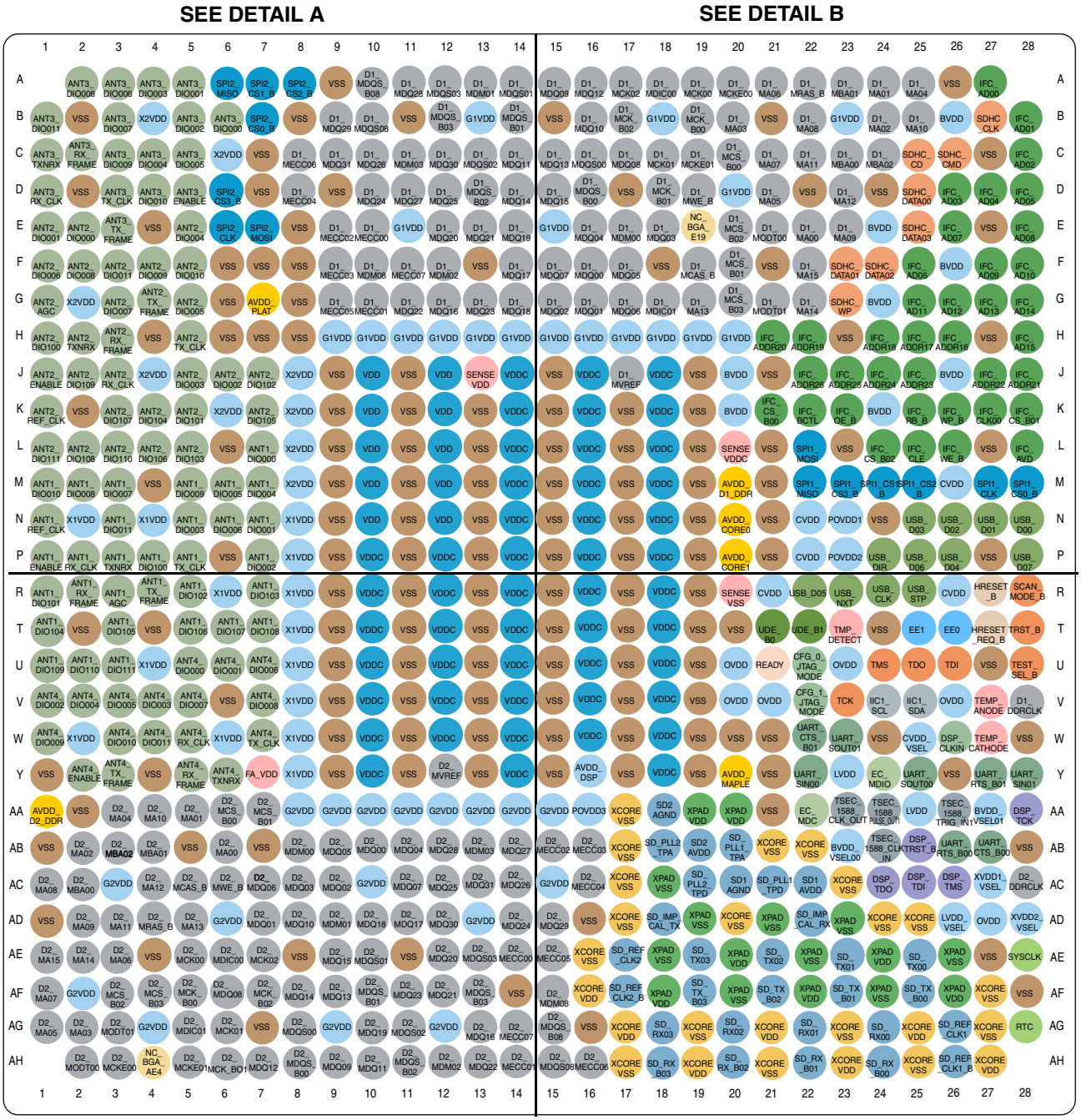


Figure 2. Ball Layout Diagram—Top-Level View

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MDQ13	Data	AF9	I/O	G2VDD	—
D2_MDQ14	Data	AF8	I/O	G2VDD	—
D2_MDQ15	Data	AE9	I/O	G2VDD	—
D2_MDQ16	Data	AG13	I/O	G2VDD	—
D2_MDQ17	Data	AD11	I/O	G2VDD	—
D2_MDQ18	Data	AD10	I/O	G2VDD	—
D2_MDQ19	Data	AG10	I/O	G2VDD	—
D2_MDQ20	Data	AE12	I/O	G2VDD	—
D2_MDQ21	Data	AF12	I/O	G2VDD	—
D2_MDQ22	Data	AH13	I/O	G2VDD	—
D2_MDQ23	Data	AF11	I/O	G2VDD	—
D2_MDQ24	Data	AD14	I/O	G2VDD	—
D2_MDQ25	Data	AC12	I/O	G2VDD	—
D2_MDQ26	Data	AC14	I/O	G2VDD	—
D2_MDQ27	Data	AB14	I/O	G2VDD	—
D2_MDQ28	Data	AB12	I/O	G2VDD	—
D2_MDQ29	Data	AD15	I/O	G2VDD	—
D2_MDQ30	Data	AD12	I/O	G2VDD	—
D2_MDQ31	Data	AC13	I/O	G2VDD	—
D2_MDM00	Data Mask	AB8	O	G2VDD	—
D2_MDM01	Data Mask	AD9	O	G2VDD	—
D2_MDM02	Data Mask	AH12	O	G2VDD	—
D2_MDM03	Data Mask	AB13	O	G2VDD	—
D2_MDQS00	Data Strobe	AG8	I/O	G2VDD	—
D2_MDQS01	Data Strobe	AE10	I/O	G2VDD	—
D2_MDQS02	Data Strobe	AG11	I/O	G2VDD	—
D2_MDQS03	Data Strobe	AE13	I/O	G2VDD	—
D2_MDQS_B00	Data Strobe	AH8	I/O	G2VDD	—
D2_MDQS_B01	Data Strobe	AF10	I/O	G2VDD	—
D2_MDQS_B02	Data Strobe	AH11	I/O	G2VDD	—
D2_MDQS_B03	Data Strobe	AF13	I/O	G2VDD	—
D2_MBA00	Bank Select	AC2	O	G2VDD	—
D2_MBA01	Bank Select	AB4	O	G2VDD	—
D2_MBA02	Bank Select	AB3	O	G2VDD	—
D2_MA00	Address	AB6	O	G2VDD	—
D2_MA01	Address	AA5	O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_CLE/ GPO48	NAND Command Latch Enable/GPCM Write Byte Select1	L25	O	BVDD	18
IFC_OE_B/ GPO49	NOR Output Enable/NAND Read Enable/ GPCM Output Enable/Generic ASIC Interface Read-Write Indicator	K23	O	BVDD	2
IFC_WP_B/ GPO66	IFC Write Protect	K26	O	BVDD	18
IFC_RB_B/ GPO50	IFC Read Busy/GPCM External Transreciver/ Generic ASIC i/f Ready Indicator	K25	I	BVDD	—
IFC_BCTL/ GPO67	Data Buffer Control	K22	O	BVDD	18
IFC_CLK00/ GPO68	IFC Clock	K27	O	BVDD	—
eSDHC					
SDHC_CLK/ SIM_CLK/ GPO52	SDHC Clock	B27	O	BVDD	—
SDHC_CMD/ SIM_RST_B/ GPIO48	SDHC Command	C26	I/O	BVDD	15
SDHC_DATA00/ SIM_TRXD/ GPIO49	SDHC Data2 in all modes	D25	I/O	BVDD	15
SDHC_DATA01/ SIM_SVEN/ GPIO50	SDHC Data1 in 4-bit mode	F23	I/O	BVDD	15
SDHC_DATA02/ SIM_PD/ GPIO51	SDHC Data2 in 4-bit mode	F24	I/O	BVDD	15
SDHC_DATA03/ DMA_DDONE_B00/ CKSTP1_IN_B/ GPIO77	SDHC Data3 in 1-bit mode SDHC Data3 in 4-bit mode	E25	I/O	BVDD	15,16
SDHC_WP/ DMA_DREQ_B00/ CKSTP0_IN_B/ GPIO78	SDHC Write Protect Detect	G23	I	BVDD	—
SDHC_CD/ DMA_DACK_B00/ MCP1_B/ GPIO79/ IRQ10	SDHC Card Detect	C25	I	BVDD	—
USIM					

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
USB_D06/ UART_CTS_B02/ GPIO62	ULPI Data	P25	I/O	CVDD	—
USB_D05/ UART_RTS_B02/ GPIO63	ULPI Data	R22	I/O	CVDD	—
USB_D04/ GPIO00/ IRQ00	ULPI Data	P26	I/O	CVDD	—
USB_D03/ GPIO01/ IRQ01	ULPI Data	N25	I/O	CVDD	—
USB_D02/ IIC2_SDA/ GPIO71	ULPI Data	N26	I/O	CVDD	—
USB_D01/ IIC2_SCL/ GPIO72	ULPI Data	N27	I/O	CVDD	—
USB_D00/ IRQ02/ GPIO53	ULPI Data	N28	I/O	CVDD	—
USB_STP/ IRQ_OUT_B/ GPO73	ULPI Stop	R25	O	CVDD	—
USB_DIR/ GPIO02/ TIMER01/ MCP0_B	ULPI Data Direction	P24	I	CVDD	—
USB_NXT/ GPIO03/ IRQ03/ TRIG_IN	ULPI Next Data Throttle Control	R23	I	CVDD	—
USB over ANT2					
ANT2_DIO009/ **USB_CLK**/ GPIO59	ULPI Clock	F4	I	X2VDD	—
ANT2_DIO007/ **USB_D07**/ GPIO32	ULPI Data	G3	I/O	X2VDD	—
ANT2_DIO006/ **USB_D06**/ GPIO31	ULPI Data	F1	I/O	X2VDD	—
ANT2_DIO005/ **USB_D05**/ GPIO30	ULPI Data	G5	I/O	X2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT3_RX_CLK/ TDM2_TCK/ GPIO04	Receive Clock	D1	I	X2VDD	—
ANT3_TXNRX	TX_RX Control	C1	O	X2VDD	—
ANT3_ENABLE	Antenna Enable	D5	O	X2VDD	—
ANT3_TX_FRAME	Transmit Frame	E3	O	X2VDD	2
ANT3_RX_FRAME/ GPIO05	Receive Frame	C2	I	X2VDD	—
ANT3_DIO000/ CP_SYNC1	Data	B6	I/O	X2VDD	—
ANT3_DIO001/ CP_SYNC2	Data	A5	I/O	X2VDD	4, 13
ANT3_DIO002/ CP_LOS1	Data	B5	I/O	X2VDD	4, 13
ANT3_DIO003/ CP_LOS2	Data	A4	I/O	X2VDD	4, 13
ANT3_DIO004/ CP_TX_INT_B	Data	C4	I/O	X2VDD	4, 13
ANT3_DIO005/ CP_RCLK	Data	C5	I/O	X2VDD	4, 13
ANT3_DIO006/ CP_RX_INT_B	Data	A3	I/O	X2VDD	4, 13
ANT3_DIO007/ TDM2_TFS	Data	B3	I/O	X2VDD	—
ANT3_DIO008/ TDM2_RCK/ CKSTP0_OUT_B	Data	A2	I/O	X2VDD	—
ANT3_DIO009/ TDM2_RFS/ CKSTP1_OUT_B	Data	C3	I/O	X2VDD	4, 13
ANT3_DIO010/ TDM2_RXD	Data	D4	I/O	X2VDD	4, 13
ANT3_DIO011/ TDM2_TXD	Data	B1	I/O	X2VDD	—
RF Interface 4					
UART_RTS_B01/ SYS_DMA_DONE/ GPO45/ **ANT4_AGC**	AGC	Y27	O	OVDD	—
ANT4_TX_CLK	Transmit Clock	W7	O	X1VDD	—
ANT4_RX_CLK/ GPIO04/ TRIG_IN	Receive Clock	W5	I	X1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI1_CS3_B/ **CKSTP1_OUT_B**/ GPO76	Checkstop Out	M23	O	CVDD	—
READY/ ASLEEP/ READY_P1	Ready/Trigger Out/Asleep	U21	O	OVDD	2
UDE_B0	Unconditional Debug Event	T21	I	OVDD	—
UDE_B1	Unconditional Debug Event	T22	I	OVDD	—
EE0	DSP Debug Request	T26	I	OVDD	—
EE1	DSP Debug Acknowledge	T25	O	OVDD	2
TMP_DETECT	Tamper Detect	T23	I	OVDD	—
UART_RTS_B00/ **PPS_LED**/ GPO43	UART0 Ready to Send	AB26	O	OVDD	—
Clocking					
SYSCLK	System Clock	AE28	I	OVDD	—
D1_DDRCLK	DDR PLL Reference Clock	V28	I	OVDD	—
D2_DDRCLK	DDR PLL Reference Clock	AC28	I	OVDD	—
RTC	Real Time Clock	AG28	I	OVDD	—
DSP_CLKIN	DSP PLL Reference Clock	W26	I	OVDD	—
TSEC_1588_PULSE_OUT1/ **PPS_OUT**	PPS Pulse Out	AA24	O	LVDD	2
I/O Voltage Select					
BVDD_VSEL00	BVDD Voltage Selection	AB23	I	OVDD	—
BVDD_VSEL01	BVDD Voltage Selection	AA27	I	OVDD	—
CVDD_VSEL	CVDD Voltage Selection	W25	I	OVDD	—
LVDD_VSEL	LVDD Voltage Selection	AD26	I	OVDD	—
XVDD1_VSEL	XVDD 1 Voltage Selection	AC27	I	OVDD	—
XVDD2_VSEL	XVDD 2 Voltage Selection	AD28	I	OVDD	—
Test					
SCAN_MODE_B	Scan Mode	R28	I	OVDD	1
CFG_0_JTAG_MODE	JTAG mode selection 0	U22	I	OVDD	10
CFG_1_JTAG_MODE	JTAG mode selection 1	V22	I	OVDD	10
TEST_SEL_B	Test Select	U28	I	OVDD	11
JTAG (Power Architecture)					
TCK	Test Clock	V23	I	OVDD	
TDI	Test Data In	U26	I	OVDD	3

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO108/ GPIO21/ **IRQ08**	External Interrupt	T7	I	X1VDD	—
IFC_AD12**/** GPIO38**/** **IRQ09**	External Interrupt	G26	I	BVDD	—
ANT1_DIO109/ GPIO22/ **IRQ09**	External Interrupt	U1	I	X1VDD	—
SDHC_CD/ DMA_DACK_B00/ MCP1_B/ GPIO79/ **IRQ10**	External Interrupt	C25	I	BVDD	—
ANT1_DIO106/ GPIO87/ **IRQ10**	External Interrupt	T5	I	X1VDD	—
USB_CLK/ UART_SIN02/ GPIO69/ **IRQ11**/ TIMER03	External Interrupt	R24	I	CVDD	—
ANT1_DIO107/ GPIO88/ **IRQ11**	External Interrupt	T6	I	X1VDD	—
USB_STP/ **IRQ_OUT_B**/ GPO73	Interrupt Output	R25	O	CVDD	—
ANT4_DIO006/ **IRQ_OUT_B**	Interrupt Output	U7	O	X1VDD	—
GPIO					
USB_D04/ **GPIO00**/ IRQ00	General Purpose I/O	P26	I/O	CVDD	—
USB_D03/ **GPIO01**/ IRQ01	General Purpose I/O	N25	I/O	CVDD	—
USB_DIR/ **GPIO02**/ TIMER01/ MCP0_B	General Purpose I/O	P24	I/O	CVDD	—
USB_NXT/ **GPIO03**/ IRQ03/ TRIG_IN	General Purpose I/O	R23	I/O	CVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
AVDD_PLAT	Platform PLL Supply	G7	—	AVDD_PLAT	—
AVDD_CORE0	Core PLL Supply	N20	—	AVDD_CORE0	—
AVDD_CORE1	Core PLL Supply	P20	—	AVDD_CORE1	—
AVDD_D1_DDR	DDR PLL Supply	M20	—	AVDD_D1_DDR	—
AVDD_D2_DDR	DDR PLL Supply	AA1	—	AVDD_D2_DDR	—
AVDD_DSP	DSP PLL Supply	Y16	—	AVDD_DSP	—
AVDD_MAPLE	MAPLE PLL Supply	Y20	—	AVDD_MAPLE	—
SD1AVDD	SerDes PLL Supply	AC22	—	SD1AVDD	—
SD2AVDD	SerDes PLL Supply	AB19	—	SD2AVDD	—
POVDD1	Secure Fuse Programming Overdrive	N23	—	POVDD1	8
POVDD2	Central Fuse Programming Overdrive—DSP	P23	—	—	8
POVDD3	Central Fuse Programming Overdrive—DSP	AA16	—	—	8
FA_VDD	POSt VDD	Y7	—	—	7
VDDC	Core/Platform Supply	J14	—	VDDC	—
VDDC	Core/Platform Supply	K14	—	VDDC	—
VDDC	Core/Platform Supply	L14	—	VDDC	—
VDDC	Core/Platform Supply	M14	—	VDDC	—
VDDC	Core/Platform Supply	N14	—	VDDC	—
VDDC	Core/Platform Supply	P10	—	VDDC	—
VDDC	Core/Platform Supply	P12	—	VDDC	—
VDDC	Core/Platform Supply	P14	—	VDDC	—
VDDC	Core/Platform Supply	R10	—	VDDC	—
VDDC	Core/Platform Supply	R12	—	VDDC	—
VDDC	Core/Platform Supply	R14	—	VDDC	—
VDDC	Core/Platform Supply	T10	—	VDDC	—
VDDC	Core/Platform Supply	T12	—	VDDC	—
VDDC	Core/Platform Supply	T14	—	VDDC	—
VDDC	Core/Platform Supply	U10	—	VDDC	—
VDDC	Core/Platform Supply	U12	—	VDDC	—
VDDC	Core/Platform Supply	U14	—	VDDC	—
VDDC	Core/Platform Supply	V10	—	VDDC	—
VDDC	Core/Platform Supply	V12	—	VDDC	—
VDDC	Core/Platform Supply	V14	—	VDDC	—
VDDC	Core/Platform Supply	W10	—	VDDC	—
VDDC	Core/Platform Supply	W12	—	VDDC	—
VDDC	Core/Platform Supply	W14	—	VDDC	—

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
IFC, GPIO[0:7], eSDHC	47 ± 7	BV_{DD} = 3.3/2.5/1.8 V	—
DDR3 (programmable)	16 32 (half strength mode)	GV_{DD} = 1.5 V DDR3 GV_{DD} = 1.35 V DDR3L	1
eTSEC, USB	47 ± 7	LV_{DD} = 3.3/2.5 V	—
DUART1, system control, I^2C1, USIM, JTAG	47 ± 7	OV_{DD} = 3.3 V	2
USB, eSPI1, DUART2, I^2C2, USIM	47 ± 7	CV_{DD} = 3.3/1.8 V	2
RF parallel interface	LVCMOS	$X1V_{DD}$ = 3.3/1.8 V	—
eSPI2, USB, TDM1, TDM2, RF parallel interface	—	$X2V_{DD}$ = 3.3/1.8 V	—

Note:

1 The drive strength of the DDR3 interface in half-strength mode is at T_j = 125°C and at GV_{DD} (min).

2 USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. VDD, VDDC, AVDD (all PLL supplies), XCOREVDD
2. LVDD, BVDD, CVDD, OVDD, X1VDD, X2VDD, G1VDD, G2VDD, XPADVDD
3. For secure boot fuse programming: After deassertion of HRESET_B, drive POV_{DD1} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD1} = GND before the system is power cycled (HRESET_B assertion) or powered down (V_{DDC} ramp down) per the required timing specified in Table 5. See Section 3.14, "Security Fuse Processor," for additional details.

WARNING

Only 100,000 POR cycles are permitted per lifetime of a device. Only one secure boot fuse programming event is permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND.

POV_{DD2} and POV_{DD3} are always tied to GND.

2.8.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM, and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 22. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{ILAC}	—	 MVREFn – 0.150 MVREFn – 0.175	V	—
AC input high voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{IHAC}	 MVREF*n* + 0.150 MVREF*n* + 0.175	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 23. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage > 1067 MHz data rate ≤ 1067 MHz data rate	V_{ILAC}	—	 MVREF*n* – 0.135 MVREF*n* – 0.160	V	—
AC input high voltage > 1067 MHz data rate ≤ 1067 MHz data rate	V_{IHAC}	 MVREF*n* + 0.135 MVREF*n* + 0.160	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3/3L SDRAM.

Table 24. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
1333 MHz data rate		–125	125		
1200 MHz data rate		–147.5	147.5		
1066 MHz data rate		–170	170		
800 MHz data rate		–200	200		
667 MHz data rate		–240	240		

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating from 3.3-V supply.

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 2.5-V supply.

Table 60. GPIO DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OH}	1.7	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.7	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 1.8-V supply.

Table 61. GPIO DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Table 61. GPIO DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 62. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

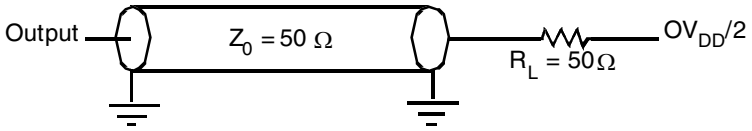


Figure 32. GPIO AC Test Load

2.19 TDM

This section describes the DC and AC electrical specifications for the TDM.

2.19.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics for the TDM interface when operating at 3.3 V.

Table 63. TDM DC Electrical Characteristics ($X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	–0.3	0.8	V	1
Input current ($X2V_{IN}$ = 0 V or $X2V_{IN}$ = $X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage ($X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Table 63. TDM DC Electrical Characteristics ($X2V_{DD}$ = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max $X2V_{IN}$ respective values found in Table 3
2. Note that the symbol $X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

This table provides the DC electrical characteristics for the TDM interface when operating at 1.8 V.

Table 64. TDM DC Electrical Characteristics ($X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($X2V_{IN}$ = 0 V or $X2V_{IN}$ = $X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max $X2V_{IN}$ respective values found in Table 3
2. Note that the symbol $X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

2.19.2 TDM AC Electrical Characteristics

This table provides the input and output AC timing specifications for the TDM interface.

Table 65. TDM AC Timing Specifications for 62.5 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Note
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns	3
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns	3
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns	3
TDM all input setup time	t_{DMIVKH}	3.6	—	ns	4, 5
TDMxRD input hold time	$t_{DMRDIXKH}$	1.9	—	ns	4, 8
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns	5
TDMxTCK high to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns	7
TDMxTCK high to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns	7, 9
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns	7
TDMxTCK high to TDMxTD output high impedance	t_{DM_OUTHI}	—	9.8	ns	7
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns	6
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns	6

Table 66. Differential Signal Definitions (continued)

Term	Definition
Differential Waveform	The differential waveform is constructed by subtracting the inverting signal (SD_TX_B[0:3], for example) from the non-inverting signal (SD_TX_B[0:3], for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 36 as an example for differential waveform.
Common Mode Voltage, V_{cm}	The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TX[0:3]} + V_{SD\_TX\_B[0:3]}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.1.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD_REF_CLK1/SD_REF_CLK1_B or SD_REF_CLK2/SD_REF_CLK2_B. Figure 37 shows a receiver reference diagram of the SerDes reference clocks.

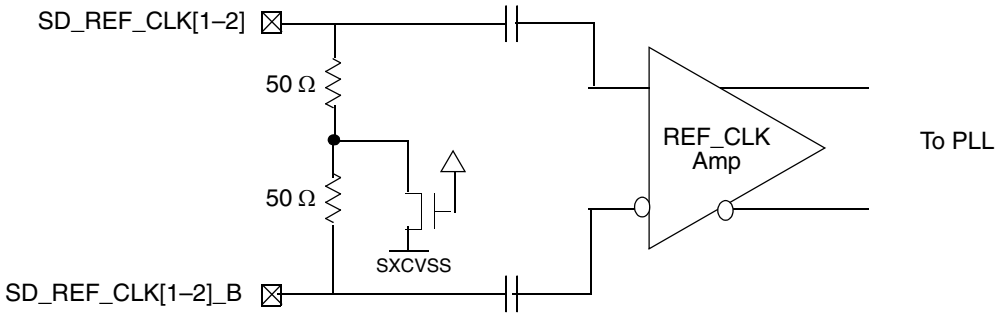


Figure 37. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are:

- The supply voltage requirements for $XCOREV_{DD}$ are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B are internally AC-coupled differential inputs as shown in Figure 37. Each differential clock input (SD_REF_CLK[1–2] or SD_REF_CLK[1–2]_B has on-chip 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.

Table 73. CPRI Receiver DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR compliant channel.
Differential resistance	R_Rdin	80	—	120	Ω	—

Note: LV-II is CEI-6G-LR-based.

2.20.2.4 DC-Level Requirements for SGMII Configurations

Table 74 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Specifications are valid at the recommended operating conditions listed in Table 3.

Table 74. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	500	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000000
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	459	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000010
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	417	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000101
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	376	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001000

Table 77. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. This does not include spread spectrum or REF_CLK jitter. It includes device random jitter at 10^{-12}. See notes 2 and 3.
Time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-NAX-JITTER} = 0.25$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2, 3, and 4.

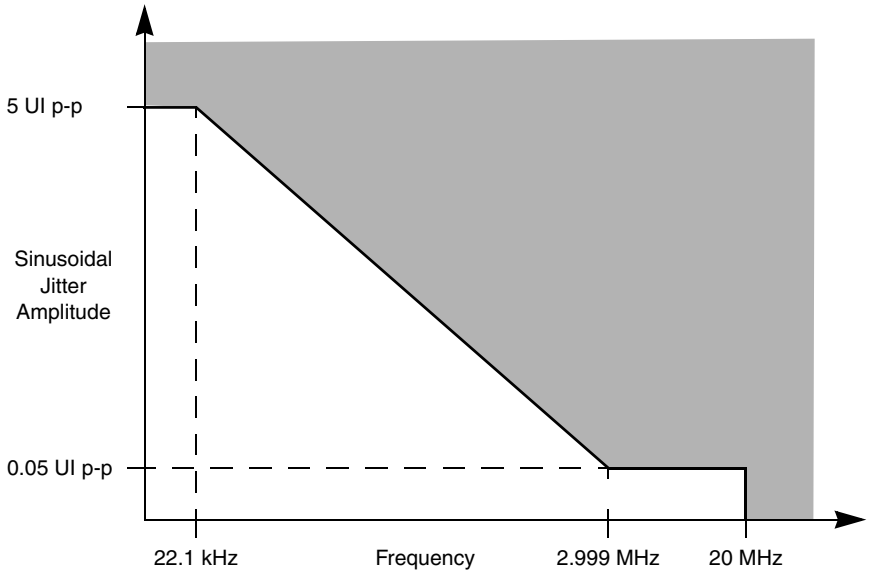


Figure 46. Single Frequency Sinusoidal Jitter Limits for Baud Rate 5.0 Gbps

2.20.3.6 Compliance Test and Measurement Load

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and SD_TX_B*n*) or at the receiver inputs (SD_RX*n* and SD_RX*n*_B). The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 47.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

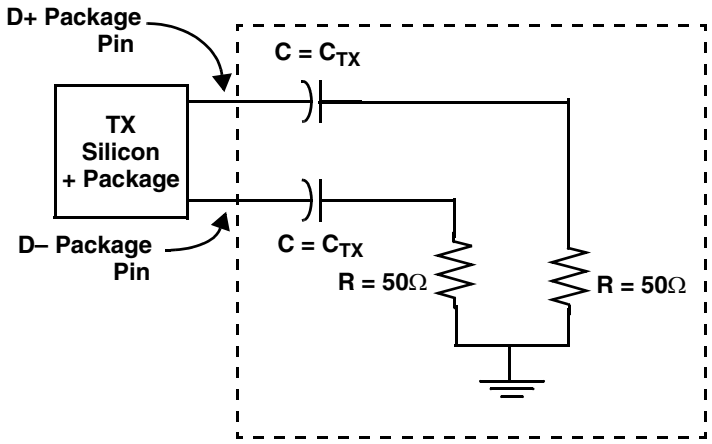
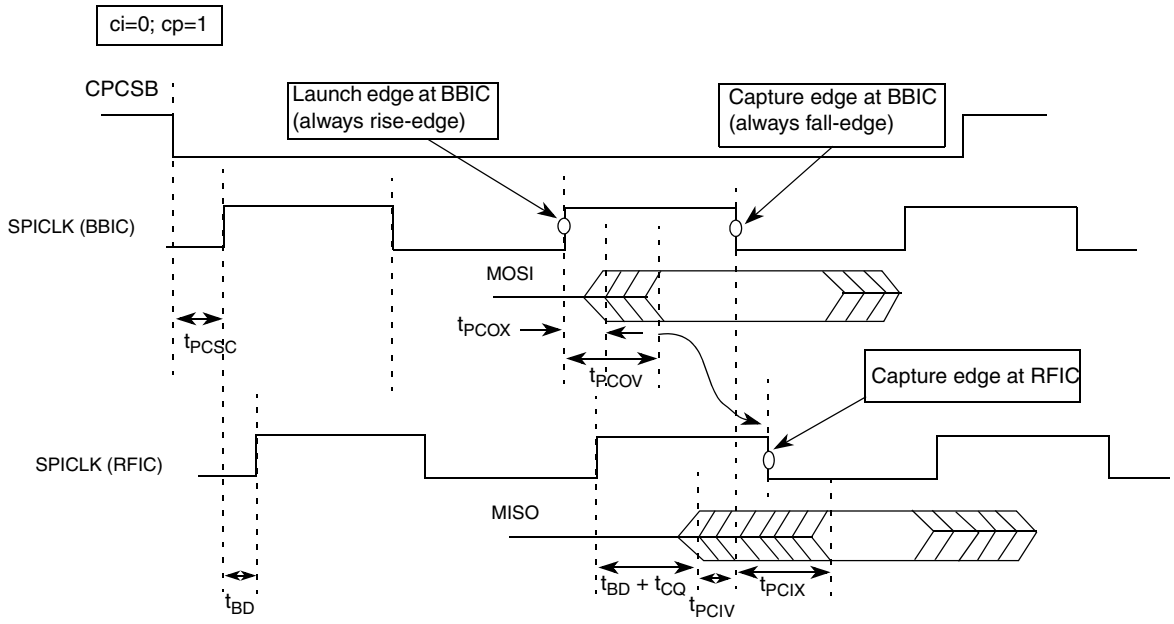


Figure 47. Compliance Test/Measurement Load



t_{BD}: Board delay from the BSC9132 BBIC to the external RFIC or back
t_{CQ}: Delay in RFIC from input of SPICLK to output valid data
Max permissible board skew: 100 ps
Proposed frequency of SPICLK: 30 MHz

Data timing at RF parallel interface:
Input data setup requirement: 1 ns
Input data hold requirement: 0 ns
t_{CQ}: 4.5 ns–6.5 ns (6.5 ns is critical, which defines the max frequency)

Figure 49. RF Parallel Control Plane Interface AC Timing Diagram

2.22 Universal Subscriber Identity Module (USIM)

The USIM module interface consist of a total of five pins. Only “Internal One Wire” interface mode is supported. In this mode, the Rx input of the USIM IP is connected to the TX output of the USIM, which is internal to the device. Only one bidirectional signal (Rx/Tx) is routed to the device pin, which is connected to the external SIM card.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the Rx/Tx pins; however, the SIM module can work with CLK equal to 16 times the data rate on Rx/Tx pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card will be used by the SIM card to recover the clock from the data much like a standard UART. All five pins of SIM module are asynchronous to each other.

There are no required timing relationships between the pads in normal mode, The SIM card is initiated by the interface device, whereupon the SIM card will send a response with an Answer to Reset. Although the SIM interface has no specific requirement, the ISO-7816 specifies reset and power down sequences. For detailed information, see ISO-7816.

The USIM interface pins are available at two locations. At one location, it is multiplexed with eSDHC and TDM functionality and is powered by the BVDD power supply (3.3V/2.5V/1.8V). At the other location, it is multiplexed with eSPI and UART functionality and is powered by CVDD power supply (3.3V/1.8V).

3.2.1 DSP Clock Ranges

Table 104 provides the clocking specifications for the SC3850 processor core, MAPLE, and DSP memory.

Table 104. DSP Processor Clocking Specifications

DSP Core	Minimum Frequency	Maximum Frequency	Unit
SC3850 cores	800	1200	MHz
MAPLE eVTPE	800	800	MHz
DSP DDR Controller	800	1333	MHz

3.2.2 DSPCLKIN and SC3850 Core Frequency Options

Table 105 shows the expected frequency options for DSPCLKIN and SC3850 core frequencies.

Table 105. Options for SC3850 Core0 and Core1 Clocking

PLL_T2 MF	DSPCLKIN Frequency (MHz)			
	66.66	80	100	133
	SC3850 Core Frequency (MHz)			
1	66.66	80	100	133
6	400	480	600	800
7.5	500	600	750	1000
8	533	640	800	1066
9	600	720	900	1200
10	667	800	1000	—
12	800	960	1200	—
15	1000	1200	—	—

3.3 Supply Power Default Setting

This device is capable of supporting multiple power supply levels on its I/O supply. Table 106 through Table 110 shows the encoding used to select the voltage level for each I/O supply. When setting the VSEL signals, "1" is selected through a pull-up resistor to OVDD (as seen in Table 1).

Table 106. Default Voltage Level for BV_{DD}

BVDD_VSEL[0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 V
11	Reserved

3.9 Output Buffer DC Impedance

The drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 58). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

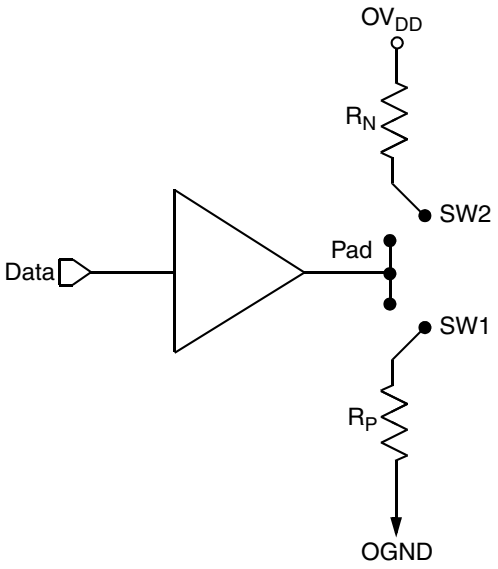


Figure 58. Driver Impedance Measurement

Table 111 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DDC}, nominal OV_{DD}, 90°C.

Table 111. Impedance Characteristics

Impedance	IFC, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	43 Target	20 Target	Z_0	W
R_P	43 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 2.

3.10 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET_B is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET_B is asserted, is latched when HRESET_B deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET_B (and for platform/system clocks after HRESET_B deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with