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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=bsc9132nsn7mnmb

Figure 5 shows detailed view C.

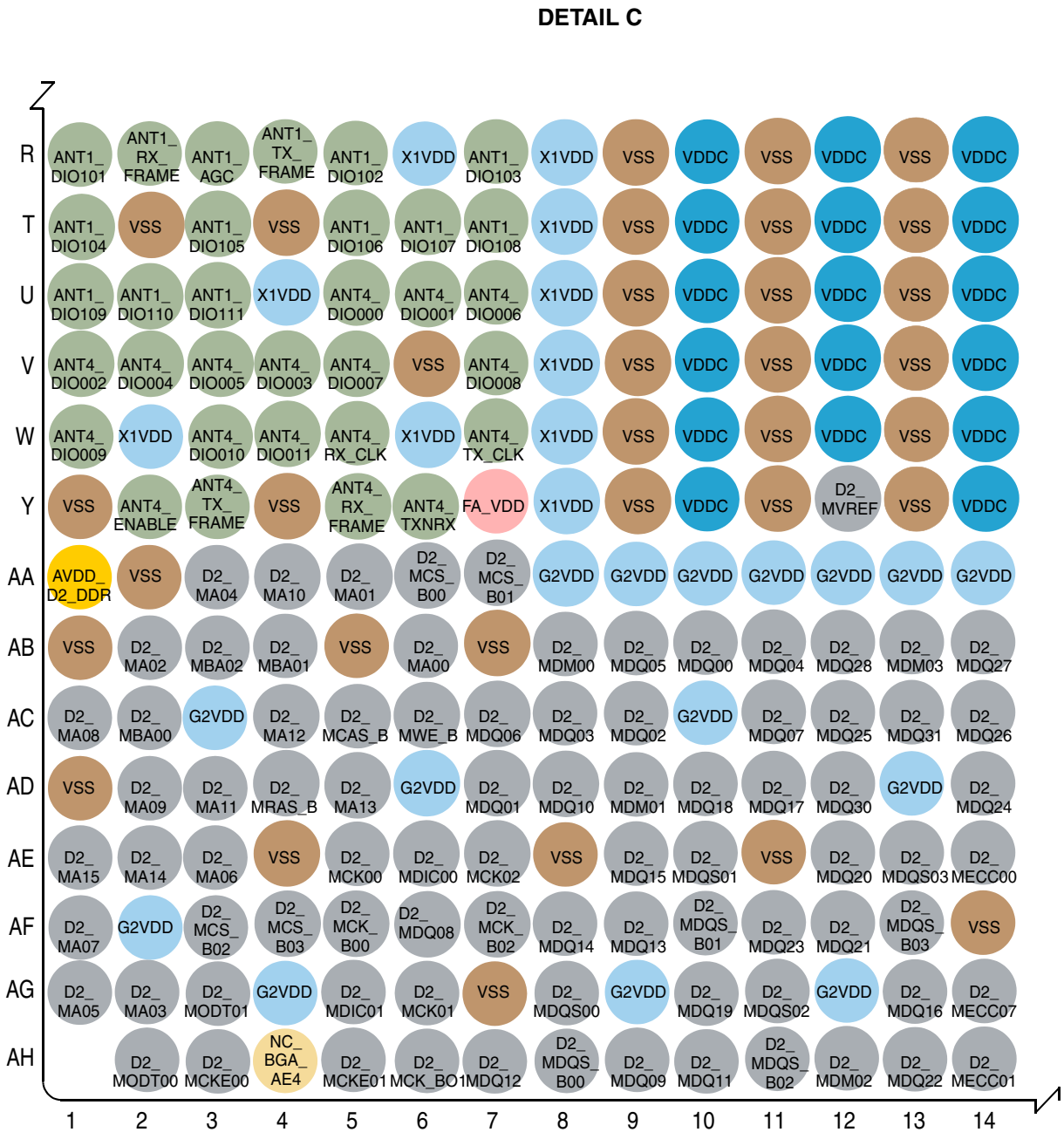


Figure 5. Ball Layout Diagram—Detail C

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_AD12/ GPIO38/ IRQ09	IFC Muxed Address,Data	G26	I/O	BVDD	—
IFC_AD13/ GPIO39/ IRQ07	IFC Muxed Address,Data	G27	I/O	BVDD	—
IFC_AD14/ GPIO40/ IRQ06	IFC Muxed Address,Data	G28	I/O	BVDD	—
IFC_AD15/ GPIO41/ TIMER02	IFC Muxed Address,Data	H28	I/O	BVDD	—
IFC_ADDR16/ GPO08	IFC Address	H26	O	BVDD	2
IFC_ADDR17/ GPO09	IFC Address	H25	O	BVDD	2
IFC_ADDR18/ GPO10	IFC Address	H24	O	BVDD	2
IFC_ADDR19/ GPO11	IFC Address	H22	O	BVDD	2
IFC_ADDR20/ GPO12	IFC Address	H21	O	BVDD	2
IFC_ADDR21/ GPO13	IFC Address	J28	O	BVDD	2
IFC_ADDR22/ GPO14	IFC Address	J27	O	BVDD	18
IFC_ADDR23/ GPO15	IFC Address	J25	O	BVDD	2
IFC_ADDR24/ GPO16	IFC Address	J24	O	BVDD	2
IFC_ADDR25/ GPO17	IFC Address	J23	O	BVDD	2
IFC_ADDR26/ GPO18	IFC Address	J22	O	BVDD	2
IFC_AVD/ GPO54	IFC Address Valid	L28	O	BVDD	2
IFC_CS_B00/ GPO55	IFC Chip Select	K21	O	BVDD	—
IFC_CS_B01/ GPO64	IFC Chip Select	K28	O	BVDD	—
IFC_CS_B02/ GPO65	IFC Chip Select	L24	O	BVDD	—
IFC_WE_B/ GPO52	IFC Write Enable/GPCM Write Byte Select0/ Generic ASIC i/f Start of Frame	L26	O	BVDD	2

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI1_CS3_B/ **CKSTP1_OUT_B**/ GPO76	Checkstop Out	M23	O	CVDD	—
READY/ ASLEEP/ READY_P1	Ready/Trigger Out/Asleep	U21	O	OVDD	2
UDE_B0	Unconditional Debug Event	T21	I	OVDD	—
UDE_B1	Unconditional Debug Event	T22	I	OVDD	—
EE0	DSP Debug Request	T26	I	OVDD	—
EE1	DSP Debug Acknowledge	T25	O	OVDD	2
TMP_DETECT	Tamper Detect	T23	I	OVDD	—
UART_RTS_B00/ **PPS_LED**/ GPO43	UART0 Ready to Send	AB26	O	OVDD	—
Clocking					
SYSCLK	System Clock	AE28	I	OVDD	—
D1_DDRCLK	DDR PLL Reference Clock	V28	I	OVDD	—
D2_DDRCLK	DDR PLL Reference Clock	AC28	I	OVDD	—
RTC	Real Time Clock	AG28	I	OVDD	—
DSP_CLKIN	DSP PLL Reference Clock	W26	I	OVDD	—
TSEC_1588_PULSE_OUT1/ **PPS_OUT**	PPS Pulse Out	AA24	O	LVDD	2
I/O Voltage Select					
BVDD_VSEL00	BVDD Voltage Selection	AB23	I	OVDD	—
BVDD_VSEL01	BVDD Voltage Selection	AA27	I	OVDD	—
CVDD_VSEL	CVDD Voltage Selection	W25	I	OVDD	—
LVDD_VSEL	LVDD Voltage Selection	AD26	I	OVDD	—
XVDD1_VSEL	XVDD 1 Voltage Selection	AC27	I	OVDD	—
XVDD2_VSEL	XVDD 2 Voltage Selection	AD28	I	OVDD	—
Test					
SCAN_MODE_B	Scan Mode	R28	I	OVDD	1
CFG_0_JTAG_MODE	JTAG mode selection 0	U22	I	OVDD	10
CFG_1_JTAG_MODE	JTAG mode selection 1	V22	I	OVDD	10
TEST_SEL_B	Test Select	U28	I	OVDD	11
JTAG (Power Architecture)					
TCK	Test Clock	V23	I	OVDD	
TDI	Test Data In	U26	I	OVDD	3

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_AD09/ **GPIO35**	General Purpose I/O	F27	I/O	BVDD	—
IFC_AD10/ **GPIO36**	General Purpose I/O	F28	I/O	BVDD	—
IFC_AD11/ **GPIO37/** IRQ08	General Purpose I/O	G25	I/O	BVDD	—
IFC_AD12/ **GPIO38/** IRQ09	General Purpose I/O	G26	I/O	BVDD	—
IFC_AD13/ **GPIO39/** IRQ07	General Purpose I/O	G27	I/O	BVDD	—
IFC_AD14/ **GPIO40/** IRQ06	General Purpose I/O	G28	I/O	BVDD	—
IFC_AD15/ **GPIO41/** TIMER02	General Purpose I/O	H28	I/O	BVDD	—
UART_CTS_B00/ SIM_PD/ TIMER04/ **GPIO42**/ IRQ04	General Purpose I/O	AB27	I/O	OVDD	—
UART_CTS_B01/ SYS_DMA_REQ/ SRESET_B/ **GPIO44**/ IRQ05	General Purpose I/O	W22	I/O	OVDD	—
IIC1_SDA/ **GPIO46**	General Purpose I/O	V25	I/O	OVDD	—
IIC1_SCL/ **GPIO47**	General Purpose I/O	V24	I/O	OVDD	—
SDHC_CMD/ SIM_RST_B/ **GPIO48**	General Purpose I/O	C26	I/O	BVDD	—
SDHC_DATA00/ SIM_TRXD/ **GPIO49**	General Purpose I/O	D25	I/O	BVDD	—
SDHC_DATA01/ SIM_SVEN/ **GPIO50**	General Purpose I/O	F23	I/O	BVDD	—
SDHC_DATA02/ SIM_PD/ **GPIO51**	General Purpose I/O	F24	I/O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
G1VDD	DDR Supply	E11	—	G1VDD	—
G1VDD	DDR Supply	H9	—	G1VDD	—
G1VDD	DDR Supply	H10	—	G1VDD	—
G1VDD	DDR Supply	H11	—	G1VDD	—
G1VDD	DDR Supply	H12	—	G1VDD	—
G1VDD	DDR Supply	H13	—	G1VDD	—
G1VDD	DDR Supply	H14	—	G1VDD	—
G1VDD	DDR Supply	H15	—	G1VDD	—
G1VDD	DDR Supply	H16	—	G1VDD	—
G1VDD	DDR Supply	H17	—	G1VDD	—
G1VDD	DDR Supply	H18	—	G1VDD	—
G1VDD	DDR Supply	H19	—	G1VDD	—
G1VDD	DDR Supply	H20	—	G1VDD	—
G1VDD	DDR Supply	B18	—	G1VDD	—
G1VDD	DDR Supply	B23	—	G1VDD	—
G1VDD	DDR Supply	D20	—	G1VDD	—
G1VDD	DDR Supply	E15	—	G1VDD	—
G2VDD	DDR Supply	AC3	—	G2VDD	—
G2VDD	DDR Supply	AC10	—	G2VDD	—
G2VDD	DDR Supply	AA8	—	G2VDD	—
G2VDD	DDR Supply	AA9	—	G2VDD	—
G2VDD	DDR Supply	AA10	—	G2VDD	—
G2VDD	DDR Supply	AA11	—	G2VDD	—
G2VDD	DDR Supply	AA12	—	G2VDD	—
G2VDD	DDR Supply	AA13	—	G2VDD	—
G2VDD	DDR Supply	AA14	—	G2VDD	—
G2VDD	DDR Supply	AA15	—	G2VDD	—
G2VDD	DDR Supply	AD6	—	G2VDD	—
G2VDD	DDR Supply	AD13	—	G2VDD	—
G2VDD	DDR Supply	AF2	—	G2VDD	—
G2VDD	DDR Supply	AG4	—	G2VDD	—
G2VDD	DDR Supply	AG9	—	G2VDD	—
G2VDD	DDR Supply	AG12	—	G2VDD	—
G2VDD	DDR Supply	AC15	—	G2VDD	—
LVDD	Ethernet Supply	Y23	—	LVDD	—
LVDD	Ethernet Supply	AA25	—	LVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	C7	—	—	—
VSS	Platform and Core Ground	D2	—	—	—
VSS	Platform and Core Ground	D7	—	—	—
VSS	Platform and Core Ground	D9	—	—	—
VSS	Platform and Core Ground	E4	—	—	—
VSS	Platform and Core Ground	E8	—	—	—
VSS	Platform and Core Ground	F6	—	—	—
VSS	Platform and Core Ground	F7	—	—	—
VSS	Platform and Core Ground	F8	—	—	—
VSS	Platform and Core Ground	F13	—	—	—
VSS	Platform and Core Ground	G6	—	—	—
VSS	Platform and Core Ground	G8	—	—	—
VSS	Platform and Core Ground	H4	—	—	—
VSS	Platform and Core Ground	H6	—	—	—
VSS	Platform and Core Ground	H7	—	—	—
VSS	Platform and Core Ground	H8	—	—	—
VSS	Platform and Core Ground	J9	—	—	—
VSS	Platform and Core Ground	J11	—	—	—
VSS	Platform and Core Ground	K2	—	—	—
VSS	Platform and Core Ground	K9	—	—	—
VSS	Platform and Core Ground	K11	—	—	—
VSS	Platform and Core Ground	K13	—	—	—
VSS	Platform and Core Ground	L6	—	—	—
VSS	Platform and Core Ground	L9	—	—	—
VSS	Platform and Core Ground	L11	—	—	—
VSS	Platform and Core Ground	L13	—	—	—
VSS	Platform and Core Ground	M11	—	—	—
VSS	Platform and Core Ground	M13	—	—	—
VSS	Platform and Core Ground	M4	—	—	—
VSS	Platform and Core Ground	M9	—	—	—
VSS	Platform and Core Ground	N9	—	—	—
VSS	Platform and Core Ground	N11	—	—	—
VSS	Platform and Core Ground	N13	—	—	—
VSS	Platform and Core Ground	P9	—	—	—
VSS	Platform and Core Ground	P11	—	—	—
VSS	Platform and Core Ground	P13	—	—	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
NC	Address Parity Error	E19	—	—	—
NC	Address Parity Error	AH4	—	—	—

1 These are test signals for factory use only and must be pulled up (with 100 Ω–1 kΩ) to OVDD for normal operation.

2 This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.

3 These pins have weak internal pull-up P-FETs that are always enabled.

4 This pin must NOT be pulled down during power-on reset.

5 This pin is an open drain signal.

6 This pin should be pulled down with 200Ω ± 1% resistor when used in autocalibration mode.

7 This pin should be pulled down to VSS with 10 kΩ.

8 This pin is used for fuse programming. Should be tied to VSS for normal operation (fuse read). See section Section 2.2, “Power Sequencing,” for more details.

9 This pin may be connected to a temperature diode monitoring device such as the Analog Devices, ADT7461A™. If a temperature diode monitoring device will not be connected, these pins may be connected to test point or left as a no connect.

10 Pin should be pulled high or low depending on the JTAG topology selected. Refer to Section 3.11, “JTAG Configuration Signals.”

11 This pin should be tied to GND/VSS when MAPLE is powered down; otherwise it should be tied to OVDD.

12 This pin is an open-drain signal if the IIC2 pin is selected.

13 It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.

14 MDIC00 is grounded through an 36.5 O precision 1% resistor and MDIC01 is connected to GVDD through an 36.5 O precision 1% resistor. These pins are used for automatic calibration of the DDR3/DDR3L IOs.

15 This pin should be pulled up to power rail with 10 kΩ.

16 Do not use this pin as CD pin.

17 This pin should be pulled down to GND with 10 kΩ.

18 This pin is a reset configuration pin without default value.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
IFC, GPIO[0:7], eSDHC	47 ± 7	BV_{DD} = 3.3/2.5/1.8 V	—
DDR3 (programmable)	16 32 (half strength mode)	GV_{DD} = 1.5 V DDR3 GV_{DD} = 1.35 V DDR3L	1
eTSEC, USB	47 ± 7	LV_{DD} = 3.3/2.5 V	—
DUART1, system control, I^2C1, USIM, JTAG	47 ± 7	OV_{DD} = 3.3 V	2
USB, eSPI1, DUART2, I^2C2, USIM	47 ± 7	CV_{DD} = 3.3/1.8 V	2
RF parallel interface	LVCMOS	$X1V_{DD}$ = 3.3/1.8 V	—
eSPI2, USB, TDM1, TDM2, RF parallel interface	—	$X2V_{DD}$ = 3.3/1.8 V	—

Note:

1 The drive strength of the DDR3 interface in half-strength mode is at T_j = 125°C and at GV_{DD} (min).

2 USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. VDD, VDDC, AVDD (all PLL supplies), XCOREVDD
2. LVDD, BVDD, CVDD, OVDD, X1VDD, X2VDD, G1VDD, G2VDD, XPADVDD
3. For secure boot fuse programming: After deassertion of HRESET_B, drive POV_{DD1} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD1} = GND before the system is power cycled (HRESET_B assertion) or powered down (V_{DDC} ramp down) per the required timing specified in Table 5. See Section 3.14, "Security Fuse Processor," for additional details.

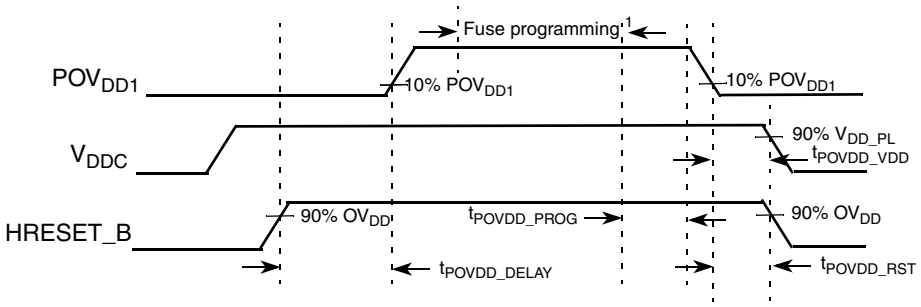
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device. Only one secure boot fuse programming event is permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND.

POV_{DD2} and POV_{DD3} are always tied to GND.

This figure provides the POV_{DD1} timing diagram.



NOTE: POVDD must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD1} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD1}.

Table 5. POV_{DD1} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	1500	—	t_{SYSCLK}	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the deassertion of HRESET_B to driving POV_{DD1} ramp up. Delay measured from HRESET_B deassertion at 90% OV_{DD} to 10% POV_{DD1} ramp up.
2. Delay required from fuse programming finished to POV_{DD1} ramp down start. Fuse programming must complete while POV_{DD1} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND. After fuse programming is completed, it is required to return POV_{DD1} = GND.
3. Delay required from POV_{DD1} ramp down complete to V_{DDC} ramp down start. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before V_{DDC} is at 90% V_{DDC}.
4. Delay required from POV_{DD1} ramp down complete to HRESET_B assertion. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before HRESET_B assertion reaches 90% OV_{DD}.
5. Only one secure boot fuse programming event is permitted per lifetime of a device.

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, the sequencing for GV_{DD} is not required.

Table 24. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	2
1333 MHz data rate		–250	250		
1200 MHz data rate		–275	275		
1066 MHz data rate		–300	300		
800 MHz data rate		–425	425		
667 MHz data rate		–510	510		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

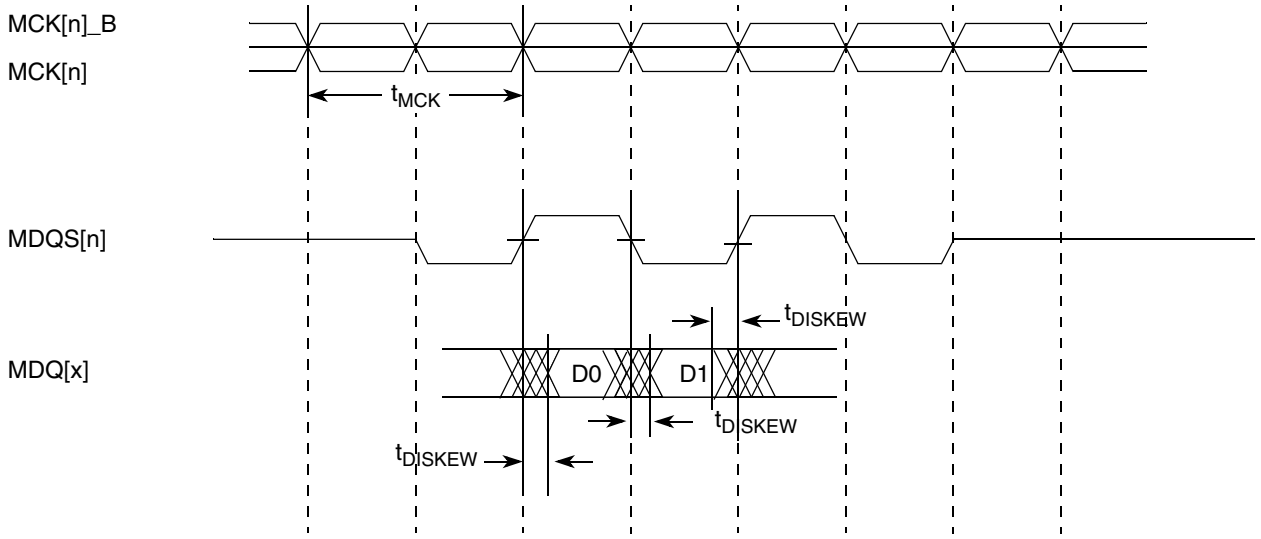


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

2.8.2.2 DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR3 and DDR3L SDRAM interface.

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	1.5	3	ns	2

Table 38. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V) (continued)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.11.3.2 eTSEC IEEE Std 1588 AC Specifications

This table provides the IEEE Std 1588 AC timing specifications.

Table 39. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	5	—	T_{RX_CLK}*7	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns respectively.

Table 42. USB General Timing Parameters (ULPI Mode) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 19 and Figure 20 provide the USB AC test load and signals, respectively.

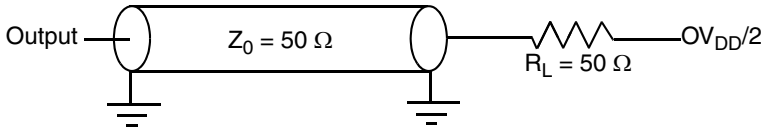


Figure 19. USB AC Test Load

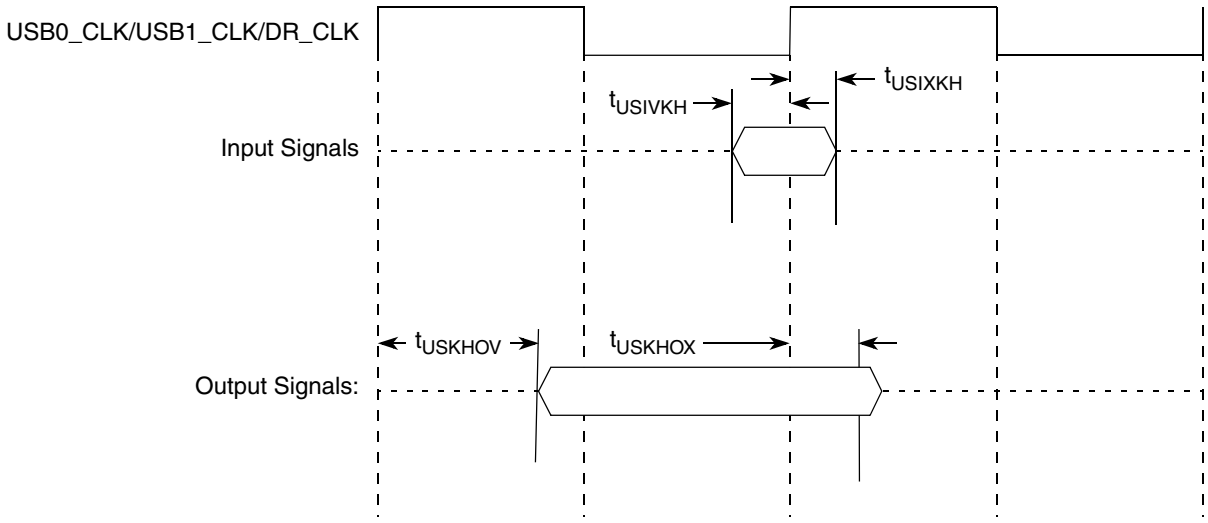


Figure 20. USB Signals

Table 63. TDM DC Electrical Characteristics ($X2V_{DD}$ = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max $X2V_{IN}$ respective values found in Table 3
2. Note that the symbol $X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

This table provides the DC electrical characteristics for the TDM interface when operating at 1.8 V.

Table 64. TDM DC Electrical Characteristics ($X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($X2V_{IN}$ = 0 V or $X2V_{IN}$ = $X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max $X2V_{IN}$ respective values found in Table 3
2. Note that the symbol $X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

2.19.2 TDM AC Electrical Characteristics

This table provides the input and output AC timing specifications for the TDM interface.

Table 65. TDM AC Timing Specifications for 62.5 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Note
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns	3
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns	3
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns	3
TDM all input setup time	t_{DMIVKH}	3.6	—	ns	4, 5
TDMxRD input hold time	$t_{DMRDIXKH}$	1.9	—	ns	4, 8
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns	5
TDMxTCK high to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns	7
TDMxTCK high to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns	7, 9
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns	7
TDMxTCK high to TDMxTD output high impedance	t_{DM_OUTHI}	—	9.8	ns	7
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns	6
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns	6

This figure shows the TDM transmit signal timing.

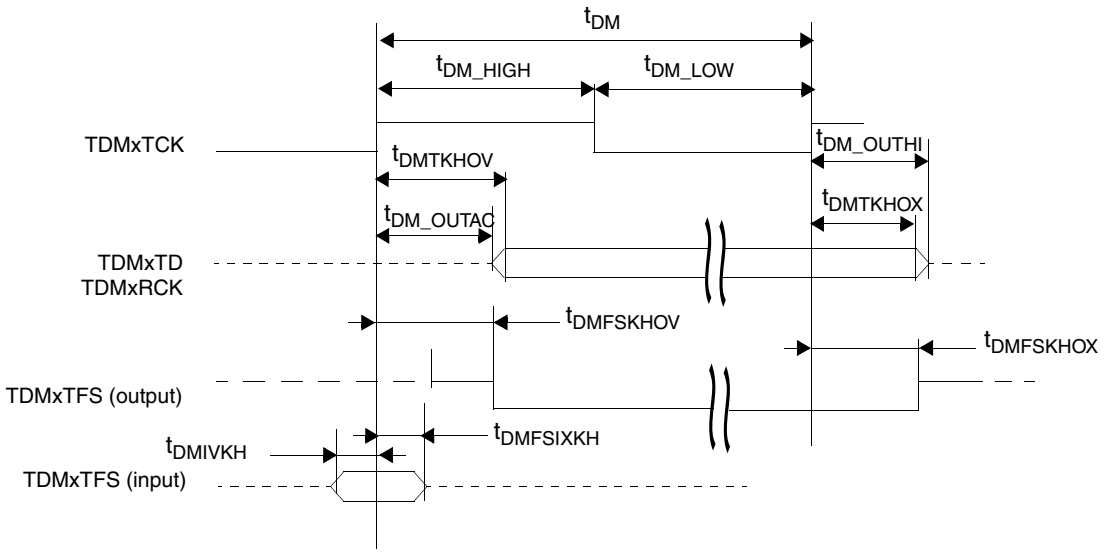


Figure 34. TDM Transmit Signals

This figure provides the AC test load for the TDM.

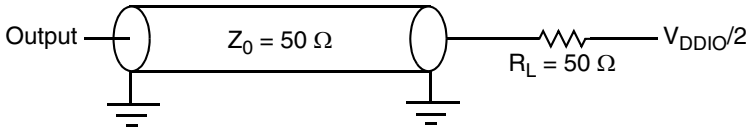


Figure 35. TDM AC Test Load

2.20 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The device features an HSSI that includes one 4-channel SerDes port (lanes 0 through 3) used for high-speed serial interface applications (PCI Express, CPRI, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the reset configuration word. Specific AC electrical characteristics are defined in Section 2.20.3, “HSSI AC Timing Specifications.”

Table 73. CPRI Receiver DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR compliant channel.
Differential resistance	R_Rdin	80	—	120	Ω	—

Note: LV-II is CEI-6G-LR-based.

2.20.2.4 DC-Level Requirements for SGMII Configurations

Table 74 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Specifications are valid at the recommended operating conditions listed in Table 3.

Table 74. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	500	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000000
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	459	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000010
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	417	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000101
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	376	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001000

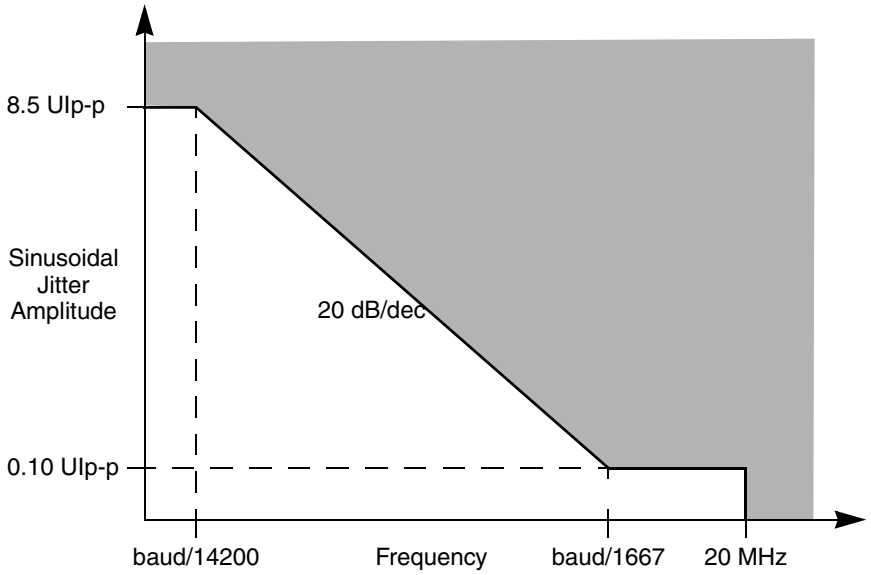


Figure 44. Single Frequency Sinusoidal Jitter Limits for Baud Rate <3.125 Gbps

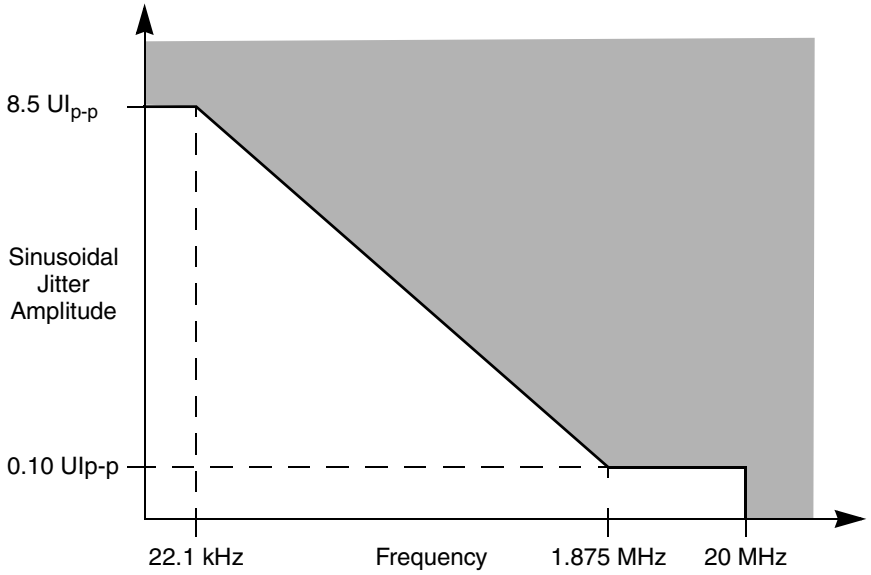
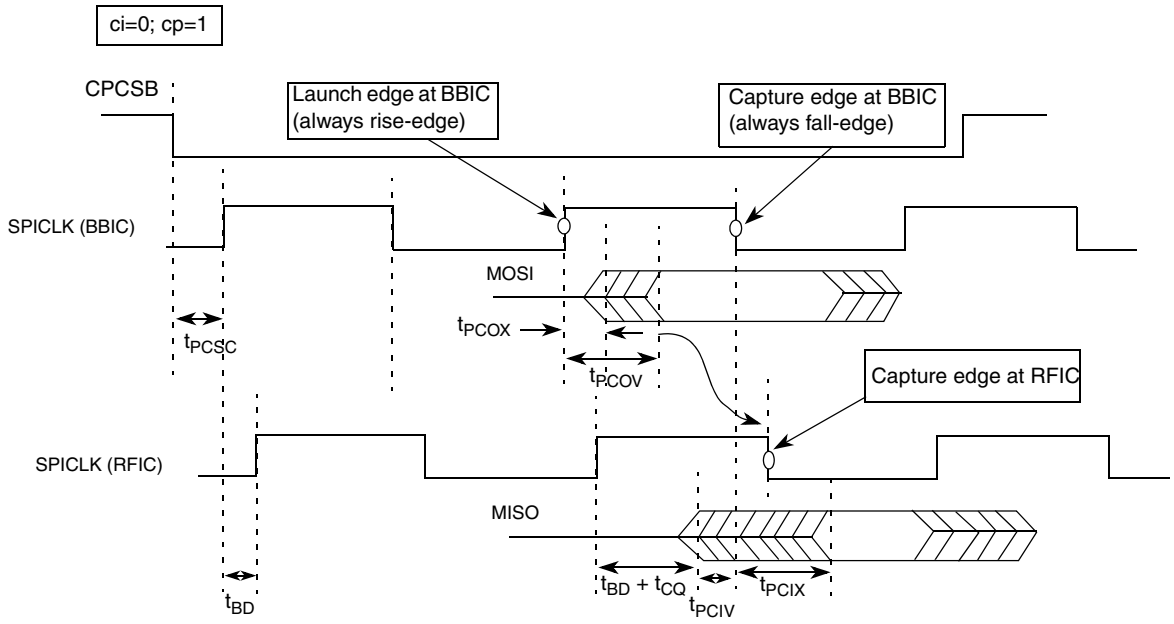


Figure 45. Single Frequency Sinusoidal Jitter Limits for Baud Rate 3.125 Gbps



t_{BD}: Board delay from the BSC9132 BBIC to the external RFIC or back
t_{CQ}: Delay in RFIC from input of SPICLK to output valid data
Max permissible board skew: 100 ps
Proposed frequency of SPICLK: 30 MHz

Data timing at RF parallel interface:
Input data setup requirement: 1 ns
Input data hold requirement: 0 ns
t_{CQ}: 4.5 ns–6.5 ns (6.5 ns is critical, which defines the max frequency)

Figure 49. RF Parallel Control Plane Interface AC Timing Diagram

2.22 Universal Subscriber Identity Module (USIM)

The USIM module interface consist of a total of five pins. Only “Internal One Wire” interface mode is supported. In this mode, the Rx input of the USIM IP is connected to the TX output of the USIM, which is internal to the device. Only one bidirectional signal (Rx/Tx) is routed to the device pin, which is connected to the external SIM card.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the Rx/Tx pins; however, the SIM module can work with CLK equal to 16 times the data rate on Rx/Tx pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card will be used by the SIM card to recover the clock from the data much like a standard UART. All five pins of SIM module are asynchronous to each other.

There are no required timing relationships between the pads in normal mode, The SIM card is initiated by the interface device, whereupon the SIM card will send a response with an Answer to Reset. Although the SIM interface has no specific requirement, the ISO-7816 specifies reset and power down sequences. For detailed information, see ISO-7816.

The USIM interface pins are available at two locations. At one location, it is multiplexed with eSDHC and TDM functionality and is powered by the BVDD power supply (3.3V/2.5V/1.8V). At the other location, it is multiplexed with eSPI and UART functionality and is powered by CVDD power supply (3.3V/1.8V).

the isolation resistor allows future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.

- TCK should be pulled down to GND through a 1 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TDO, or TMS.

NOTE

In the case where the DSP JTAG is also used (as described in Table 112), DSP_TRST and DSP_TCK need to be handled in the same way as TRST and TCK are, as mentioned above.

3.12 Guidelines for High-Speed Interface Termination

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[3:0]
- SD_TX_B[3:0]

The following pins must be connected to GND:

- SD_RX[3:0], SD_RX_B[3:0]
- SD_REF_CLK, SD_REF_CLK_B

3.13 Thermal

This section describes the thermal specifications.

3.13.1 Thermal Characteristics

Table 113 provides the package thermal characteristics.

Table 113. Package Thermal Resistance Characteristics

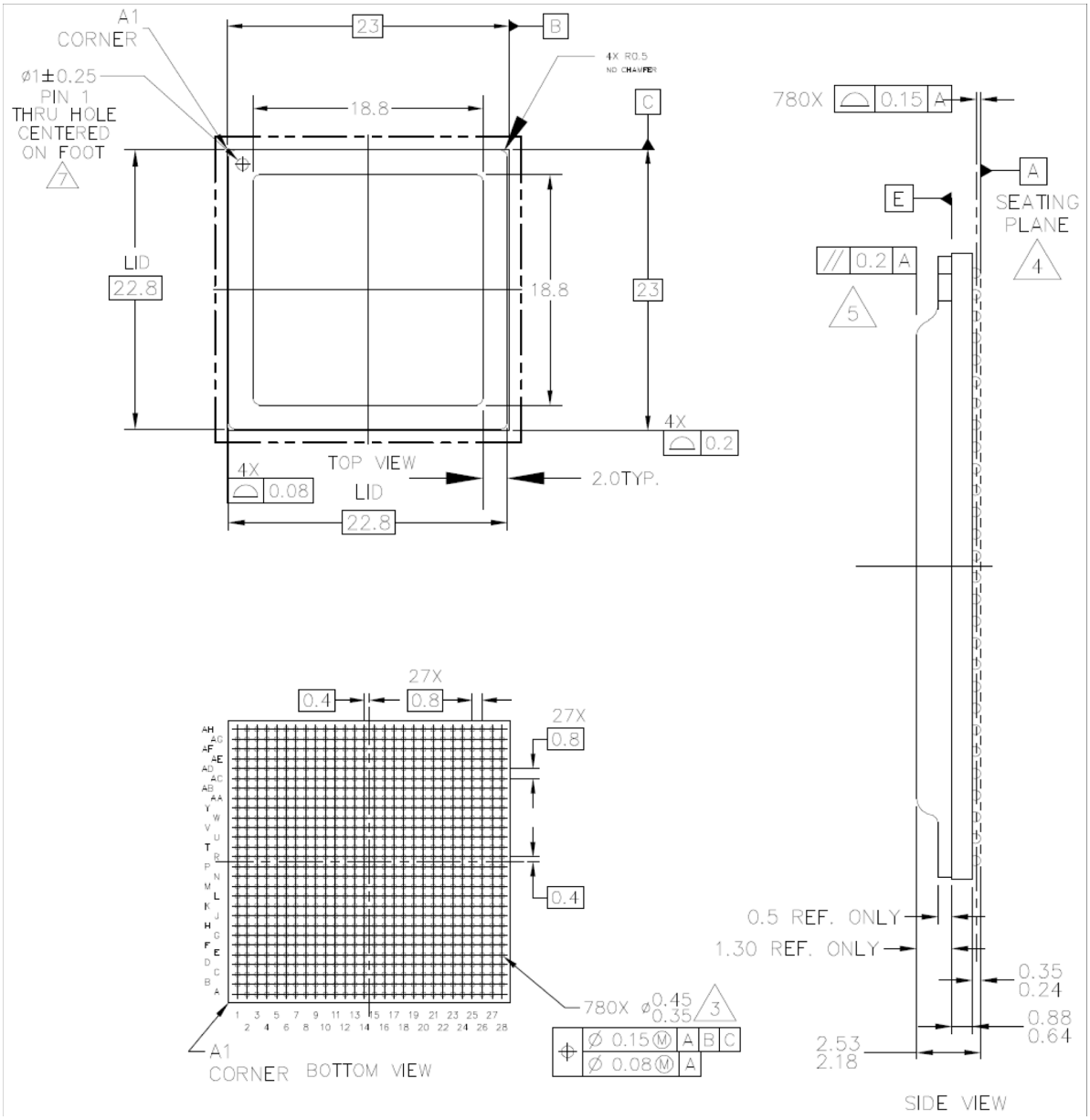
Characteristic	JEDEC Board	Symbol	Lid	Unit
Junction-to-Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	21	°C/W
Junction-to-Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W
Junction-to-Ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	15	°C/W
Junction-to-Ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	11	°C/W
Junction-to-Board	—	$R_{\theta JB}$	4.0	°C/W
Junction-to-Case Top	—	$R_{\theta JCtop}$	0.7	°C/W

Note:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.2 Mechanical Dimensions of the FC-PBGA

Figure 61 shows the package and bottom surface nomenclature.



Notes:
1. All dimentions are in milimeters.
2. Dimensions and tolerancing per ASME Y14.5-1994.
3. Maximum ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 through hole should be centered within foot area.

Figure 61. BSC9132 Mechanical Dimensions and Package Diagram

5 Ordering Information

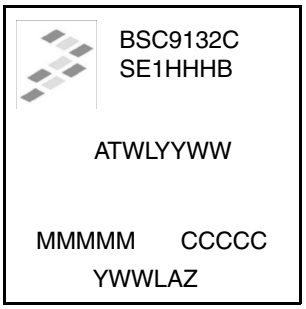
The table below provides the Freescale part numbering nomenclature for the BSC9132. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 114. Part numbering nomenclature

	n	*x*	*t*	*e*	*n*	*c*	*d*	*f*	*r*
Product Code	**Part Identifier**	**Qual Status**	**Temp Range**	**Encryp-tion**	**Package Type**	**CPU Freq**	**DDR Speed**	**DSP Freq**	**Die Revision**
BSC	9132	N = Industrial Tier	S, L = Std temp (0–105°C) X, J = Ext temp (-40–105°C)	E = SEC Present N = No SEC Present	7 = FC-PBGA Pb-free Bumps and Package	K = 1000 MHz M = 1200 MHz P = 1400 MHz	N = 1333 MHz	K = 1000 MHz M = 1200 MHz	B = Rev 1.1

5.1 Part Marking

Parts are marked as the example shown in this figure.



FCPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.
BSC9132CSE1HHHB is the orderable part number. See Table 114 for details.

Figure 62. Part Marking for FCPBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part. Some documents may require a non-disclosure agreement. Contact your local FAE for assistance.

- *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* (BSC9132RM)