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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SC3850, Security; SEC 4.4
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=bsc9132nxe7knkb

Table 1. BSC9132 Pinout Listing

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
DDR 1 (Power Architecture)					
D1_MDQ00	Data	F16	I/O	G1VDD	—
D1_MDQ01	Data	G16	I/O	G1VDD	—
D1_MDQ02	Data	G15	I/O	G1VDD	—
D1_MDQ03	Data	E18	I/O	G1VDD	—
D1_MDQ04	Data	E16	I/O	G1VDD	—
D1_MDQ05	Data	F17	I/O	G1VDD	—
D1_MDQ06	Data	G17	I/O	G1VDD	—
D1_MDQ07	Data	F15	I/O	G1VDD	—
D1_MDQ08	Data	C17	I/O	G1VDD	—
D1_MDQ09	Data	A15	I/O	G1VDD	—
D1_MDQ10	Data	B16	I/O	G1VDD	—
D1_MDQ11	Data	C14	I/O	G1VDD	—
D1_MDQ12	Data	A16	I/O	G1VDD	—
D1_MDQ13	Data	C15	I/O	G1VDD	—
D1_MDQ14	Data	D14	I/O	G1VDD	—
D1_MDQ15	Data	D15	I/O	G1VDD	—
D1_MDQ16	Data	G12	I/O	G1VDD	—
D1_MDQ17	Data	F14	I/O	G1VDD	—
D1_MDQ18	Data	G14	I/O	G1VDD	—
D1_MDQ19	Data	E14	I/O	G1VDD	—
D1_MDQ20	Data	E12	I/O	G1VDD	—
D1_MDQ21	Data	E13	I/O	G1VDD	—
D1_MDQ22	Data	G11	I/O	G1VDD	—
D1_MDQ23	Data	G13	I/O	G1VDD	—
D1_MDQ24	Data	D10	I/O	G1VDD	—
D1_MDQ25	Data	D12	I/O	G1VDD	—
D1_MDQ26	Data	C10	I/O	G1VDD	—
D1_MDQ27	Data	D11	I/O	G1VDD	—
D1_MDQ28	Data	A11	I/O	G1VDD	—
D1_MDQ29	Data	B9	I/O	G1VDD	—
D1_MDQ30	Data	C12	I/O	G1VDD	—
D1_MDQ31	Data	C9	I/O	G1VDD	—
D1_MDM00	Data Mask	E17	O	G1VDD	—
D1_MDM01	Data Mask	A13	O	G1VDD	—
D1_MDM02	Data Mask	F12	O	G1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO104/ **TDM1_RCK**/ GPIO92	TDM1 Receive Clock	K4	I/O	X2VDD	—
ANT2_DIO105/ **TDM1_RFS**/ TIMER08	TDM1 Receive Frame Sync	K7	I/O	X2VDD	—
ANT2_DIO102/ **TDM1_RXD**	TDM1 Receive Data	J7	I/O	X2VDD	—
TDM2 over RF3					
ANT3_RX_CLK/ **TDM2_TCK**/ GPIO04	TDM2 Clock	D1	I/O	X2VDD	—
ANT3_DIO007/ **TDM2_TFS**	TDM2 Transmit Frame Sync	B3	I/O	X2VDD	—
ANT3_DIO011/ **TDM2_TXD**	TDM2 Transmit Data	B1	I/O	X2VDD	—
ANT3_DIO008/ **TDM2_RCK**/ CKSTP0_OUT_B	TDM2 Receive Clock	A2	I/O	X2VDD	—
ANT3_DIO009/ **TDM2_RFS**/ CKSTP1_OUT_B	TDM2 Receive Frame Sync	C3	I/O	X2VDD	—
ANT3_DIO010/ **TDM2_RXD**	TDM2 Receive Data	D4	I/O	X2VDD	—
SerDes					
SD_TX03	Tx Data out	AE19	O	XPADVDD	—
SD_TX02	Tx Data out	AE21	O	XPADVDD	—
SD_TX01	Tx Data out	AE23	O	XPADVDD	—
SD_TX00	Tx Data out	AE25	O	XPADVDD	—
SD_TX_B03	Tx Data out, inverted	AF19	O	XPADVDD	—
SD_TX_B02	Tx Data out, inverted	AF21	O	XPADVDD	—
SD_TX_B01	Tx Data out, inverted	AF23	O	XPADVDD	—
SD_TX_B00	Tx Data out, inverted	AF25	O	XPADVDD	—
SD_RX03	Rx Data in	AG18	I	XCOREVDD	—
SD_RX02	Rx Data in	AG20	I	XCOREVDD	—
SD_RX01	Rx Data in	AG22	I	XCOREVDD	—
SD_RX00	Rx Data in	AG24	I	XCOREVDD	—
SD_RX_B03	Rx Data in, Inverted	AH18	I	XCOREVDD	—
SD_RX_B02	Rx Data in, Inverted	AH20	I	XCOREVDD	—
SD_RX_B01	Rx Data in, Inverted	AH22	I	XCOREVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
USB_D00/ IRQ02/ **GPIO53**	General Purpose I/O	N28	I/O	CVDD	—
SPI1_MOSI/ UART_SIN03/ SIM_SVEN/ **GPIO54**	General Purpose I/O	L22	I/O	CVDD	—
SPI1_MISO/ UART_CTS_B03/ SIM_RST_B/ **GPIO55**	General Purpose I/O	M22	I/O	CVDD	—
UART_SIN01/ **GPIO57**	General Purpose I/O	Y28	I/O	OVDD	—
ANT2_DIO009/ USB_CLK/ **GPIO59**	General Purpose I/O	F4	I/O	X2VDD	—
ANT2_DIO010/ USB_NXT/ **GPIO60**	General Purpose I/O	F5	I/O	X2VDD	—
ANT2_DIO011/ **GPIO61**	General Purpose I/O	F3	I/O	X2VDD	—
USB_D06/ UART_CTS_B02/ **GPIO62**	General Purpose I/O	P25	I/O	CVDD	—
USB_D05/ UART_RTS_B02/ **GPIO63**	General Purpose I/O	R22	I/O	CVDD	—
USB_CLK/ UART_SIN02/ **GPIO69**/ IRQ11/ TIMER03	General Purpose I/O	R24	I/O	CVDD	—
USB_D07/ UART_SOUT02/ **GPIO70**	General Purpose I/O	P28	I/O	CVDD	—
USB_D02/ IIC2_SDA/ **GPIO71**	General Purpose I/O	N26	I/O	CVDD	—
USB_D01/ IIC2_SCL/ **GPIO72**	General Purpose I/O	N27	I/O	CVDD	—
SDHC_DATA03/ DMA_DDONE_B00/ CKSTP1_IN_B/ **GPIO77**	General Purpose I/O	E25	I/O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SDHC_WP/ DMA_DREQ_B00/ CKSTP0_IN_B/ **GPIO78**	General Purpose I/O	G23	I/O	BVDD	—
SDHC_CD/ DMA_DACK_B00/ MCP1_B/ **GPIO79**/ IRQ10	General Purpose I/O	C25	I/O	BVDD	—
ANT1_RX_FRAME/ **GPIO80**	General Purpose I/O	R2	I/O	X1VDD	—
ANT1_DIO100/ **GPIO81**	General Purpose I/O	P4	I/O	X1VDD	—
ANT1_DIO101/ **GPIO82**	General Purpose I/O	R1	I/O	X1VDD	—
ANT1_DIO102/ **GPIO83**	General Purpose I/O	R5	I/O	X1VDD	—
ANT1_DIO103/ **GPIO84**	General Purpose I/O	R7	I/O	X1VDD	—
ANT1_DIO104/ **GPIO85**	General Purpose I/O	T1	I/O	X1VDD	—
ANT1_DIO105/ **GPIO86**	General Purpose I/O	T3	I/O	X1VDD	—
ANT1_DIO106/ **GPIO87**/ IRQ10	General Purpose I/O	T5	I/O	X1VDD	—
ANT1_DIO107/ **GPIO88**/ IRQ11	General Purpose I/O	T6	I/O	X1VDD	—
ANT2_RX_CLK/ **GPIO91**	General Purpose I/O	J3	I/O	X2VDD	—
ANT2_DIO104/ TDM1_RCK/ **GPIO92**	General Purpose I/O	K4	I/O	X2VDD	—
ANT1_RX_CLK/ TSEC_1588_TRIG_IN2/ **GPIO95**	General Purpose I/O	P2	I/O	X1VDD	—
GPO					
ANT4_TX_FRAME/ **GPO06**	General Purpose Output	Y3	O	X1VDD	—
IFC_ADDR16**/** **GPO08**	General Purpose Output	H26	O	BVDD	—
IFC_ADDR17**/** **GPO09**	General Purpose Output	H25	O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_ADDR18/ **GPO10**	General Purpose Output	H24	O	BVDD	—
IFC_ADDR19/ **GPO11**	General Purpose Output	H22	O	BVDD	—
IFC_ADDR20/ **GPO12**	General Purpose Output	H21	O	BVDD	—
IFC_ADDR21/ **GPO13**	General Purpose Output	J28	O	BVDD	—
IFC_ADDR22/ **GPO14**	General Purpose Output	J27	O	BVDD	—
IFC_ADDR23/ **GPO15**	General Purpose Output	J25	O	BVDD	—
IFC_ADDR24/ **GPO16**	General Purpose Output	J24	O	BVDD	—
IFC_ADDR25/ **GPO17**	General Purpose Output	J23	O	BVDD	—
IFC_ADDR26/ **GPO18**	General Purpose Output	J22	O	BVDD	—
ANT1_TXNRX/ TSEC_1588_PULSE_OUT2/ **GPO19**	General Purpose Output	P3	O	X1VDD	—
ANT1_TX_FRAME/ **GPO20**	General Purpose Output	R4	O	X1VDD	—
UART_RTS_B00/ PPS_LED/ **GPO43**	General Purpose Output	AB26	O	OVDD	—
UART_RTS_B01/ SYS_DMA_DONE/ **GPO45**/ ANT4_AGC	General Purpose Output	Y27	O	OVDD	—
IFC_CLE/ **GPO48**	General Purpose Output	L25	O	BVDD	—
IFC_OE_B/ **GPO49**	General Purpose Output	K23	O	BVDD	—
IFC_RB_B/ **GPO50**	General Purpose Output	K25	O	BVDD	—
IFC_WE_B/ **GPO52**	General Purpose Output	L26	O	BVDD	—
IFC_AVD/ **GPO54**	General Purpose Output	L28	O	BVDD	—
IFC_CS_B00/ **GPO55**	General Purpose Output	K21	O	BVDD	—
UART_SOUT01/ **GPO56**	General Purpose Output	W23	O	OVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
G1VDD	DDR Supply	E11	—	G1VDD	—
G1VDD	DDR Supply	H9	—	G1VDD	—
G1VDD	DDR Supply	H10	—	G1VDD	—
G1VDD	DDR Supply	H11	—	G1VDD	—
G1VDD	DDR Supply	H12	—	G1VDD	—
G1VDD	DDR Supply	H13	—	G1VDD	—
G1VDD	DDR Supply	H14	—	G1VDD	—
G1VDD	DDR Supply	H15	—	G1VDD	—
G1VDD	DDR Supply	H16	—	G1VDD	—
G1VDD	DDR Supply	H17	—	G1VDD	—
G1VDD	DDR Supply	H18	—	G1VDD	—
G1VDD	DDR Supply	H19	—	G1VDD	—
G1VDD	DDR Supply	H20	—	G1VDD	—
G1VDD	DDR Supply	B18	—	G1VDD	—
G1VDD	DDR Supply	B23	—	G1VDD	—
G1VDD	DDR Supply	D20	—	G1VDD	—
G1VDD	DDR Supply	E15	—	G1VDD	—
G2VDD	DDR Supply	AC3	—	G2VDD	—
G2VDD	DDR Supply	AC10	—	G2VDD	—
G2VDD	DDR Supply	AA8	—	G2VDD	—
G2VDD	DDR Supply	AA9	—	G2VDD	—
G2VDD	DDR Supply	AA10	—	G2VDD	—
G2VDD	DDR Supply	AA11	—	G2VDD	—
G2VDD	DDR Supply	AA12	—	G2VDD	—
G2VDD	DDR Supply	AA13	—	G2VDD	—
G2VDD	DDR Supply	AA14	—	G2VDD	—
G2VDD	DDR Supply	AA15	—	G2VDD	—
G2VDD	DDR Supply	AD6	—	G2VDD	—
G2VDD	DDR Supply	AD13	—	G2VDD	—
G2VDD	DDR Supply	AF2	—	G2VDD	—
G2VDD	DDR Supply	AG4	—	G2VDD	—
G2VDD	DDR Supply	AG9	—	G2VDD	—
G2VDD	DDR Supply	AG12	—	G2VDD	—
G2VDD	DDR Supply	AC15	—	G2VDD	—
LVDD	Ethernet Supply	Y23	—	LVDD	—
LVDD	Ethernet Supply	AA25	—	LVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	G2	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	J4	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	J8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	K6	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	K8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	L8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	M8	—	X2VDD	—
XCOREVDD	SerDes Core Logic Supply	AH19	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AH23	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AH27	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG25	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AF16	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG17	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG21	—	XCOREVDD	—
XPADVDD	SerDes Transceiver Supply	AA19	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AA20	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF18	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AE20	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF22	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF26	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AE24	—	XPADVDD	—
Ground					
VSS	Platform and Core Ground	A9	—	—	—
VSS	Platform and Core Ground	A26	—	—	—
VSS	Platform and Core Ground	B2	—	—	—
VSS	Platform and Core Ground	B8	—	—	—
VSS	Platform and Core Ground	B11	—	—	—
VSS	Platform and Core Ground	B15	—	—	—
VSS	Platform and Core Ground	B21	—	—	—
VSS	Platform and Core Ground	C27	—	—	—
VSS	Platform and Core Ground	D17	—	—	—

Table 10. I/O Power (continued)

PS#	Primary pin name	Pin width	Voltage domain	Recommended value	Current max	Typical current (A)	Max (A)	Note
SD	SVDD	—	SerDes Core logic supply	1.0V	—	0.144	0.144	—
	XVDD	—	SerDes I/O supply	1.5V	—	0.058	0.058	—
Analog	AVDD_CORE0	—	Core 0 PLL supply	1.0V	—	0.005	0.015	—
	AVDD_CORE1	—	Core 1 PLL supply		—			—
	AVDD_DSP	—	DSP PLL supply		—			—
	AVDD_PLAT	—	Platform PLL supply		—			—
	AVDD_D1_DDR	—	DDR PLL supply		—			—
	AVDD_D2_DDR	—	DDR PLL supply		—			—
	SDAVDD1	—	SerDes PLL supply		—			—
	SDAVDD2	—	SerDes PLL supply		—			—

Note:

1 For DDR typical, it is 40% DIMM utilization.

2 For DDR max, it is 75% DIMM utilization.

3 For I/O with different possible voltages, the currents listed above are for the higher voltage.

2.7 Input Clocks

This section provides information about the system clock specifications, spread spectrum sources, real time clock specifications, TDM clock specifications, and other input sources.

2.7.1 System Clock and DDR Clock Specifications

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) 3.3 V DC specifications.

Table 11. SYSCLK/DDRCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) AC timing specifications.

Table 12. SYSCLK/DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	66	—	100	MHz	1, 2

Table 12. SYSCLK/DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DDRCLK frequency	f_{DDRCLK}	66	—	166	MHz	1
DDRCLK cycle time	t_{DDRCLK}	6.0	—	15.15	ns	—
SYSCLK/DDRCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK/DDRCLK slew rate	—	1	—	4	V/ns	3
SYSCLK/DDRCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK/DDRCLK jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.2 DSP Clock (DSPCLKIN) Specifications

This table provides the DSP clock (DSPCLKIN) 3.3 V DC specifications.

Table 13. DSPCLKIN DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the DSP clock (DSPCLKIN) AC timing specifications.

Table 14. DSPCLKIN AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
DSPCLKIN frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
DSPCLKIN cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DSPCLKIN duty cycle	t_{KHK}/ t_{SYSCLK}	40	—	60	%	2
DSPCLKIN slew rate	—	1	—	4	V/ns	3

2.8.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 19. DDR3L SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.090	V	5
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.3	mA	6, 7
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Table 19. DDR3L SDRAM Interface DC Electrical Characteristics (continued)

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver.Peak-to-peak noise on MVREFn may not exceed the MVREFn DC level by more than ±1% of GV_{DD} (i.e. ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. IOH and IOL are measured at GV_{DD} = 1.282 V
7. See the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR controller interface capacitance for DDR3.

Table 20. DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, DQS_B	C_{IO}	6	8	pF	—
Delta input/output capacitance: DQ, DQS, DQS_B	C_{DIO}	—	0.5	pF	—

This table provides the current draw characteristics for MVREF*n*.

Table 21. Current Draw Characteristics for MVREF*n*

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MVREF*n*	I_{MVREFn}	—	700	μA	—
Current draw for DDR3L SDRAM for MVREF*n*	I_{MVREFn}	—	700	μA	—

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1333 MHz data rate		250	—		
1200 MHz data rate		275	—		
1066 MHz data rate		300	—		
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1333 MHz data rate		250	—		
1200 MHz data rate		275	—		
1066 MHz data rate		300	—		
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Table 35. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	10	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.11.2.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

Table 42. USB General Timing Parameters (ULPI Mode) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 19 and Figure 20 provide the USB AC test load and signals, respectively.

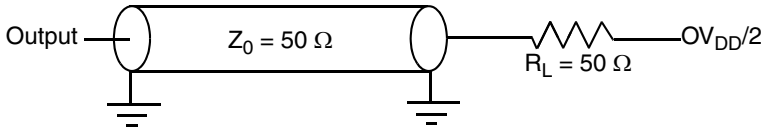

Figure 19. USB AC Test Load

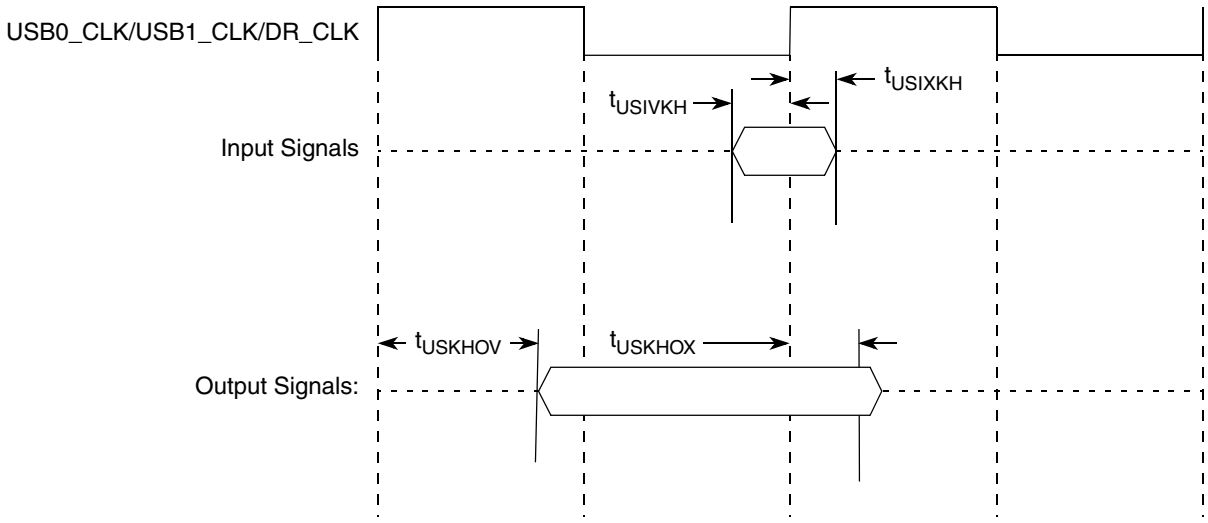

Figure 20. USB Signals

Table 50. PIC DC Electrical Characteristics (3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

This table provides the DC electrical characteristics for the PIC interface when operating at $LV_{DD}/OV_{DD}/BV_{DD}/CV_{DD}$ = 2.5 V.

Table 51. PIC DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

This table provides the DC electrical characteristics for the PIC interface when operating at $LV_{DD}/OV_{DD}/BV_{DD}/CV_{DD}$ = 1.8 V.

Table 52. PIC DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—

Table 58. I²C AC Electrical Specifications (continued)

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 56)

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

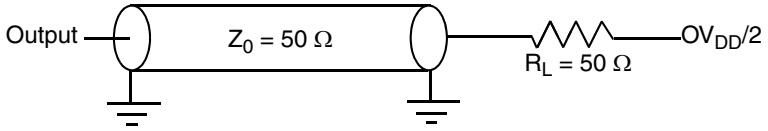

Figure 30. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

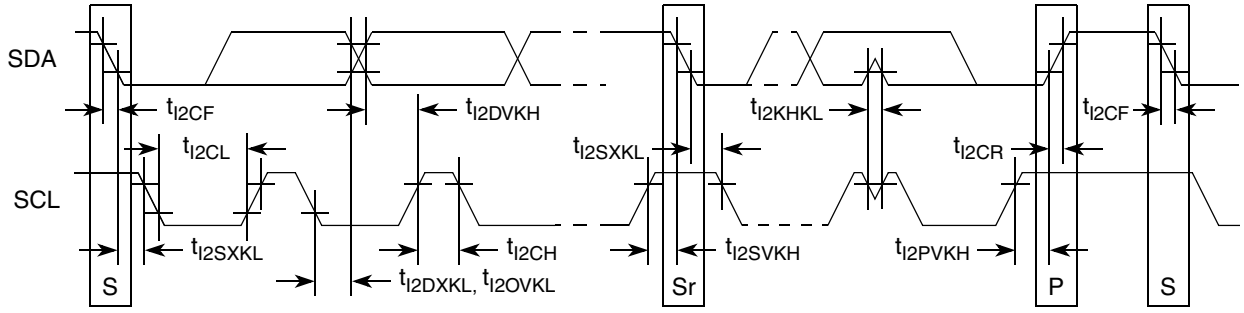

Figure 31. I²C Bus AC Timing Diagram

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface.

— To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD_REF_CLK[1–2]_B) through the same source impedance as the clock input (SD_REF_CLK[1–2]) in use.

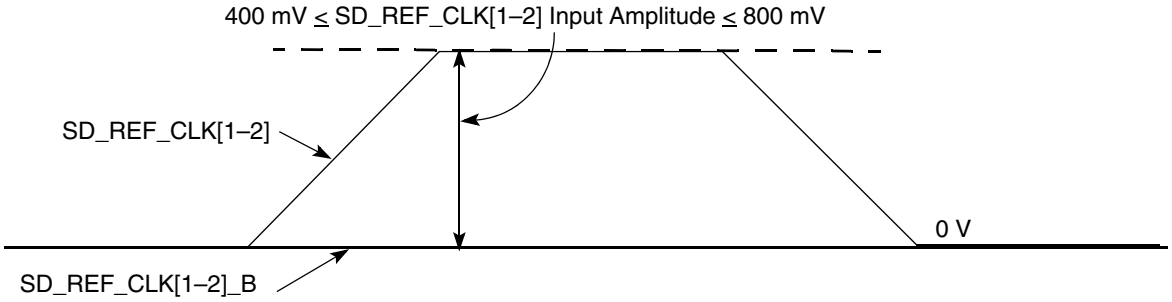

Figure 41. Single-Ended Reference Clock Input DC Requirements

2.20.2.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The BSC9132 supports a 2.5 Gbps and a 5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The transmitter specifications for 2.5 Gbps are defined in Table 67 and the receiver specifications are defined in Table 68. For 5 Gbps, the transmitter specifications are defined in Table 69 and the receiver specifications are defined in Table 1.

Note that specifications are valid at the recommended operating conditions listed in Table 3.

Table 67. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Differential peak-to-peak output voltage swing	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low Impedance
DC single-ended TX impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Table 68. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	5

Table 77. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. This does not include spread spectrum or REF_CLK jitter. It includes device random jitter at 10^{-12}. See notes 2 and 3.
Time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-NAX-JITTER} = 0.25$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2, 3, and 4.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Comments

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 47 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3 A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4 It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 79. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

3.13.2 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

3.14 Security Fuse Processor

This device implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD1} pin per Section 2.2, "Power Sequencing." POV_{DD1} should only be powered for the duration of the fuse programming cycle, with a per device limit of one fuse programming cycle. All other times POV_{DD1} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD1} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD1} to GND.

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters

The package parameters are provided in the following list. The package type is plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23 mm
Interconnects	780
Pitch	0.8 mm
Ball diameter (typical)	0.4 mm