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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SC3850, Security; SEC 4.4
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Random Number Generator
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/bsc9132nxe7mnmb

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D1_MDM03	Data Mask	C11	O	G1VDD	—
D1_MDQS00	Data Strobe	C16	I/O	G1VDD	—
D1_MDQS01	Data Strobe	A14	I/O	G1VDD	—
D1_MDQS02	Data Strobe	C13	I/O	G1VDD	—
D1_MDQS03	Data Strobe	A12	I/O	G1VDD	—
D1_MDQS_B00	Data Strobe	D16	I/O	G1VDD	—
D1_MDQS_B01	Data Strobe	B14	I/O	G1VDD	—
D1_MDQS_B02	Data Strobe	D13	I/O	G1VDD	—
D1_MDQS_B03	Data Strobe	B12	I/O	G1VDD	—
D1_MBA00	Bank Select	C23	O	G1VDD	—
D1_MBA01	Bank Select	A23	O	G1VDD	—
D1_MBA02	Bank Select	C24	O	G1VDD	—
D1_MA00	Address	E22	O	G1VDD	—
D1_MA01	Address	A24	O	G1VDD	—
D1_MA02	Address	B24	O	G1VDD	—
D1_MA03	Address	B20	O	G1VDD	—
D1_MA04	Address	A25	O	G1VDD	—
D1_MA05	Address	D21	O	G1VDD	—
D1_MA06	Address	A21	O	G1VDD	—
D1_MA07	Address	C21	O	G1VDD	—
D1_MA08	Address	B22	O	G1VDD	—
D1_MA09	Address	E23	O	G1VDD	—
D1_MA10	Address	B25	O	G1VDD	—
D1_MA11	Address	C22	O	G1VDD	—
D1_MA12	Address	D23	O	G1VDD	—
D1_MA13	Address	G19	O	G1VDD	—
D1_MA14	Address	G22	O	G1VDD	—
D1_MA15	Address	F22	O	G1VDD	—
D1_MWE_B	Write Enable	D19	O	G1VDD	—
D1_MRAS_B	Row Address Strobe	A22	O	G1VDD	—
D1_MCAS_B	Column Address Strobe	F19	O	G1VDD	—
D1_MCS_B00	Chip Select	C20	O	G1VDD	—
D1_MCS_B01	Chip Select	F20	O	G1VDD	—
D1_MCS_B02	Chip Select	E20	O	G1VDD	—
D1_MCS_B03	Chip Select	G20	O	G1VDD	—
D1_MCKE00	Clock Enable	A20	O	G1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MDQ13	Data	AF9	I/O	G2VDD	—
D2_MDQ14	Data	AF8	I/O	G2VDD	—
D2_MDQ15	Data	AE9	I/O	G2VDD	—
D2_MDQ16	Data	AG13	I/O	G2VDD	—
D2_MDQ17	Data	AD11	I/O	G2VDD	—
D2_MDQ18	Data	AD10	I/O	G2VDD	—
D2_MDQ19	Data	AG10	I/O	G2VDD	—
D2_MDQ20	Data	AE12	I/O	G2VDD	—
D2_MDQ21	Data	AF12	I/O	G2VDD	—
D2_MDQ22	Data	AH13	I/O	G2VDD	—
D2_MDQ23	Data	AF11	I/O	G2VDD	—
D2_MDQ24	Data	AD14	I/O	G2VDD	—
D2_MDQ25	Data	AC12	I/O	G2VDD	—
D2_MDQ26	Data	AC14	I/O	G2VDD	—
D2_MDQ27	Data	AB14	I/O	G2VDD	—
D2_MDQ28	Data	AB12	I/O	G2VDD	—
D2_MDQ29	Data	AD15	I/O	G2VDD	—
D2_MDQ30	Data	AD12	I/O	G2VDD	—
D2_MDQ31	Data	AC13	I/O	G2VDD	—
D2_MDM00	Data Mask	AB8	O	G2VDD	—
D2_MDM01	Data Mask	AD9	O	G2VDD	—
D2_MDM02	Data Mask	AH12	O	G2VDD	—
D2_MDM03	Data Mask	AB13	O	G2VDD	—
D2_MDQS00	Data Strobe	AG8	I/O	G2VDD	—
D2_MDQS01	Data Strobe	AE10	I/O	G2VDD	—
D2_MDQS02	Data Strobe	AG11	I/O	G2VDD	—
D2_MDQS03	Data Strobe	AE13	I/O	G2VDD	—
D2_MDQS_B00	Data Strobe	AH8	I/O	G2VDD	—
D2_MDQS_B01	Data Strobe	AF10	I/O	G2VDD	—
D2_MDQS_B02	Data Strobe	AH11	I/O	G2VDD	—
D2_MDQS_B03	Data Strobe	AF13	I/O	G2VDD	—
D2_MBA00	Bank Select	AC2	O	G2VDD	—
D2_MBA01	Bank Select	AB4	O	G2VDD	—
D2_MBA02	Bank Select	AB3	O	G2VDD	—
D2_MA00	Address	AB6	O	G2VDD	—
D2_MA01	Address	AA5	O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO007/ USB_D07/ GPIO32	Data	G3	I/O	X2VDD	—
ANT2_DIO008/ USB_DIR/ GPIO33	Data	F2	I/O	X2VDD	—
ANT2_DIO009/ USB_CLK/ GPIO59	Data	F4	I/O	X2VDD	—
ANT2_DIO010/ USB_NXT/ GPIO60	Data	F5	I/O	X2VDD	—
ANT2_DIO011/ GPIO61	Data	F3	I/O	X2VDD	—
ANT2_DIO100/ TDM1_TCK	Data	H1	I	X2VDD	—
ANT2_DIO101/ TDM1_TFS	Data	K5	I	X2VDD	—
ANT2_DIO102/ TDM1_RXD	Data	J7	I	X2VDD	—
ANT2_DIO103/ TDM1_TXD	Data	L5	I	X2VDD	—
ANT2_DIO104/ TDM1_RCK/ GPIO92	Data	K4	I	X2VDD	—
ANT2_DIO105/ TDM1_RFS/ TIMER08	Data	K7	I	X2VDD	—
ANT2_DIO106/ IRQ04	Data	L4	I	X2VDD	—
ANT2_DIO107/ IRQ05	Data	K3	I	X2VDD	—
ANT2_DIO108/ IRQ06	Data	L2	I	X2VDD	—
ANT2_DIO109/ IRQ07	Data	J2	I	X2VDD	—
ANT2_DIO110	Data	L3	I	X2VDD	—
ANT2_DIO111	Data	L1	I	X2VDD	—
RF Interface 3					
ANT2_REF_CLK/ **ANT3_AGC**	AGC	K1	O	X2VDD	—
ANT3_TX_CLK	Transmit Clock	D3	O	X2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT4_TXNRX	TX_RX Control	Y6	O	X1VDD	—
ANT4_ENABLE/ SYS_DMA_DONE	Antenna Enable	Y2	O	X1VDD	—
ANT4_TX_FRAME/ GPO06	Transmit Frame	Y3	O	X1VDD	2
ANT4_RX_FRAME/ GPIO05	Receive Frame	Y5	I	X1VDD	—
ANT4_DIO000/ TIMER05	Data	U5	I/O	X1VDD	—
ANT4_DIO001/ SYS_DMA_REQ	Data	U6	I/O	X1VDD	—
ANT4_DIO002/ IRQ00	Data	V1	I/O	X1VDD	—
ANT4_DIO003/ IRQ01	Data	V4	I/O	X1VDD	—
ANT4_DIO004/ IRQ02	Data	V2	I/O	X1VDD	—
ANT4_DIO005/ IRQ03	Data	V3	I/O	X1VDD	—
ANT4_DIO006/ IRQ_OUT_B	Data	U7	I/O	X1VDD	—
ANT4_DIO007/ MCP1_B	Data	V5	I/O	X1VDD	—
ANT4_DIO008/ MCP0_B	Data	V7	I/O	X1VDD	—
ANT4_DIO009/ CKSTP0_IN_B	Data	W1	I/O	X1VDD	—
ANT4_DIO010/ CKSTP1_IN_B	Data	W3	I/O	X1VDD	—
ANT4_DIO011/ SRESET_B	Data	W4	I/O	X1VDD	—
System Control/Power Management					
HRESET_REQ_B	Hard Reset Request Out	T27	O	OVDD	4
UART_CTS_B01/ SYS_DMA_REQ/ **SRESET_B**/ GPIO44/ IRQ05	Soft Reset over UART	W22	I	OVDD	—
ANT4_DIO011/ **SRESET_B**	Soft Reset over RF 4	W4	I	X1VDD	—
SPI1_CS2_B/ **CKSTP0_OUT_B**/ GPO75	Checkstop Out	M25	O	CVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO111/ **TIMER07**/ GPIO24	Timer 7	U3	I/O	X1VDD	—
ANT2_DIO105/ TDM1_RFS/ **TIMER08**	Timer 8	K7	I/O	X2VDD	—
OCeaN DMA					
SDHC_DATA03/ **DMA_DDONE_B00**/ CKSTP1_IN_B/ GPIO77	DMA done	E25	I/O	BVDD	
ANT2_TX_FRAME/ **DMA_DDONE_B00**	DMA done	G4	O	X2VDD	
SDHC_WP/ **DMA_DREQ_B00**/ CKSTP0_IN_B/ GPIO78	DMA request	G23	I	BVDD	—
ANT2_RX_FRAME/ **DMA_DREQ_B00**	DMA request	H3	I	X2VDD	—
SDHC_CD/ **DMA_DACK_B00**/ MCP1_B/ GPIO79/ IRQ10	DMA acknowledge	C25	O	BVDD	—
ANT2_TXNRX/ **DMA_DACK_B00**	DMA acknowledge	H2	O	X2VDD	—
System DMA					
ANT4_ENABLE/ **SYS_DMA_DONE**	System DMA done	Y2	O	X1VDD	—
UART_RTS_B01/ **SYS_DMA_DONE**/ GPO45/ ANT4_AGC	System DMA done	Y27	O	OVDD	—
UART_CTS_B01/ **SYS_DMA_REQ**/ SRESET_B/ GPIO44/ IRQ05	System DMA request	W22	I	OVDD	—
ANT4_DIO001/ **SYS_DMA_REQ**	System DMA request	U6	I	X1VDD	—
Interrupts					
USB_D04/ GPIO00/ **IRQ00**	External Interrupt	P26	I	CVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	T15	—	—	—
VSS	Platform and Core Ground	T17	—	—	—
VSS	Platform and Core Ground	T19	—	—	—
VSS	Platform and Core Ground	T20	—	—	—
VSS	Platform and Core Ground	T24	—	—	—
VSS	Platform and Core Ground	U27	—	—	—
VSS	Platform and Core Ground	U15	—	—	—
VSS	Platform and Core Ground	U17	—	—	—
VSS	Platform and Core Ground	U19	—	—	—
VSS	Platform and Core Ground	V15	—	—	—
VSS	Platform and Core Ground	V17	—	—	—
VSS	Platform and Core Ground	V19	—	—	—
VSS	Platform and Core Ground	W15	—	—	—
VSS	Platform and Core Ground	W17	—	—	—
VSS	Platform and Core Ground	W19	—	—	—
VSS	Platform and Core Ground	W20	—	—	—
VSS	Platform and Core Ground	W21	—	—	—
VSS	Platform and Core Ground	W24	—	—	—
VSS	Platform and Core Ground	W28	—	—	—
VSS	Platform and Core Ground	Y21	—	—	—
VSS	Platform and Core Ground	Y15	—	—	—
VSS	Platform and Core Ground	Y17	—	—	—
VSS	Platform and Core Ground	Y19	—	—	—
VSS	Platform and Core Ground	Y26	—	—	—
VSS	Platform and Core Ground	AB28	—	—	—
VSS	Platform and Core Ground	AA21	—	—	—
VSS	Platform and Core Ground	AD16	—	—	—
VSS	Platform and Core Ground	AE27	—	—	—
VSS	Platform and Core Ground	AF28	—	—	—
VSS	Platform and Core Ground	AG16	—	—	—
VSS	Platform and Core Ground	AD1	—	—	—
VSS	Platform and Core Ground	AE4	—	—	—
VSS	Platform and Core Ground	AE8	—	—	—
VSS	Platform and Core Ground	AE11	—	—	—
VSS	Platform and Core Ground	AF14	—	—	—
VSS	Platform and Core Ground	AG7	—	—	—

2.8.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 19. DDR3L SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.090	V	5
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.3	mA	6, 7
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1333 MHz data rate		250	—		
1200 MHz data rate		275	—		
1066 MHz data rate		300	—		
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1333 MHz data rate		250	—		
1200 MHz data rate		275	—		
1066 MHz data rate		300	—		
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

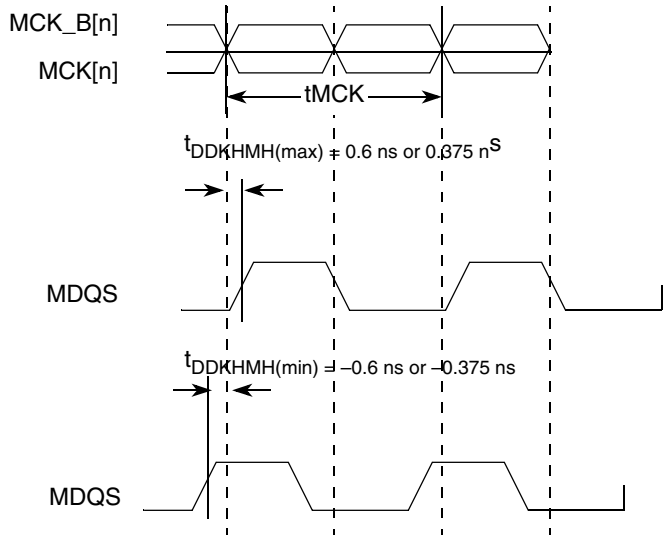


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

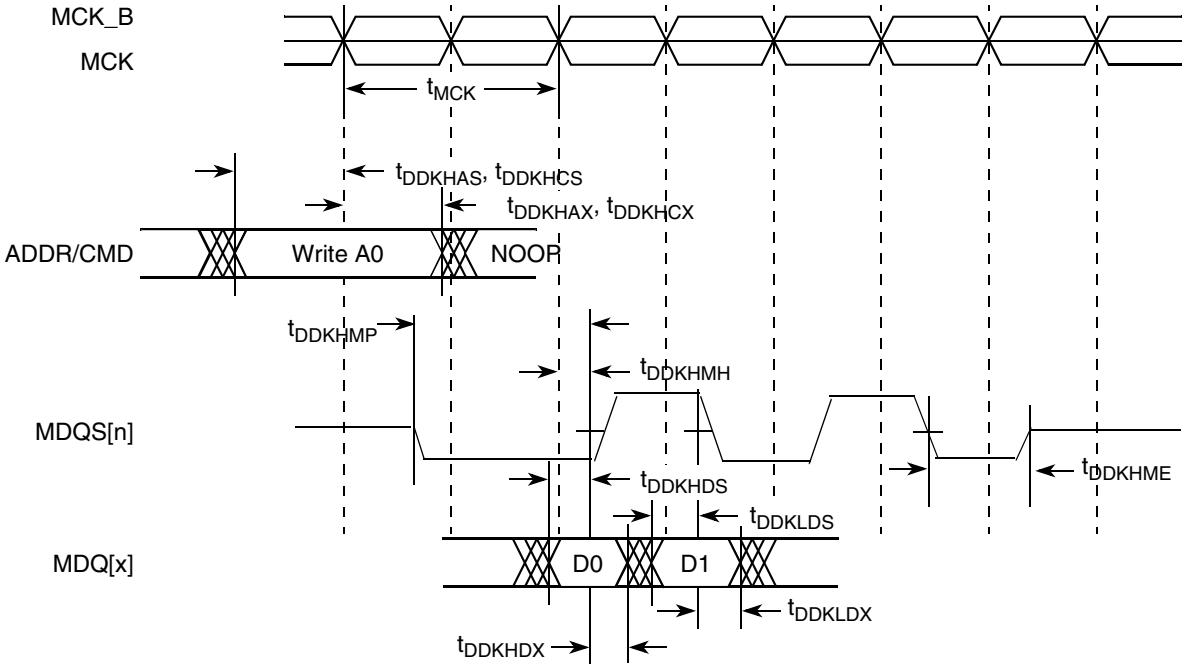


Figure 11. DDR3 and DDR3L Output Timing Diagram

Table 38. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V) (continued)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.11.3.2 eTSEC IEEE Std 1588 AC Specifications

This table provides the IEEE Std 1588 AC timing specifications.

Table 39. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	5	—	T_{RX_CLK}*7	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns respectively.

Table 52. PIC DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.15.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

Table 53. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating from 3.3-V supply.

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 2.5-V supply.

Table 60. GPIO DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OH}	1.7	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.7	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 1.8-V supply.

Table 61. GPIO DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

2.20.1 SerDes

2.20.1.1 SerDes Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 36 shows how the signals are defined. Figure 36 shows the waveform for either a transmitter output (SD_TX[0:3] and SD_TX_B[0:3]) or a receiver input (SD_RX[0:3] and SD_RX_B[0:3]). Each signal swings between X volts and Y volts where X > Y.

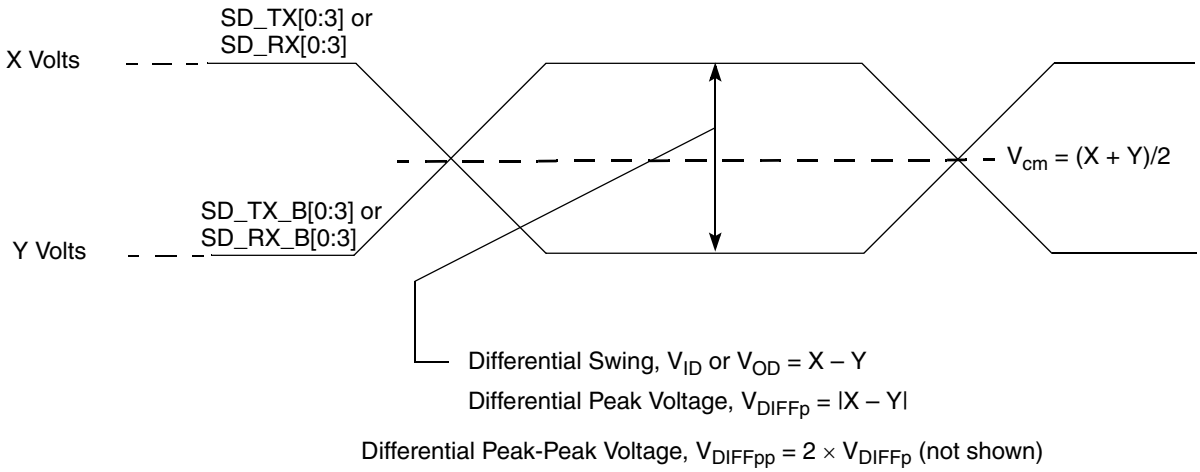


Figure 36. Differential Voltage Definitions for Transmitter/Receiver

This table lists the definitions based on this waveform. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

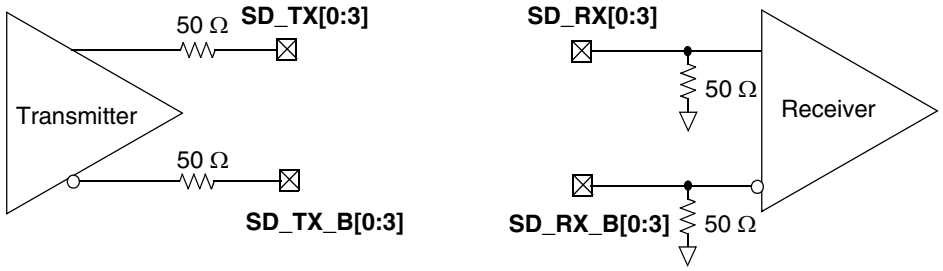
Table 66. Differential Signal Definitions

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals SD_TX[0:3], SD_TX_B[0:3], SD_RX[0:3] and SD_RX_B[0:3] each have a peak-to-peak swing of X – Y volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, VOD (or Differential Output Swing):	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX[0:3]} - V_{SD\_TX\_B[0:3]}$. The V_{OD} value can be either positive or negative.
Differential Input Voltage, VID (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX[0:3]} - V_{SD\_RX\_B[0:3]}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, V_{DIFFp}	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |X– Y| volts.
Differential Peak-to-Peak, $V_{DIFFp-p}$	Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 × V_{DIFFp} = 2 × |(A – B)| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 × |V_{OD}|.

- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA) while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in Section 2.20.2.1, "DC-Level Requirements for SerDes Reference Clocks."

2.20.1.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [0:3] indicates the specific SerDes lane. Actual signals are assigned by the RCW assignments at reset.

Figure 38. SerDes Transmitter and Receiver Reference Circuits

2.20.1.4 SerDes Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond that allowed by the specification. To offset a portion of these effects, equalization can be used. The following is a list of the most commonly used equalization techniques:

- Pre-emphasis on the transmitter.
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.20.2 HSSI DC Timing Specifications

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the CPRI data lines, and the SGMII data lines.

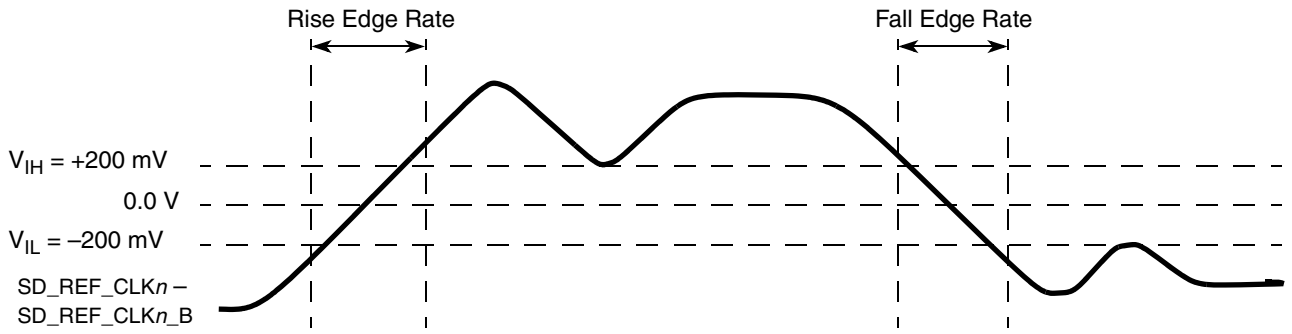


Figure 42. Differential Measurement Points for Rise and Fall Time

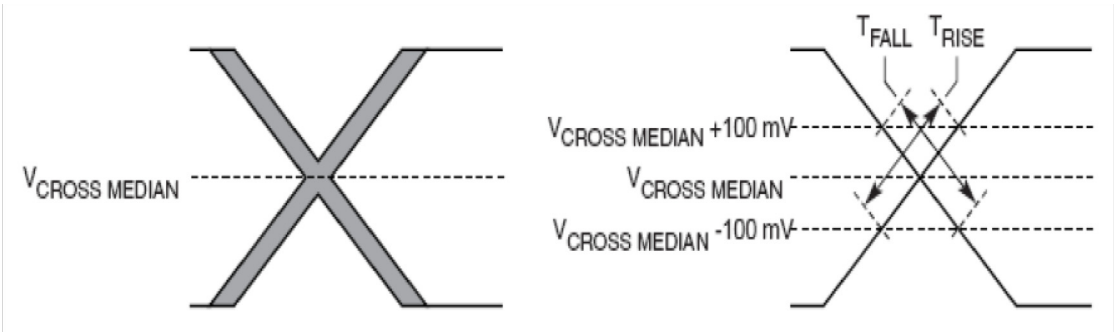


Figure 43. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.3.2 Spread Spectrum Clock

SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have the same reference clock and the industry protocol supports it. For better results, use a source without significant unintended modulation.

2.20.3.3 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The BSC9132 supports a 2.5 Gbps or a 5.0 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The 2.5 Gbps transmitter specifications are defined in Table 77 and the receiver specifications are defined in Table 78. The 5.0 Gbps transmitter specifications are defined in Table 79 and the receiver specifications are defined in Table 80. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Table 77. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.

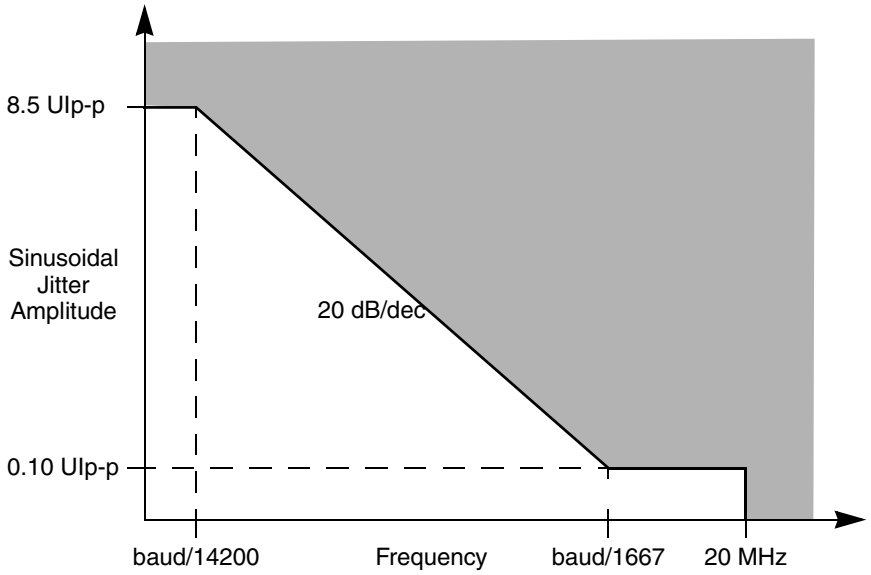


Figure 44. Single Frequency Sinusoidal Jitter Limits for Baud Rate <3.125 Gbps

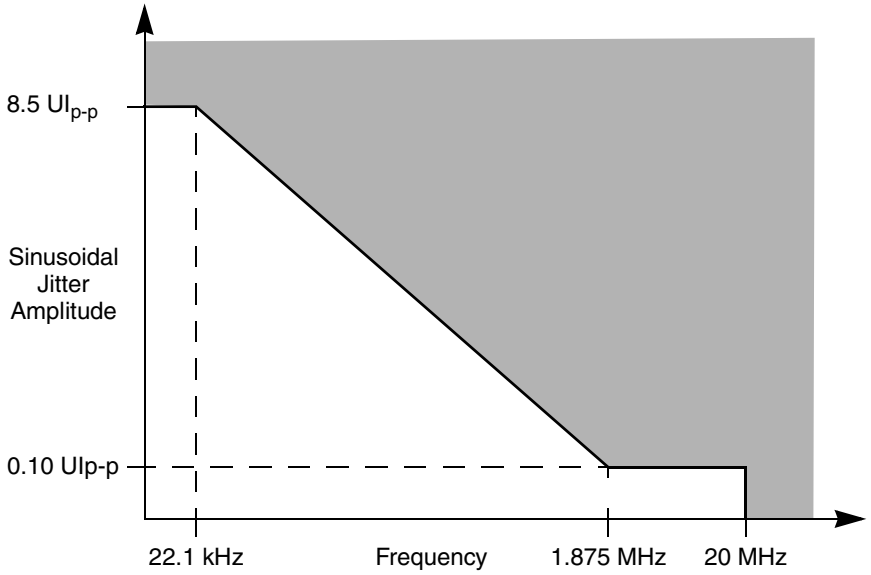


Figure 45. Single Frequency Sinusoidal Jitter Limits for Baud Rate 3.125 Gbps

2.22.3 USIM External Pull Up/Pull Down Resistor Requirements

External off-chip pull up resistor of 20 KΩ is required on the SIM_TRXD pin.

External off-chip pull down resistors are required on the SIM_PD, SIM_SVEN, SIM_RST pins.

2.22.4 USIM Reset Sequence

2.22.4.1 SIM Cards With Internal Reset

The sequence of reset for this kind of SIM cards is as follows (see Figure 51):

- After power up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, Rx must be high.
- The card must send a response on Rx acknowledging the reset between 400 and 40000 clock cycles after T0.

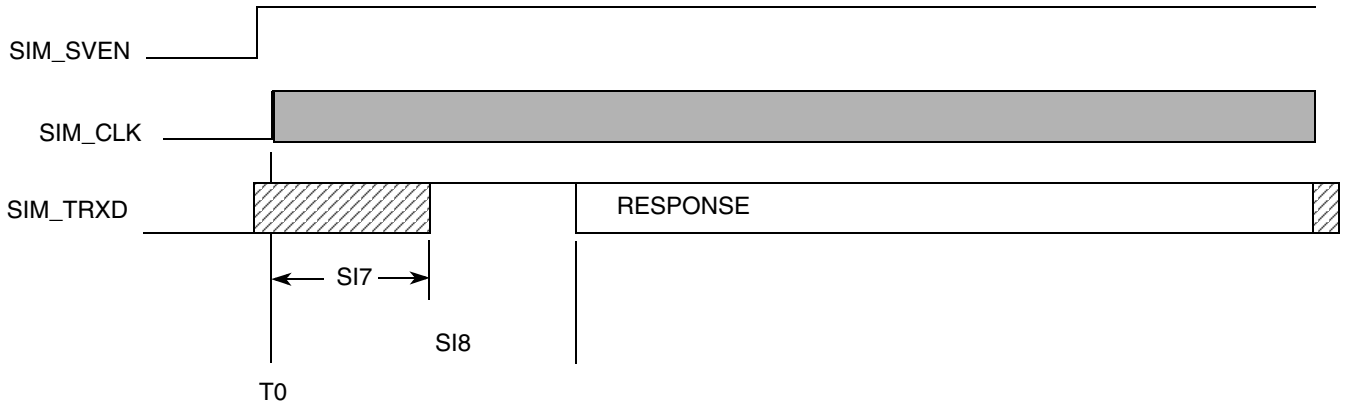


Figure 51. Internal-Reset Card Reset Sequence

Table 93. Parameters of Reset Sequence For Card With Internal Reset

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM clock to SIM TX data H	$S_{clk2dat}$	—	200	SIM_CLK clock cycle
SI8	SIM clock to SIM get ATR data	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle

2.22.4.2 SIM Cards With Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 52):

- After powering up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, SIM_TRXD must be high.
- SIM_RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on Rx during those 40000 clock cycles).
- SIM_RST is set High (time T1).
- SIM_RST must remain High for at least 40000 clock cycles after T1 and a response must be received on SIM_TRXD between 400 and 40000 clock cycles after T1.

Table 107. Default Voltage Level for CV_{DD}

CVDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 108. Default Voltage Level for $X1V_{DD}$

X1VDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 109. Default Voltage Level for $X2V_{DD}$

XVDD2_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 110. Default Voltage Level for LV_{DD}

LVDD_VSEL	I/O Voltage Level
0	3.3 V
1	2.5 V

3.4 PLL Power Supply Design

Each of the PLLs listed above is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE0, AVDD_CORE1, AVDD_D1_DDR, AVDD_D2_DDR, AVDD_DSP, and AVDD_MAPLE respectively). The AV_{DD} level should always be equivalent to V_{DDC}, and these voltages must be derived directly from V_{DDC} through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 55, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 780 ball FCPBGA the footprint, without the inductance of vias.

3.6 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ($XCOREV_{DD}$ and $XPADV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

- The board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- There should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Between the device and any SerDes voltage regulator there should be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

Figure 56 shows the SerDes PLL power supply filter circuit.

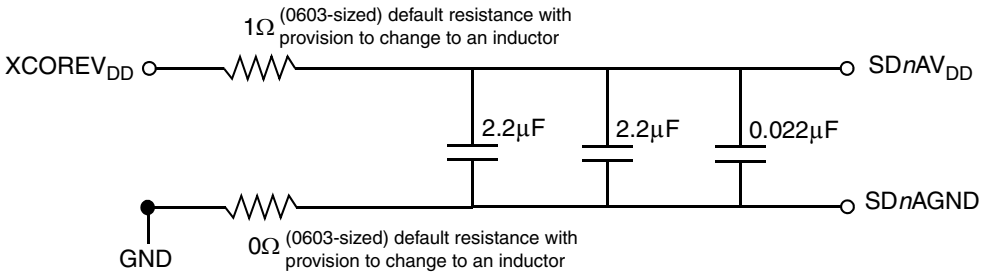


Figure 56. SerDes PLL Power Supply Filter Circuit

The power supplied to the $XCOREV_{DD}$ and $XPADV_{DD}$ are filtered using a circuit similar to Figure 57.

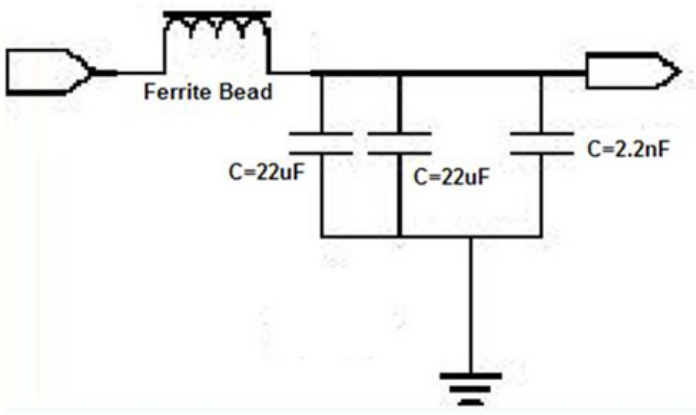


Figure 57. $XCOREV_{DD}$ and $XPADV_{DD}$ Power Supply Filter Circuit

The $XCOREV_{SS}$ and $XPADV_{SS}$ of different banks can be joined to a low noise, solid reference ground plane. Perform the noise coupling simulation on actual PCB design implementation. The user should quantify the noise and then and then take appropriate PCB layout tradeoff decisions, followed by validating the simulated noise against the measured noise for the designed PCB.

In case of a board noise coupling issue, the user may use separate islands/thick wide traces for $XCOREV_{SS}$, $XPADV_{SS}$, $XCOREV_{DD}$ and $XPADV_{DD}$. Connect these “islands" together to a single supply plane; it would be best for this connection to be a single point or multiple single-point connections as close to the source (and as far away from the chip) as possible.

3.13.2 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

3.14 Security Fuse Processor

This device implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD1} pin per Section 2.2, "Power Sequencing." POV_{DD1} should only be powered for the duration of the fuse programming cycle, with a per device limit of one fuse programming cycle. All other times POV_{DD1} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD1} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD1} to GND.

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters

The package parameters are provided in the following list. The package type is plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23 mm
Interconnects	780
Pitch	0.8 mm
Ball diameter (typical)	0.4 mm